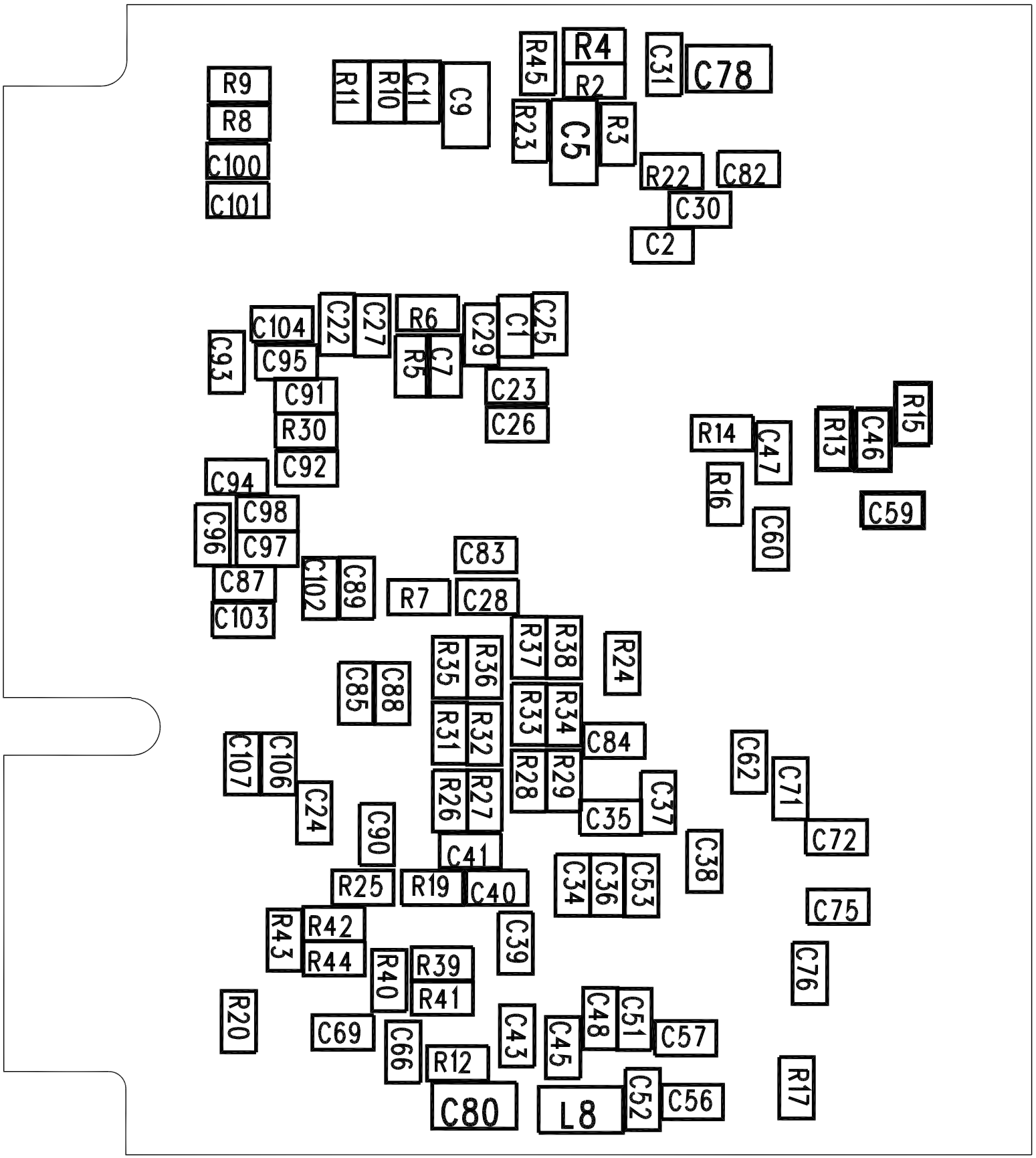
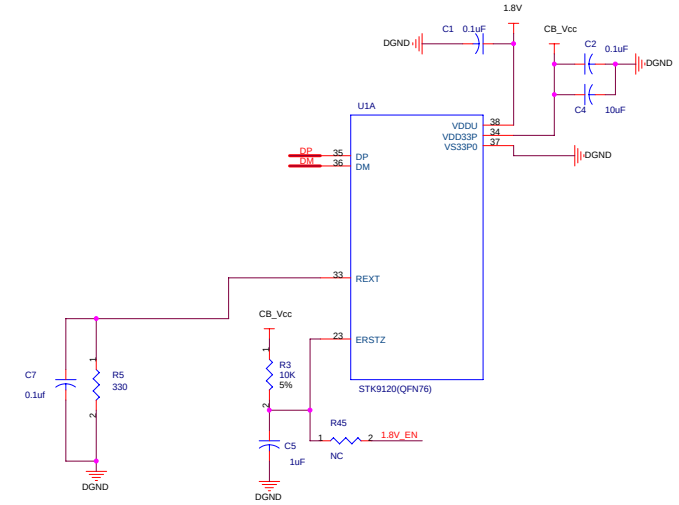
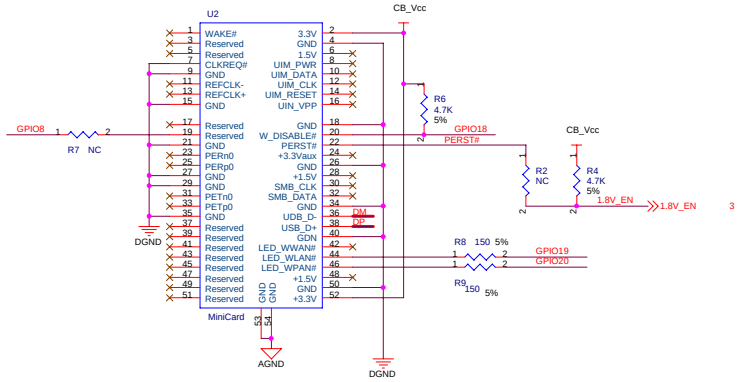
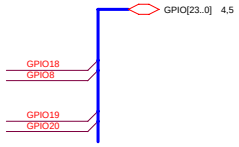
C74
R21
U8
R18
C44
L12
U4
ANT2
C73
C17
C16
C58
L1
L3
C33
C50
L7
L9
L11
C61
C55
C64
C54
C65
C99
C13
C32
U7
C70
C49
C68
C63
L10
C67
C3
U5
U6
C42
U1
C81
C4
L15
C20
ANT1
L4
C105
C86
U3
L2
U10
U9
C10


R9
R8
C100
C101
R11
R10
C11
C9
R45
R4
R2
C31
C78
R23
C5
R3
R22
C82
C30
C2
C104
C22
C27
R6
C29
C1
C25
C93
C95
R5
C7
C23
C26
C91
R30
C92
C94
C98
C96
C97
C87
C103
C102
C89
C83
R7
C28
R14
C47
R16
C60
R13
C46
R15
C59
R37
R38
R24
R35
R36
C85
C88
R33
R34
C84
R31
R32
C107
C106
C24
R28
R29
C62
C71
C72
R26
R27
C35
C37
C90
C41
C38
R25
R19
C40
C34
C36
C53
C75
R43
R42
R44
C39
C76
R40
R39
R41
R20
C69
C66
C43
C48
C51
C57
C45
R12
C80
L8
C52
C56
R17

Refer to Layout Reference for placement info







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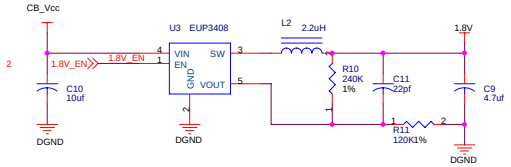
Thick trace to handle 1A @ 3.3V

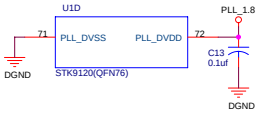


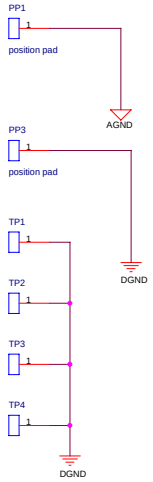
PUT A LOT OF COPPER ARROUND

TO ABSORB HEAT

Thick trace to handle 10mA @ 2.0V

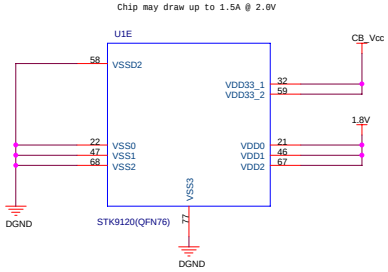
Run as a trace not plane

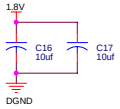




These need to be placed close to power pins

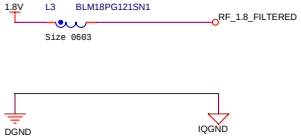
These ones should be on top

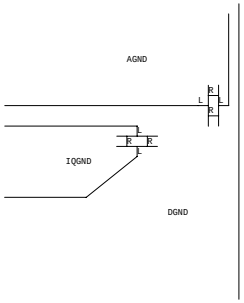




The traces should run through the Caps

Thick trace to handle .3A @ 2.0V

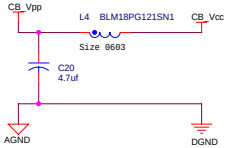


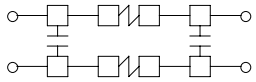


Place between Digital and RF power sections on the board

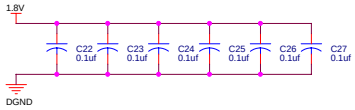
Thick traces to handle 1A at 3.3V

The traces should run through the Caps

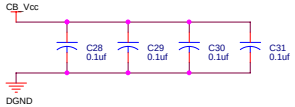




These need to be placed close to power pins



These need to be placed close to power pins



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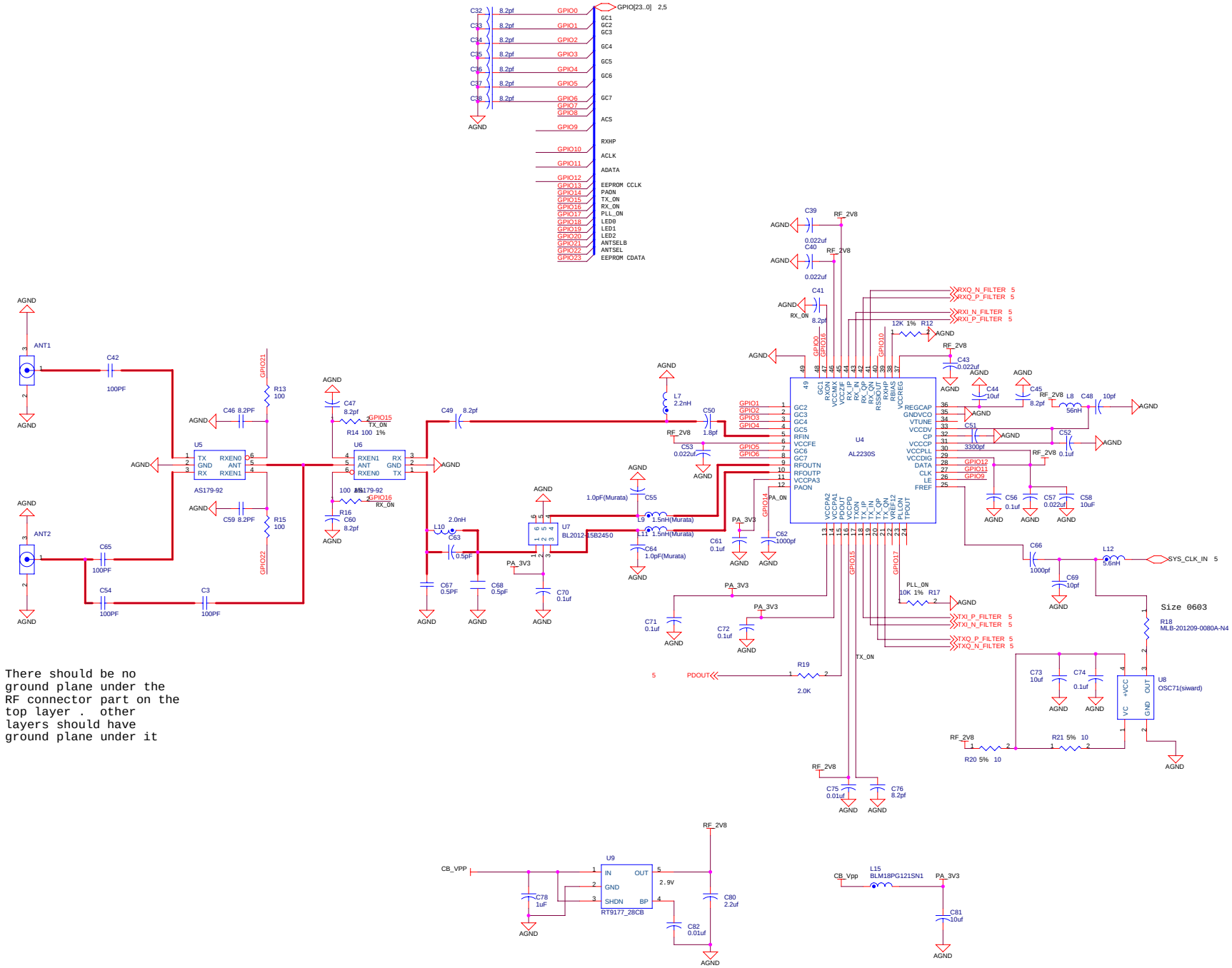

There should be no ground plane under the RF connector part on the top layer . other layers should have ground plane under it

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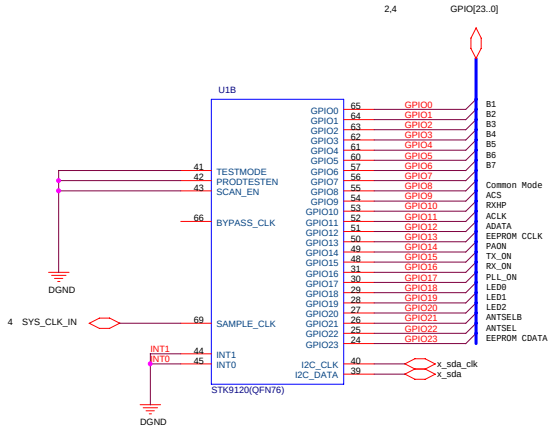
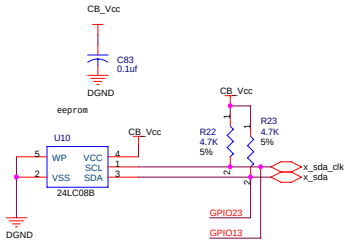


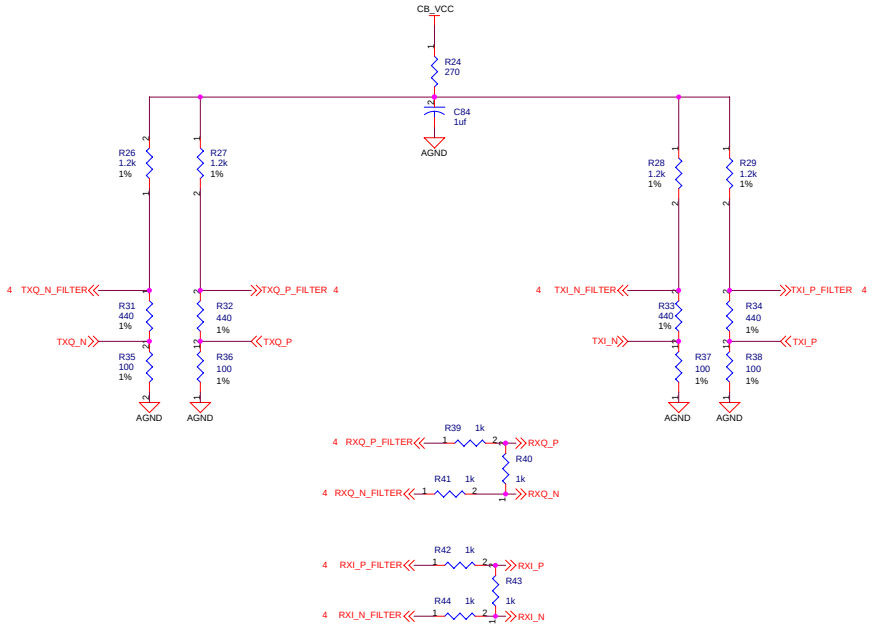
Note: GPIO23 If this GPIO is used as an ouptut the PLL_CLKO will be enabled. No effect is used as an Input

DSP Config and GPIOs

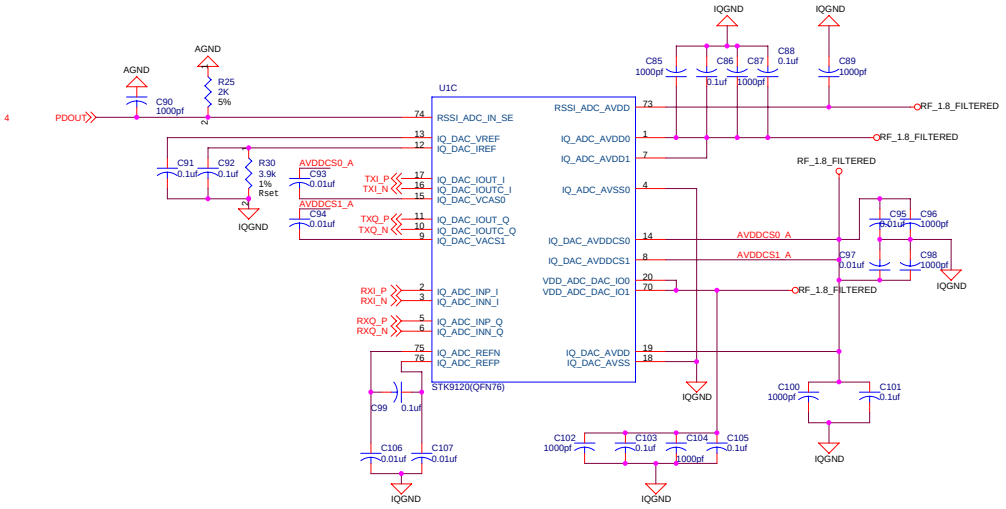


EEPROM

TX/RX RFI



IQ DAC, IQ ADC, RSSI ADC



Title	GPIO		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Friday, January 08, 2010		Sheet 5 of 5	