3DSP-WLAN + SYNTEK RF(STK9230) PCI

Version A

SYNTEK SEMICONDUCTOR Corporation

********** NOTICE **********
These are schematics of a design example which is under development.
SYNTEKSEMICONDUCTOR Corp. assumes no responsibility for the content and makes
no commitment to update any of the information herein.
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03	BUS	PCI interface
04	Power	The power supply part
05	RF Interface	The Airoha Transceiver & PA & Antenna
06	GPIO	The digital interface between DSP & RF & other parts

Title: Cover Page
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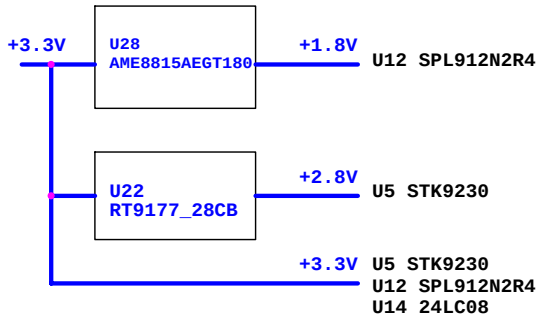

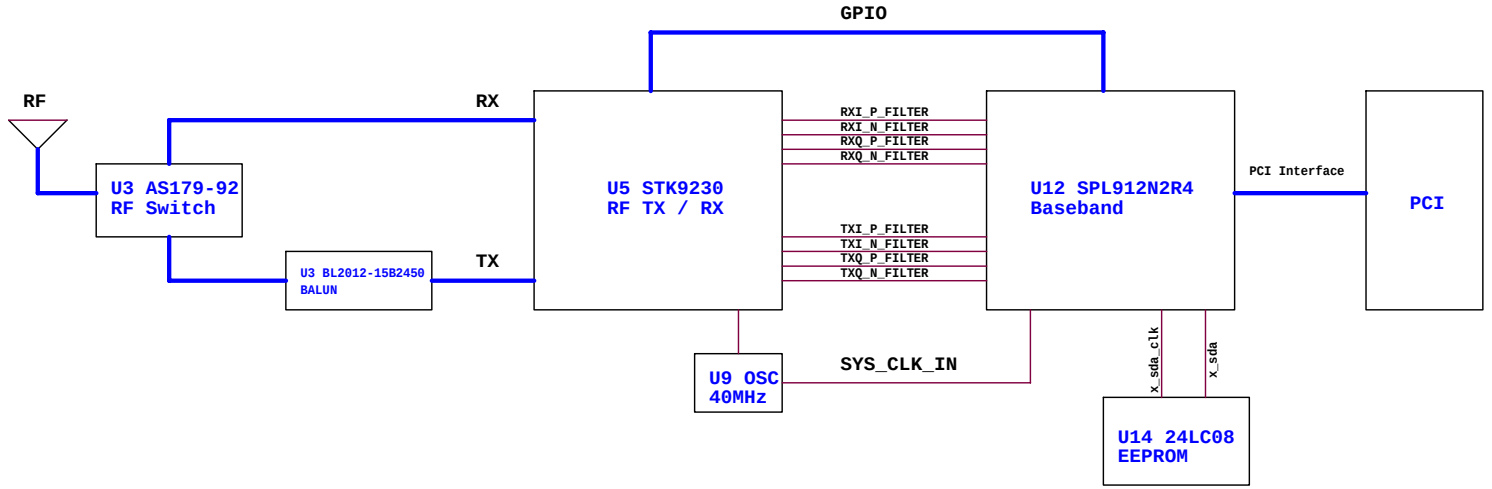

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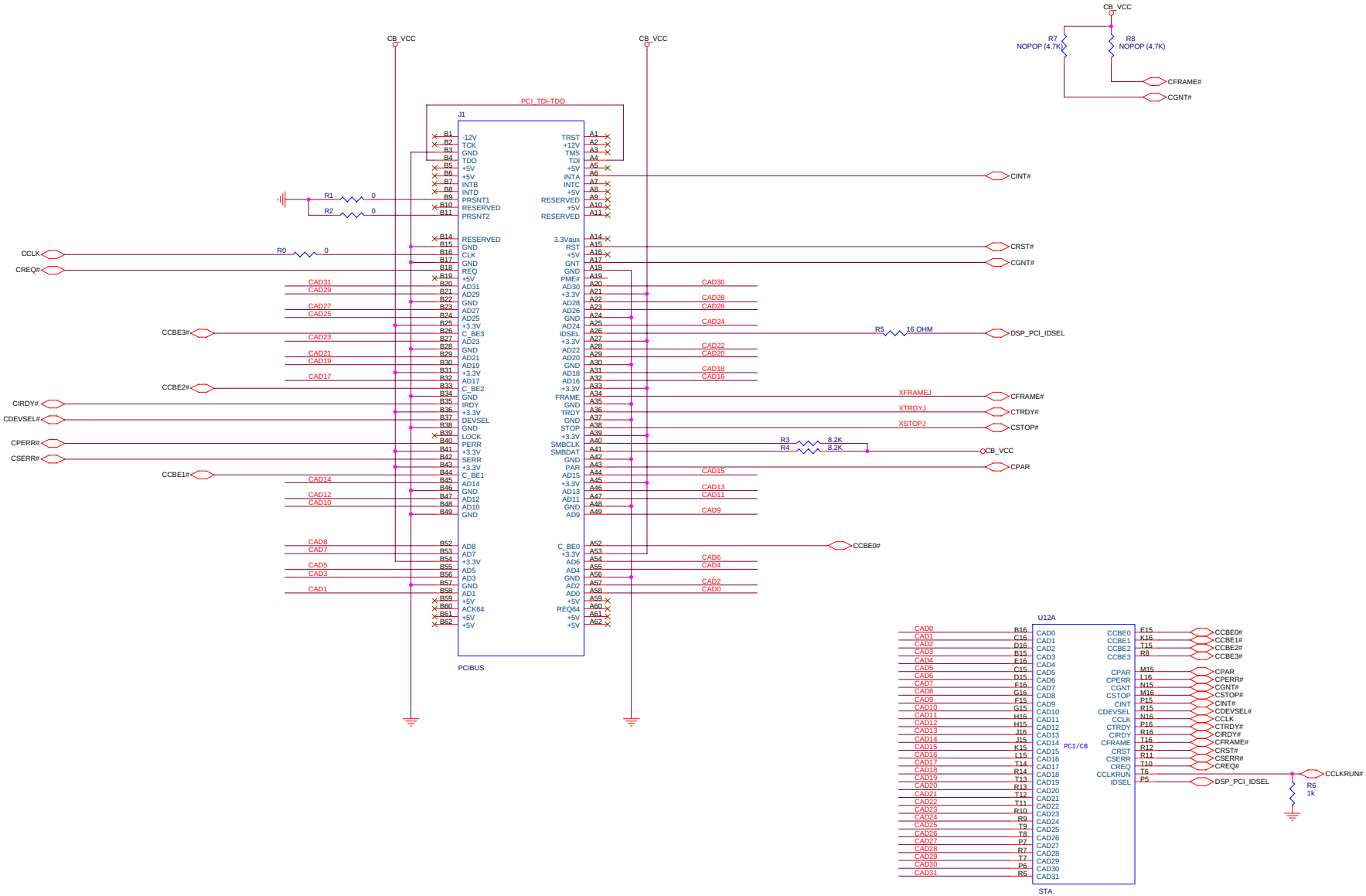

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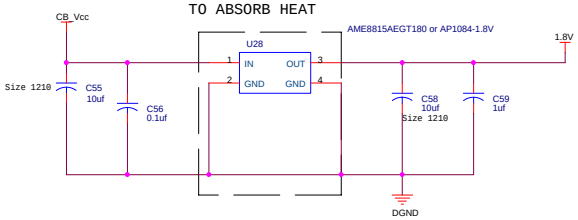
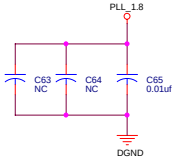
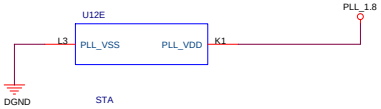
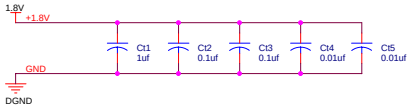
PUT A LOT OF COPPER ARROUND
TO ABSORB HEAT

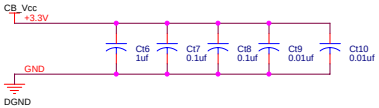




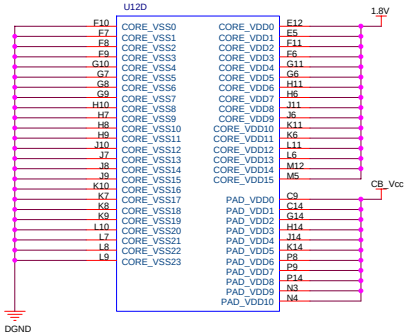


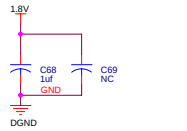


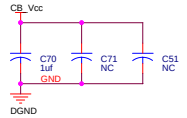
These need to be placed close to power pins
These ones should be on top



Chip may draw up to 1.5A @ 2.0V

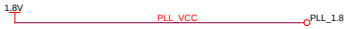






Thick trace to handle 10mA @ 2.0V

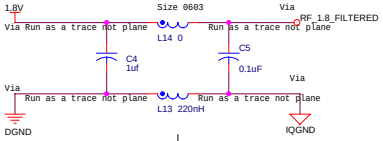
Run as a trace not plane



The traces should run through the Caps

Run as a trace not plane

Thick trace to handle .3A @ 2.0V

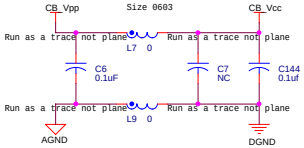


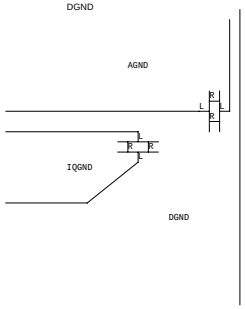
Place between Digital and RF power sections on the board

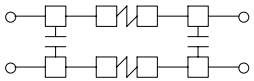
Run as a trace not plane

Thick traces to handle 1A at 3.3V

The traces should run through the Caps

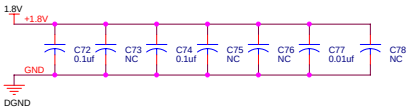




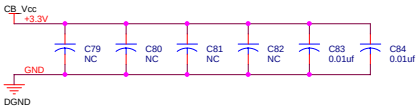


STA

These need to be placed close to power pins



These need to be placed close to power pins



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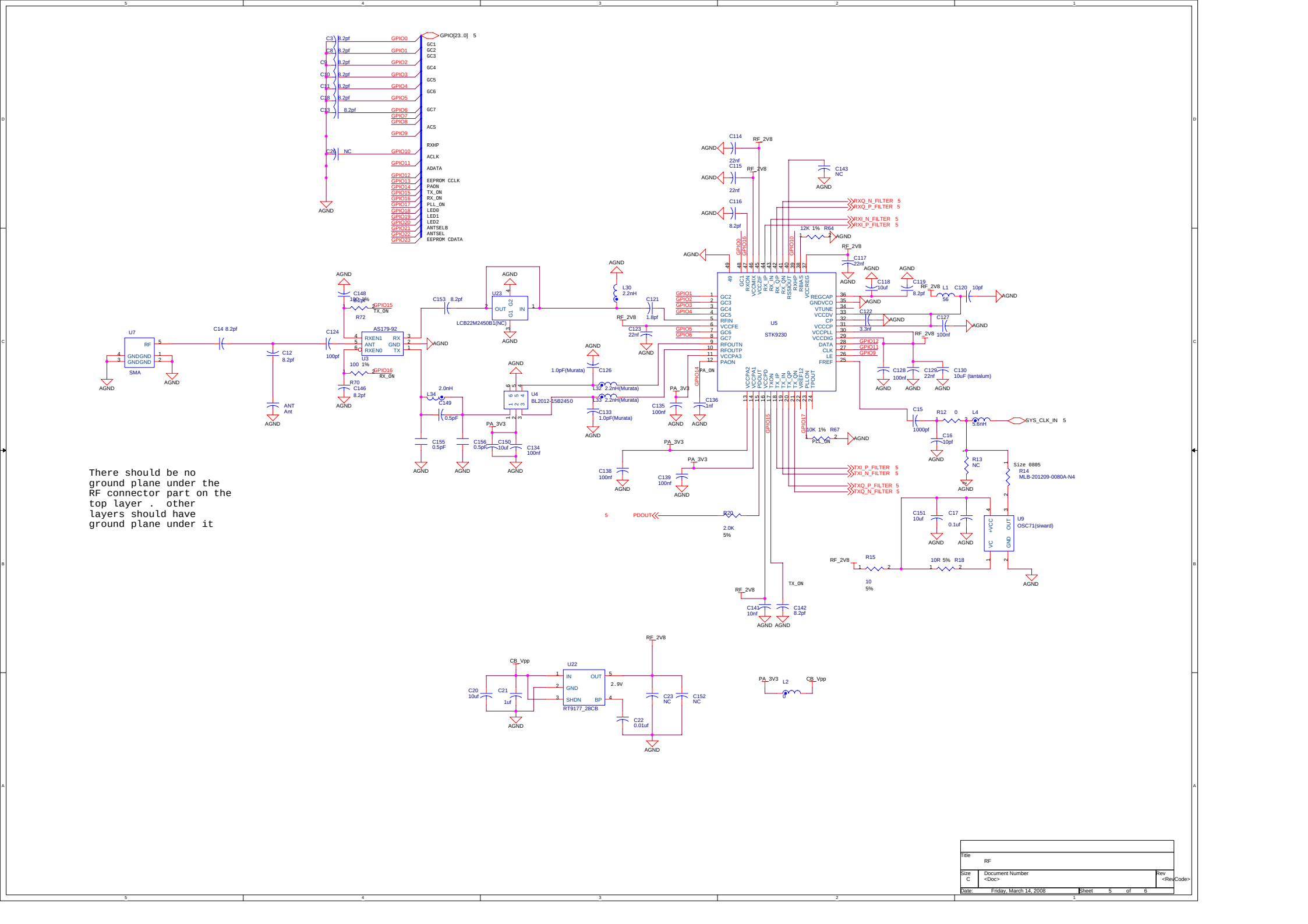

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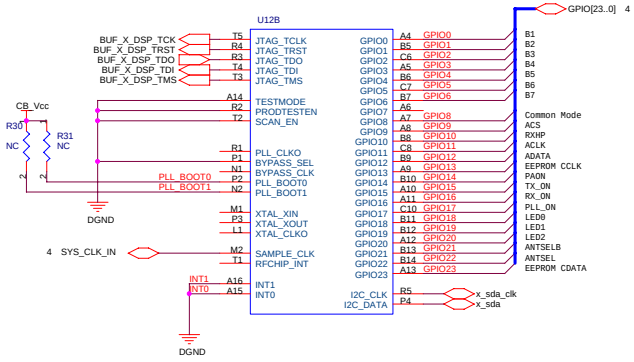
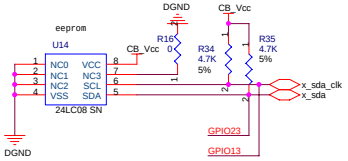
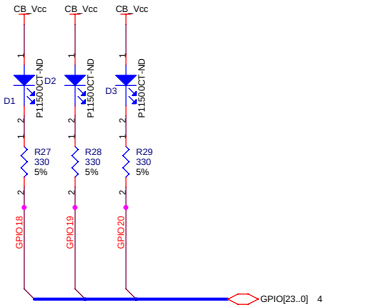


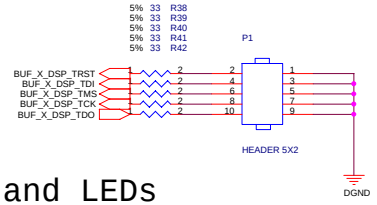
STA

Note: GPIO23 If this GPIO is used as an ouptut the PLL_CLKO will be enabled. No effect is used as an Input

DSP Config and GPIOs



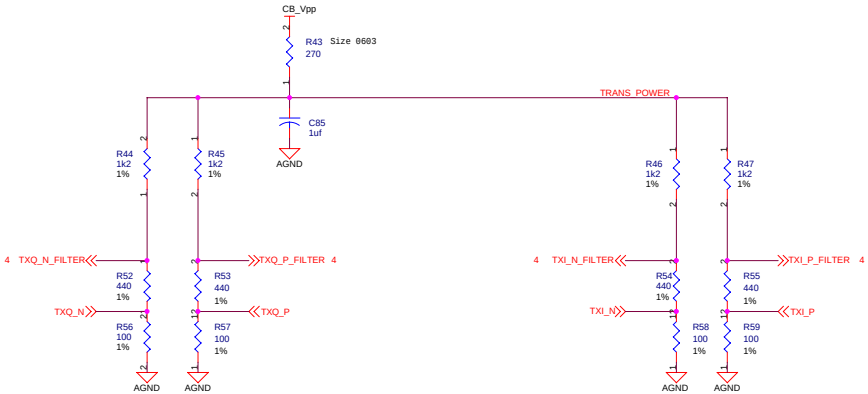


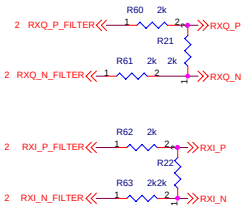


Cardbus Connection and EEPROM

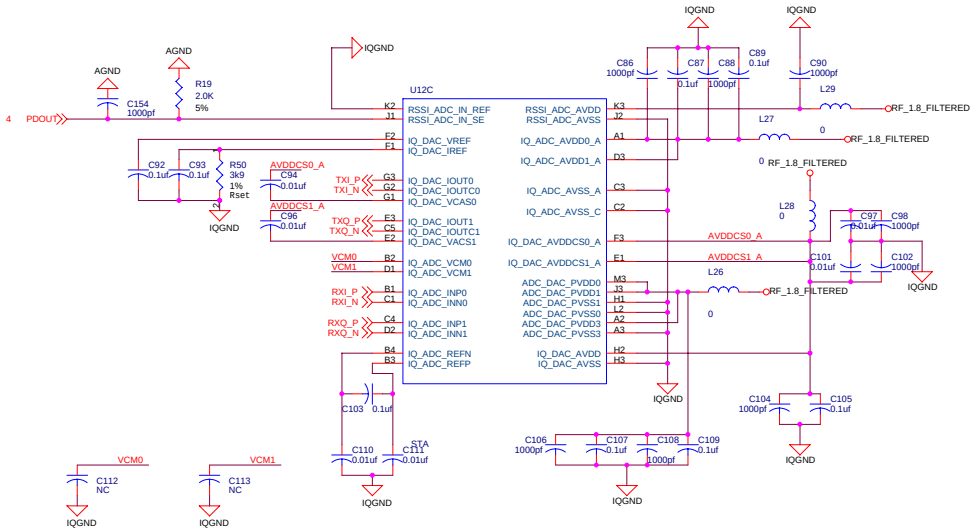
JTAG and LEDs

TX/RX RFI





IQ DAC, IQ ADC, RSSI ADC



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