

D

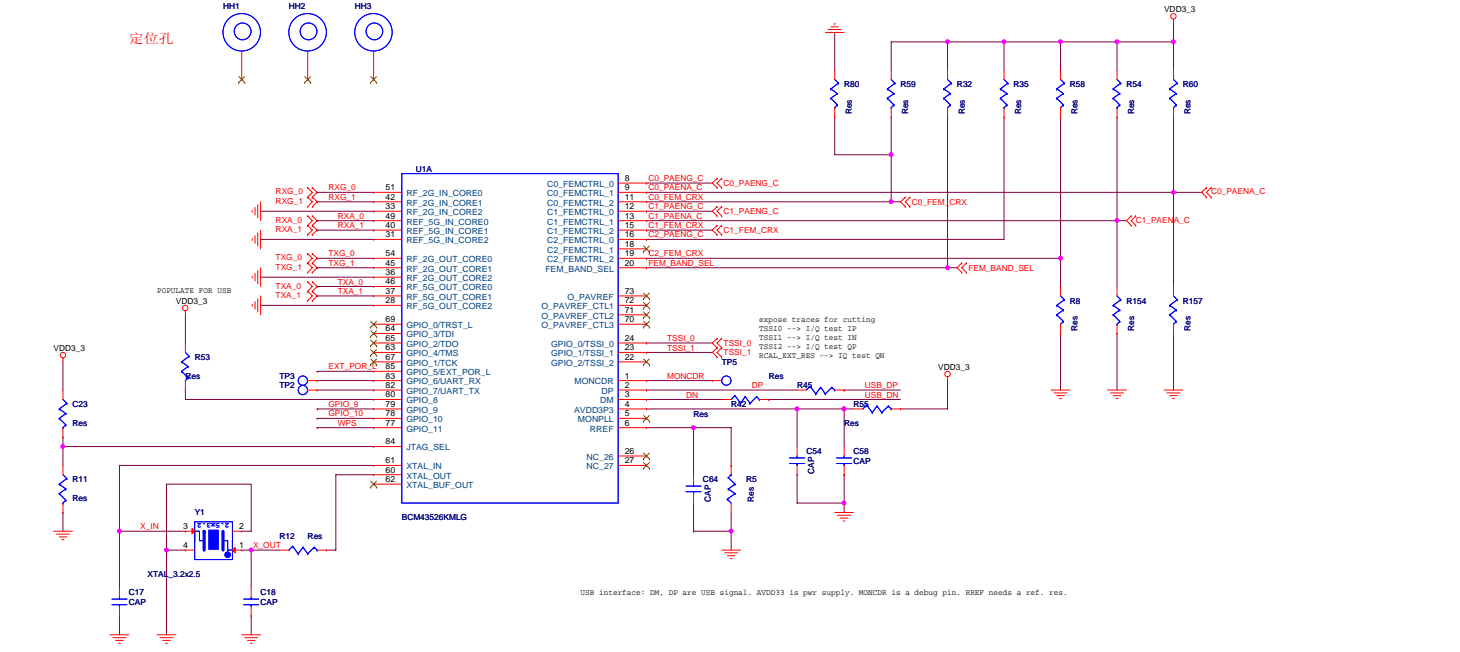
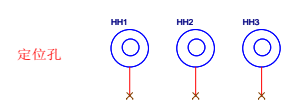
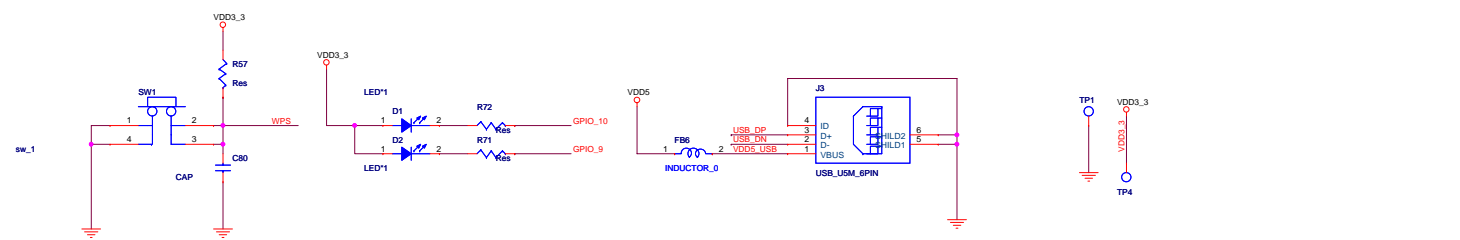
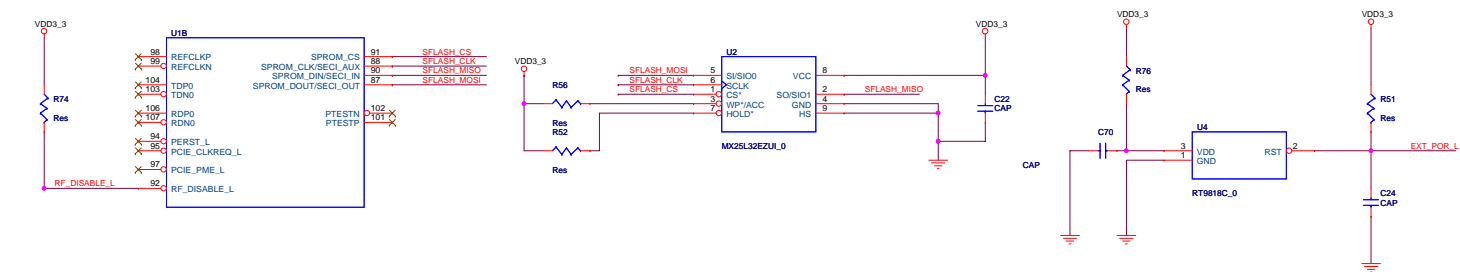
C

B

A

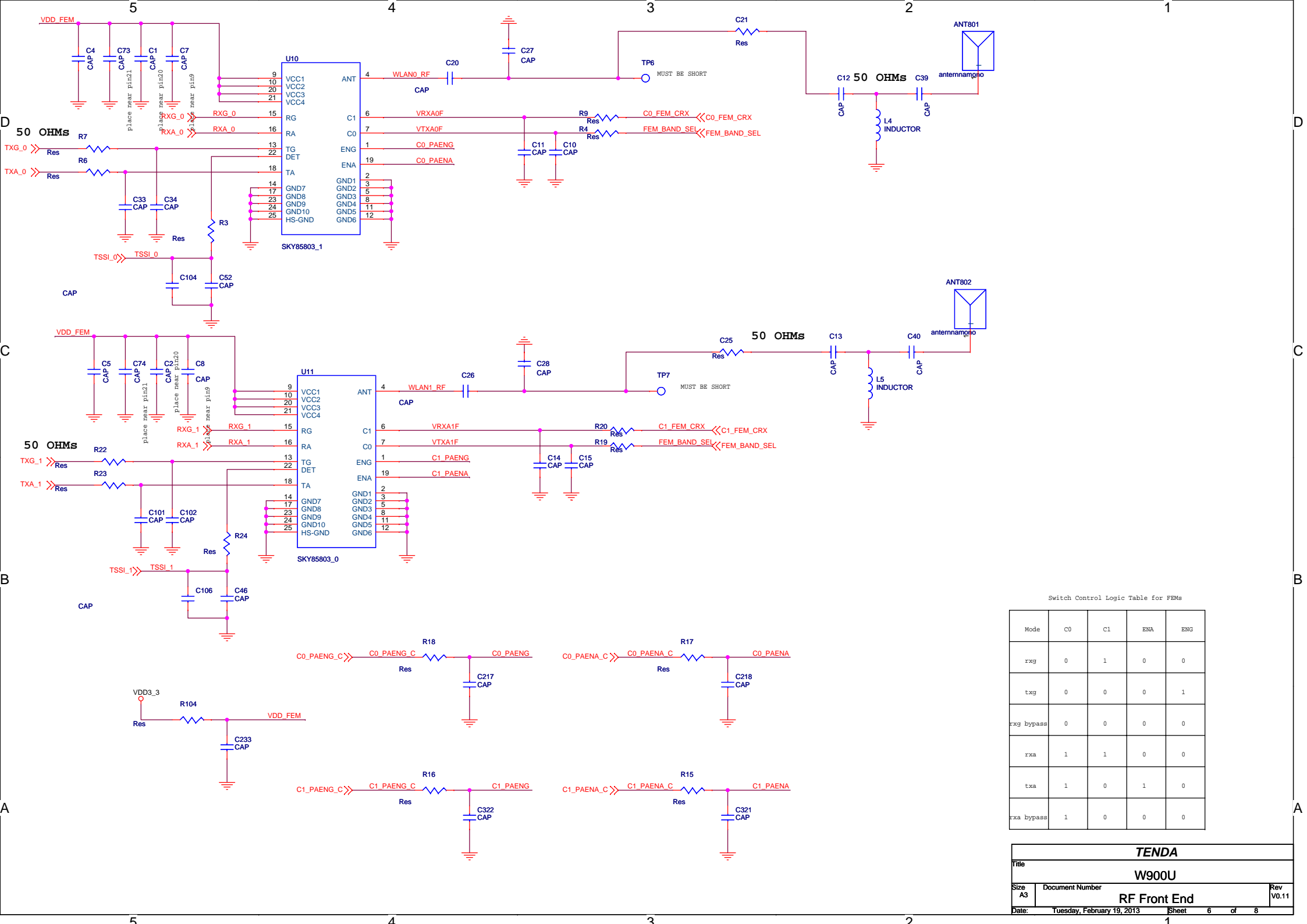
**Product Name: W900U**  
**Trade Name: Tenda**

<b>TENDA</b>		
Title		
W900U		
Size	Document Number	Rev
A4	Cover Page	V0.11
Date:	Monday, November 19, 2012	Sheet 1 of 8



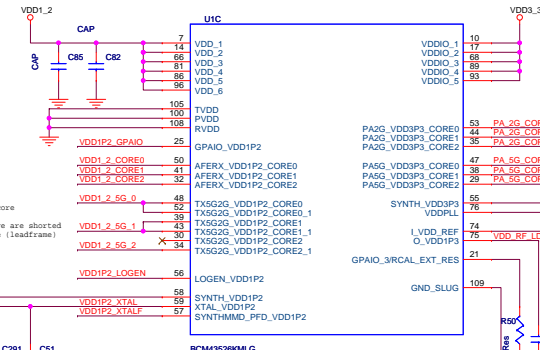
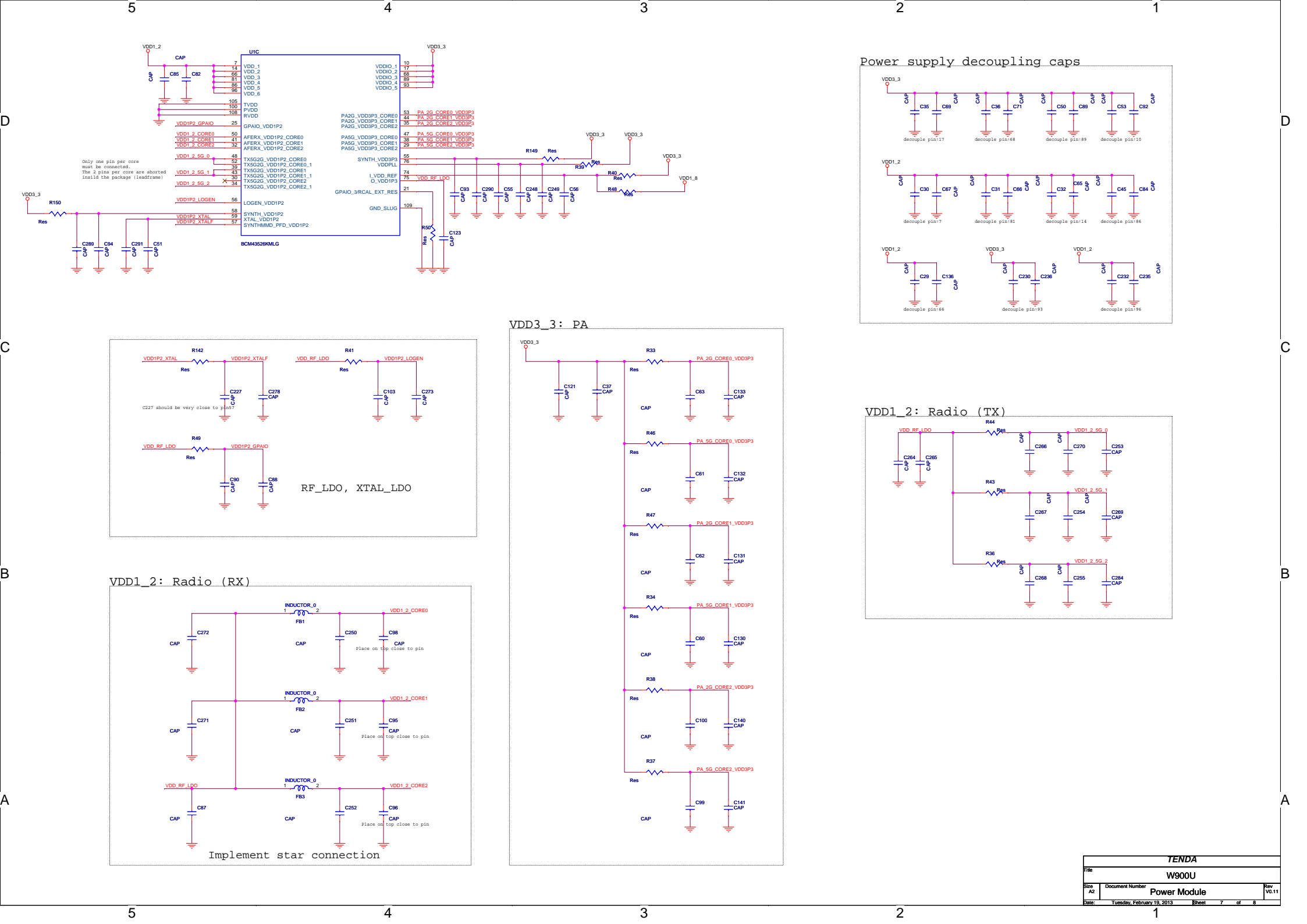
Pin	chip default	board default	description
CO_FEMCTRL_1	1	1	0: 20MHz XTAL selected 1: 40MHz XTAL selected
C1_FEMCTRL_0, CO_FEMCTRL_2	0,1	0,1	0,1: 4K SRAM size 1,0: 16K SRAM size
C1_FEMCTRL_1	1	1	0: Boot from SRAM 1: Boot from ROM
C2_FEMCTRL_0	0	1	0: don't query OTP 1: query OTP
C2_FEMCTRL_2	1	0	0: SRAM not present (ATMEL if SFLASH is present) 1: SRAM present (ST if SFLASH is present)
BANDSEL	0	0	0: SFLASH not present 1: SFLASH present
gpio[7,6]	1,1	1,1	PCIe: see Twiki
gpio8	0	1	1: USB 2.0 enable, PCIe disable (only in 12x12 package) 0: USB 2.0 disable, PCIe enable (only in 12x12 package)

For B0, R8 need to depopulate for HT available  
R80 need to populate for sflash not present

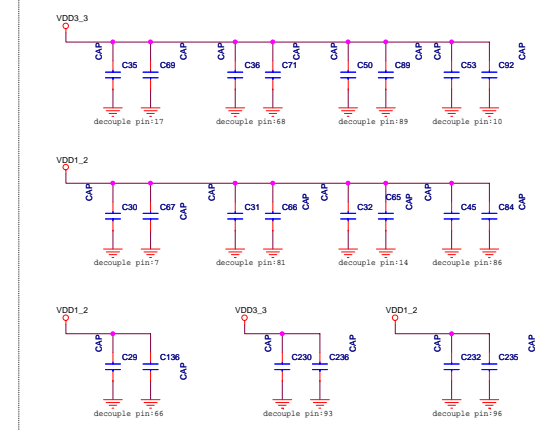


Switch Control Logic Table for FEMs

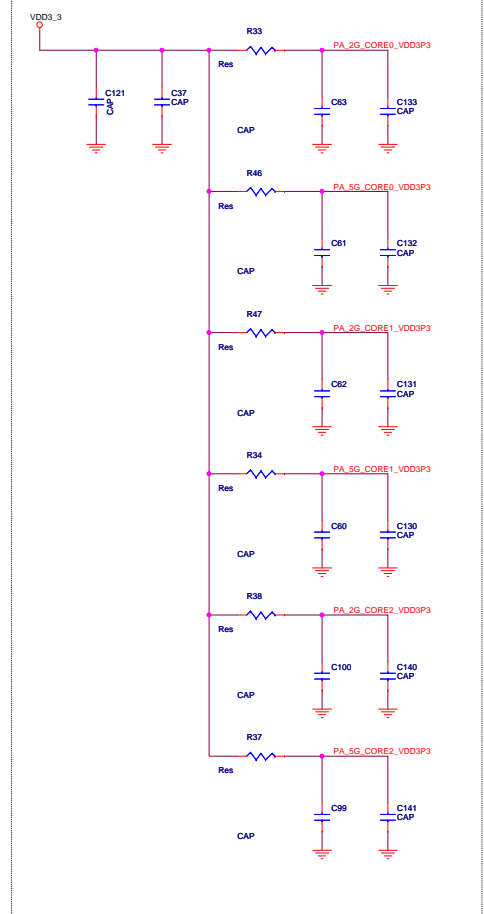
Mode	C0	C1	ENA	ENG
rxg	0	1	0	0
txg	0	0	0	1
rxg bypass	0	0	0	0
rxg	1	1	0	0
txg	1	0	1	0
txg bypass	1	0	0	0



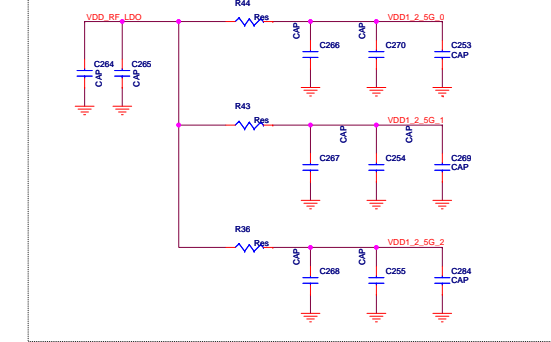
Power supply decoupling caps



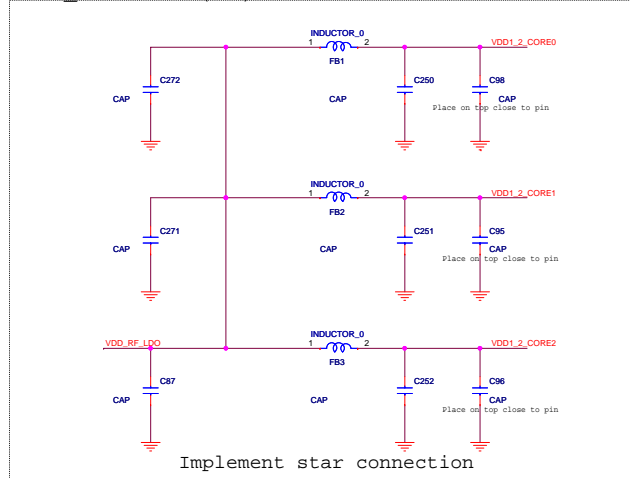
VDD3\_3: PA



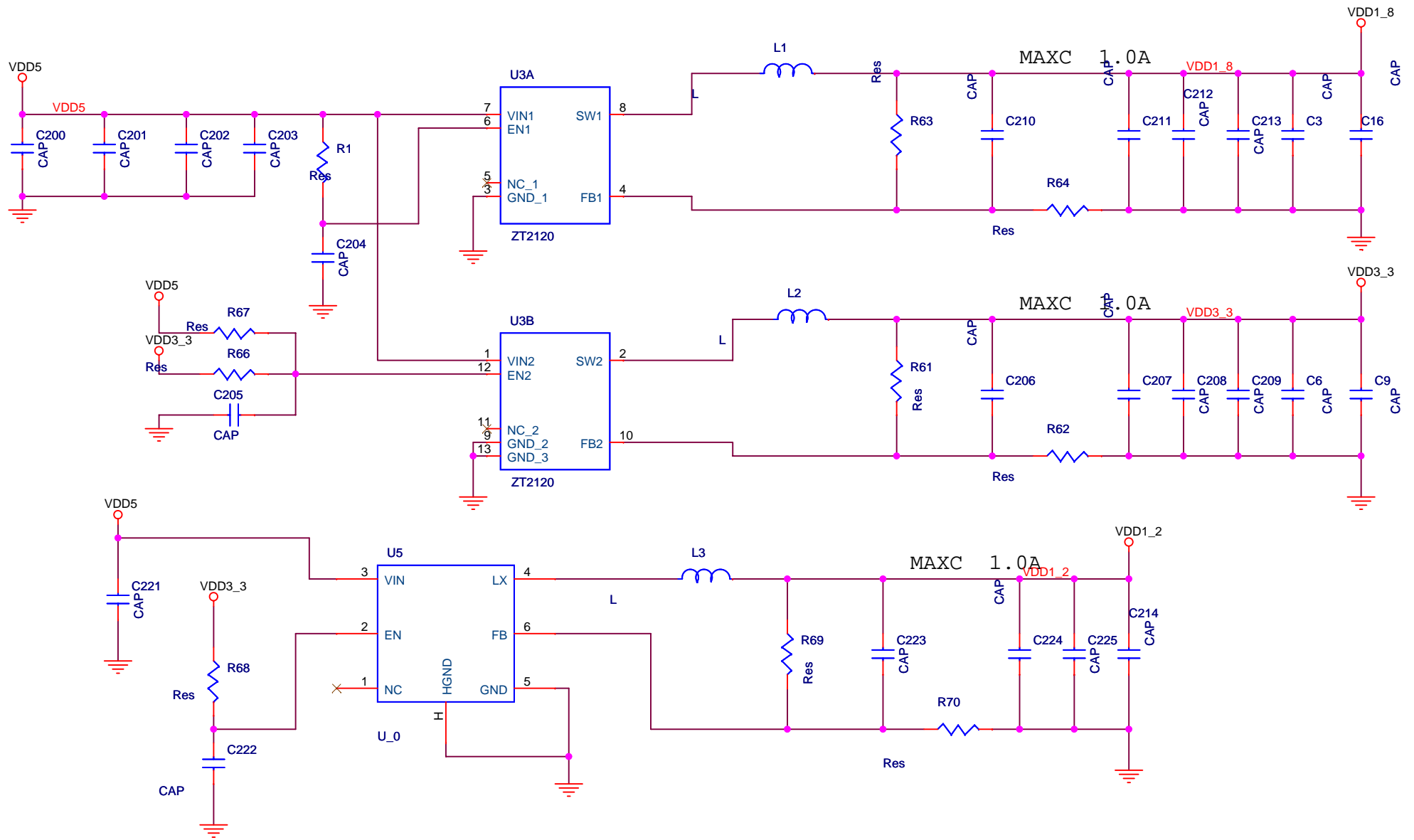
VDD1\_2: Radio (TX)



VDD1\_2: Radio (RX)



<b>TENDA</b>			
File	W900U		
Size	Document Number	Rev	
A2	Power Module	V0.11	
Date:	Tuesday, February 19, 2013	Sheet	7 of 8



power sequence 5V -> 3.3-> 1.2

<b>TENDA</b>		
Title		
W900U		
Size A4	Document Number	Rev V0.11
<b>Power Supply</b>		
Date:	Tuesday, February 19, 2013	Sheet 8 of 8