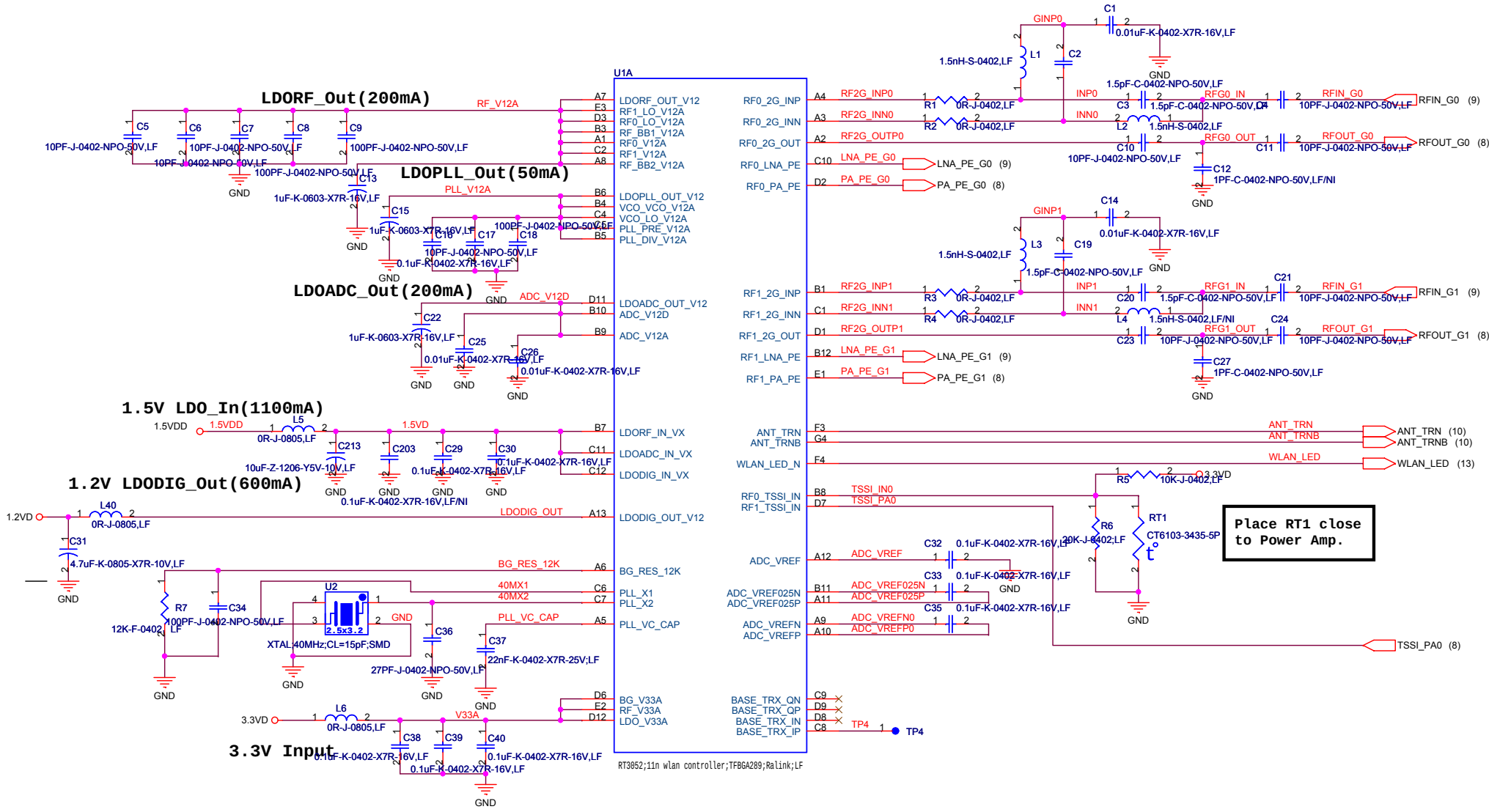

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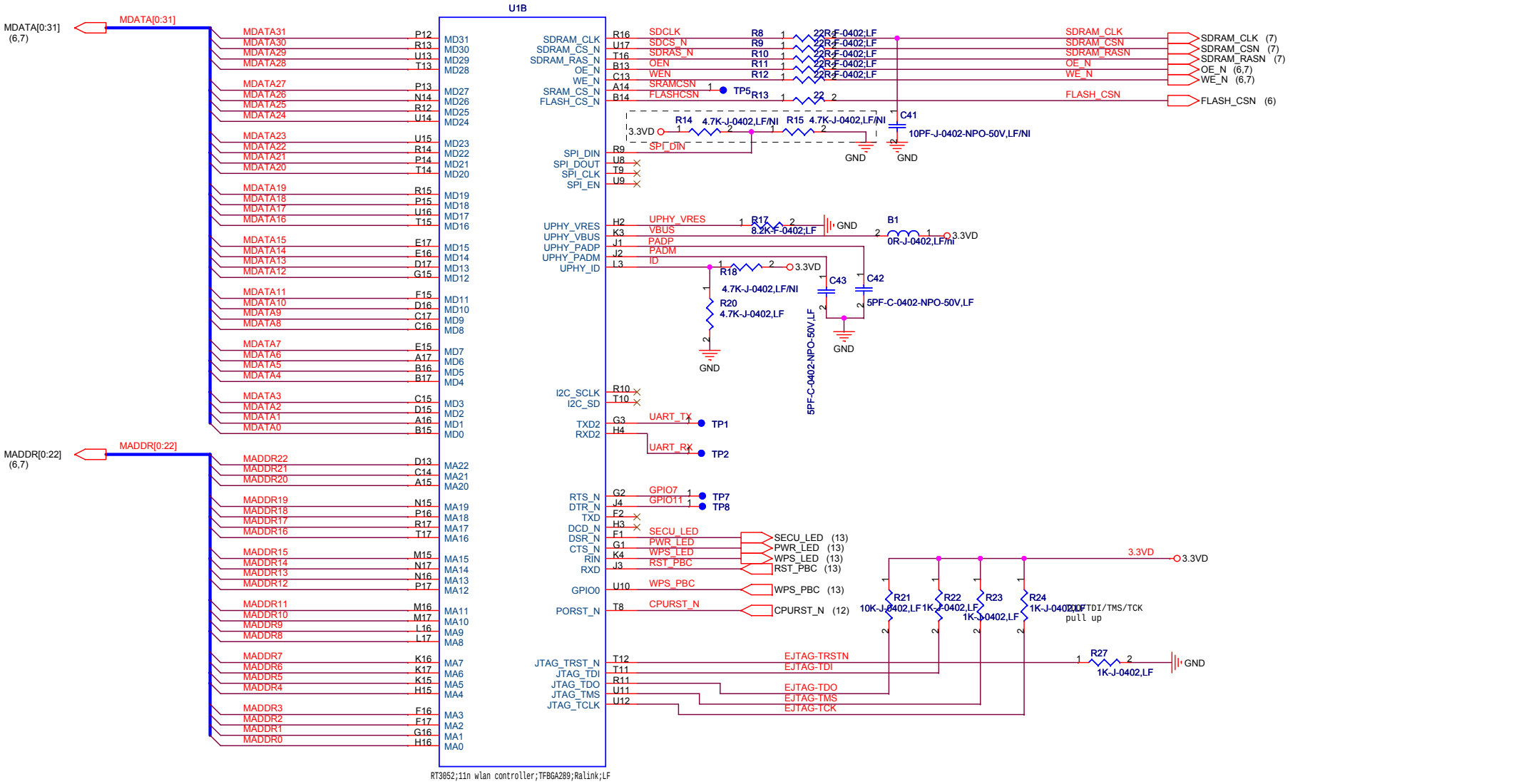
Size B	Document Number 11-RT3052-RF-A.SCH	Rev 0.1
Date: Thursday, June 18, 2009	Sheet 2 of 14	



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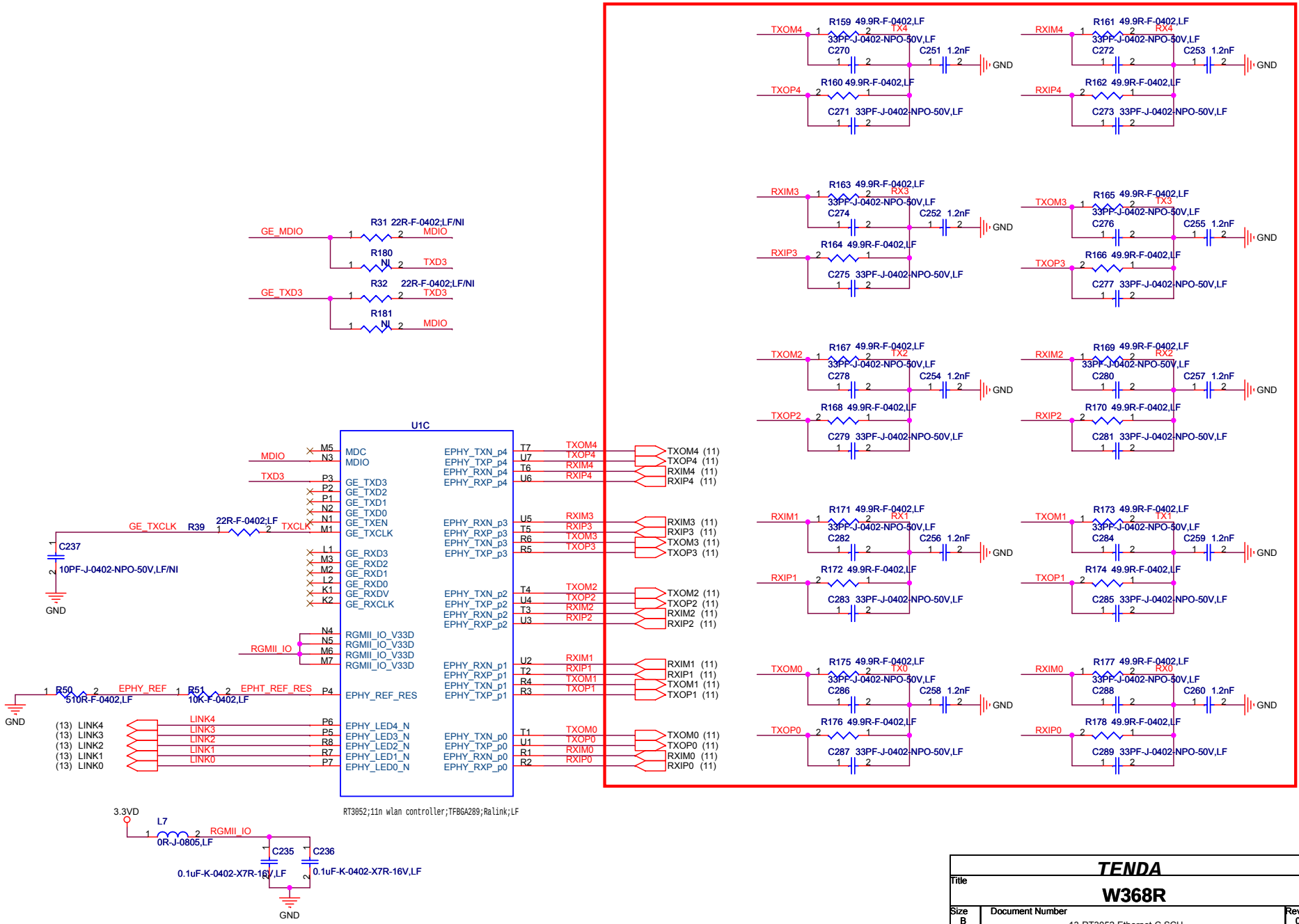
Date: Thursday, June 18, 2009	Sheet 3 of 14	



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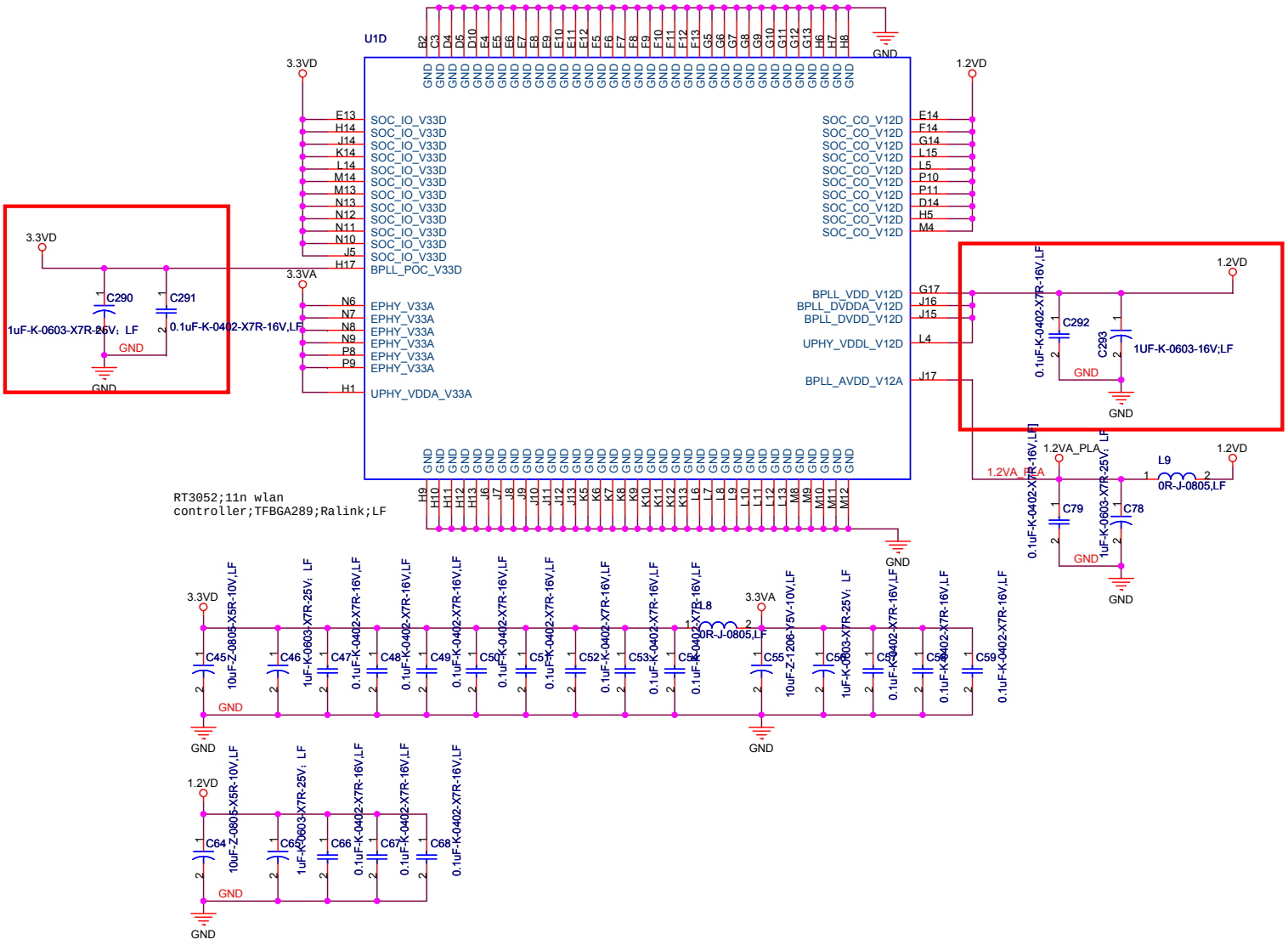
Date: Thursday, June 18, 2009	Sheet 4 of 14	



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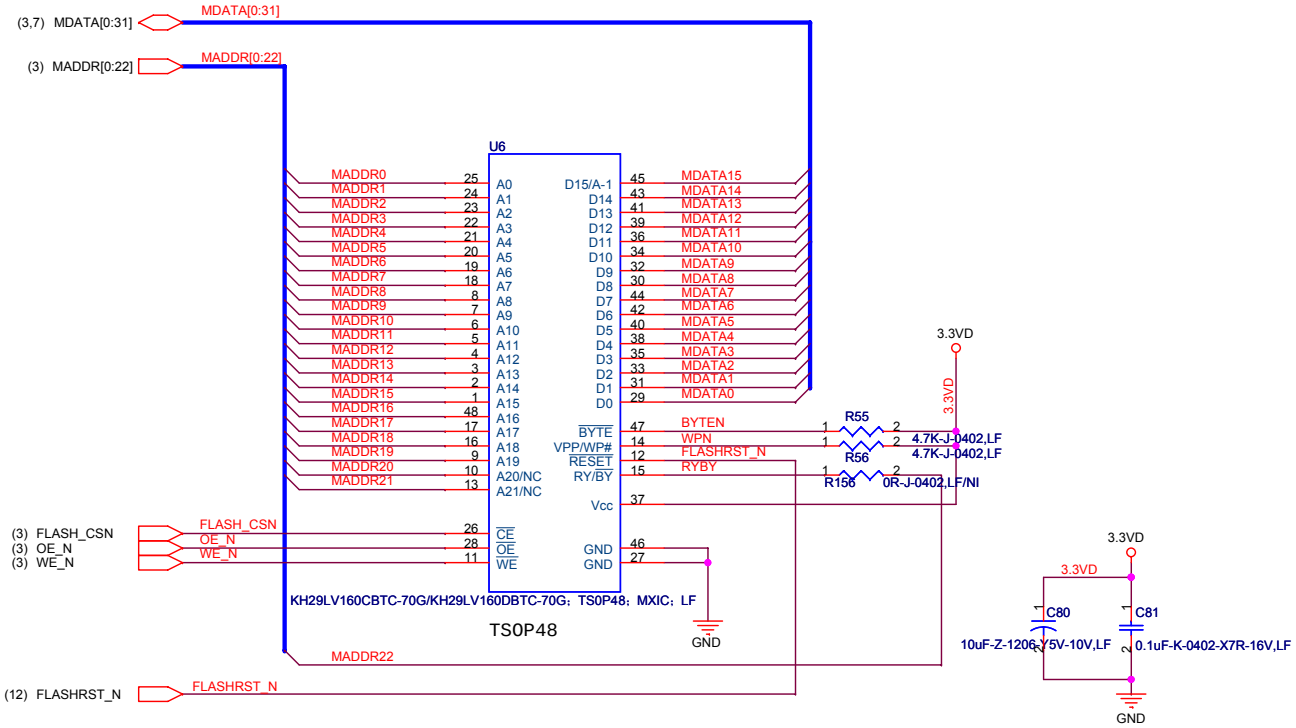
Date: Thursday, June 18, 2009	Sheet 5 of 14	



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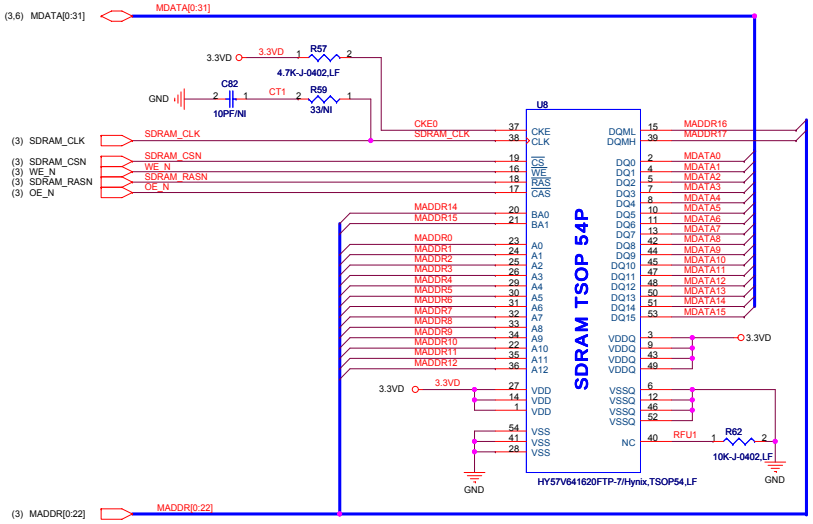
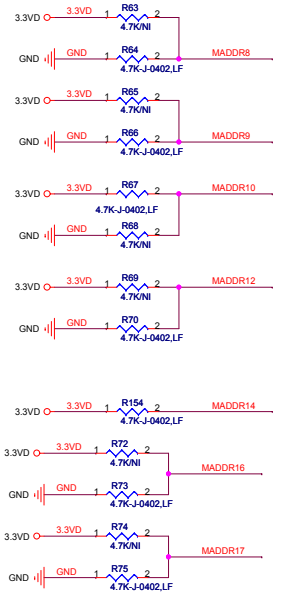
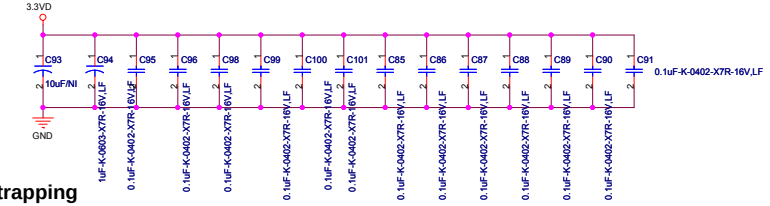
Size B	Document Number 21-FALSH.SCH	Rev 0.1
Date: Thursday, June 18, 2009	Sheet 6 of 14	







Boot Up Strapping

Pin Name	Description	Value=0	Value=1
MA[9:8]	BOOT FROM	00 : 16bit flash* 01 : 8bit flash 10 : NAND Flash 11: Internal ROM	
MA10	CPU CLK SEL	320Mhz	384Mhz*
MA12	BIG ENDIAN	Little*	Big
MA13	Bypass PLL	Not Bypass*	Bypass
MA14	Boot Addr	0x1FC00000*	0x1F000000
MA15	Reserved		
MA[17:16]	GE MODE	Gagabit Port Mode 00 : RGMII (10/100/1000M bps)* 01 : MII(10/100M bps) 10 : Reversed MII(10/100M bps) 11 : Reversed	
MA18	Reserved		
MA19	Reserved		
MA20	iNIC SDRAM	2MB*	8MB
MA21	iNIC Config	NA	EEPROM /MA20

TENDA

Title: W368R

Size: C | Document Number: 22-SDRAM-CFG.SCH | Rev: 0.1

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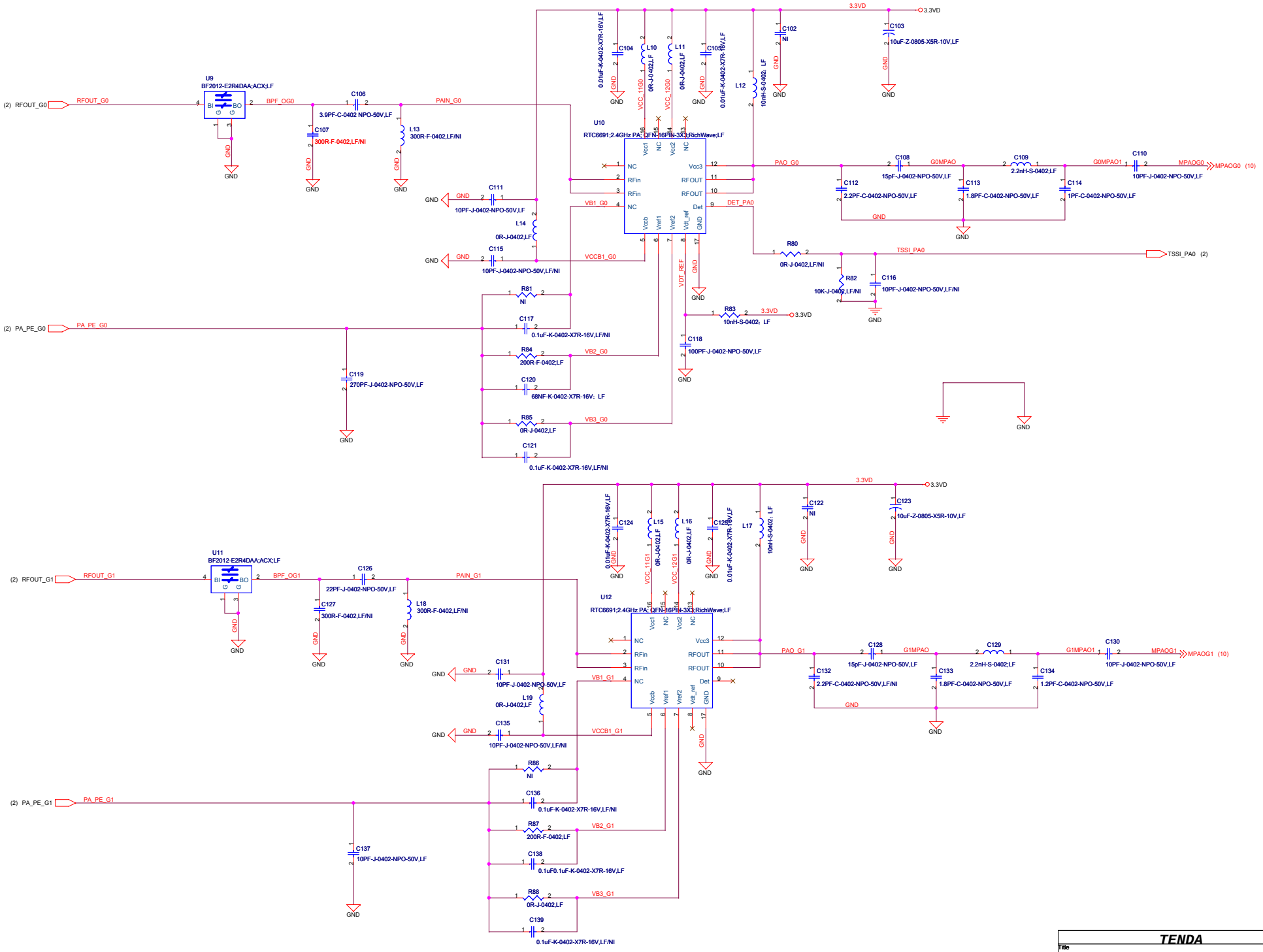

TENDA		
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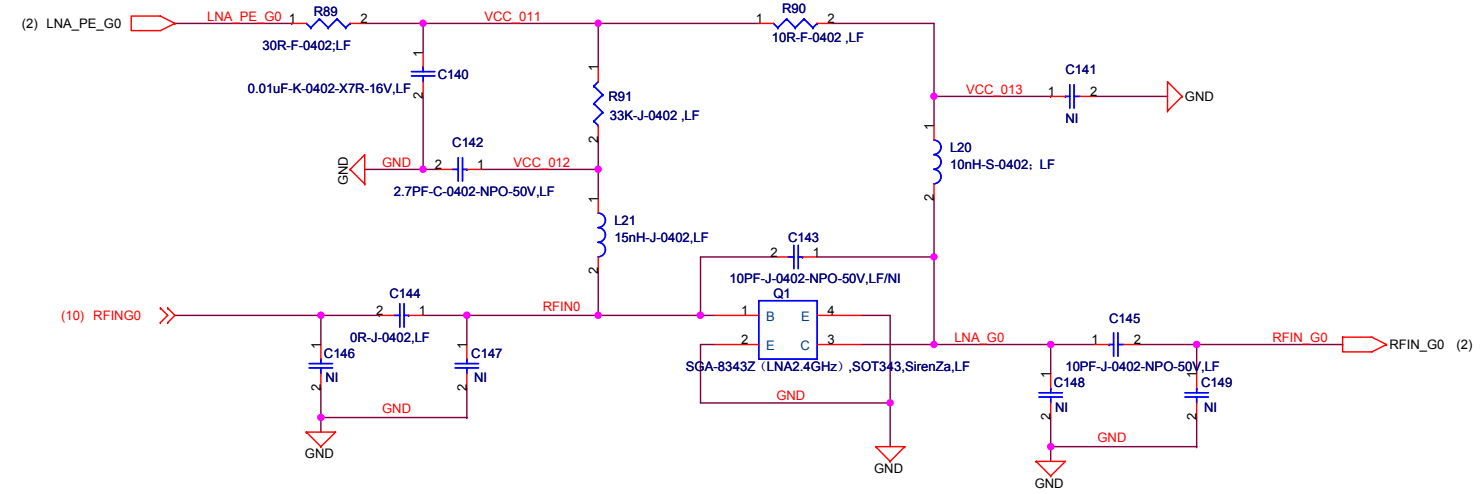
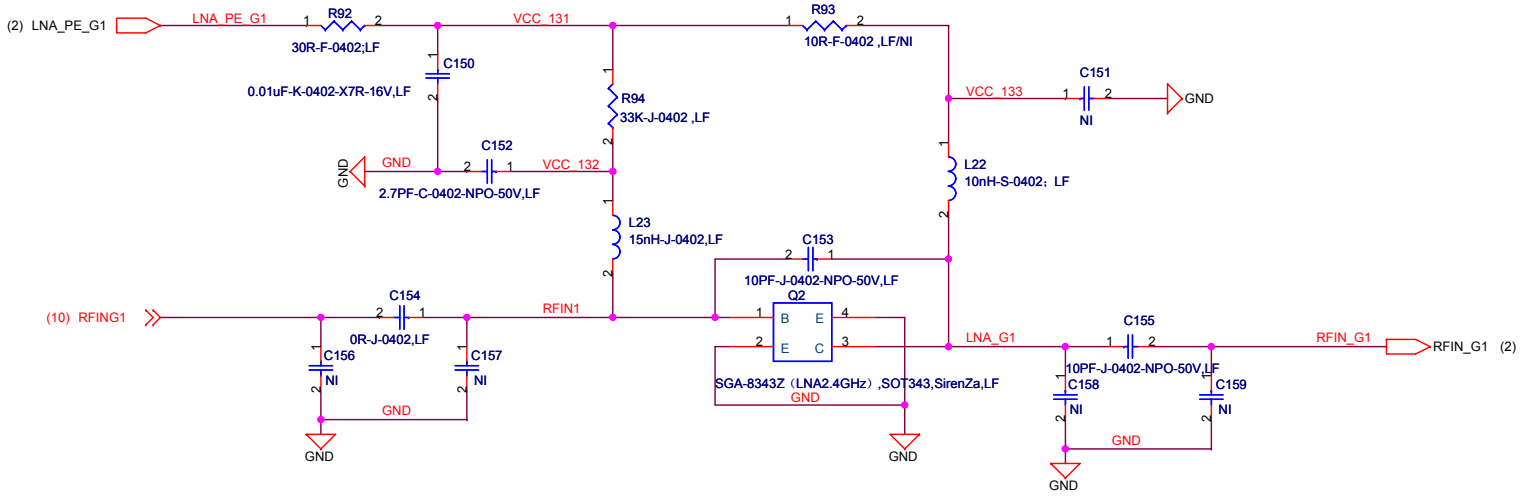
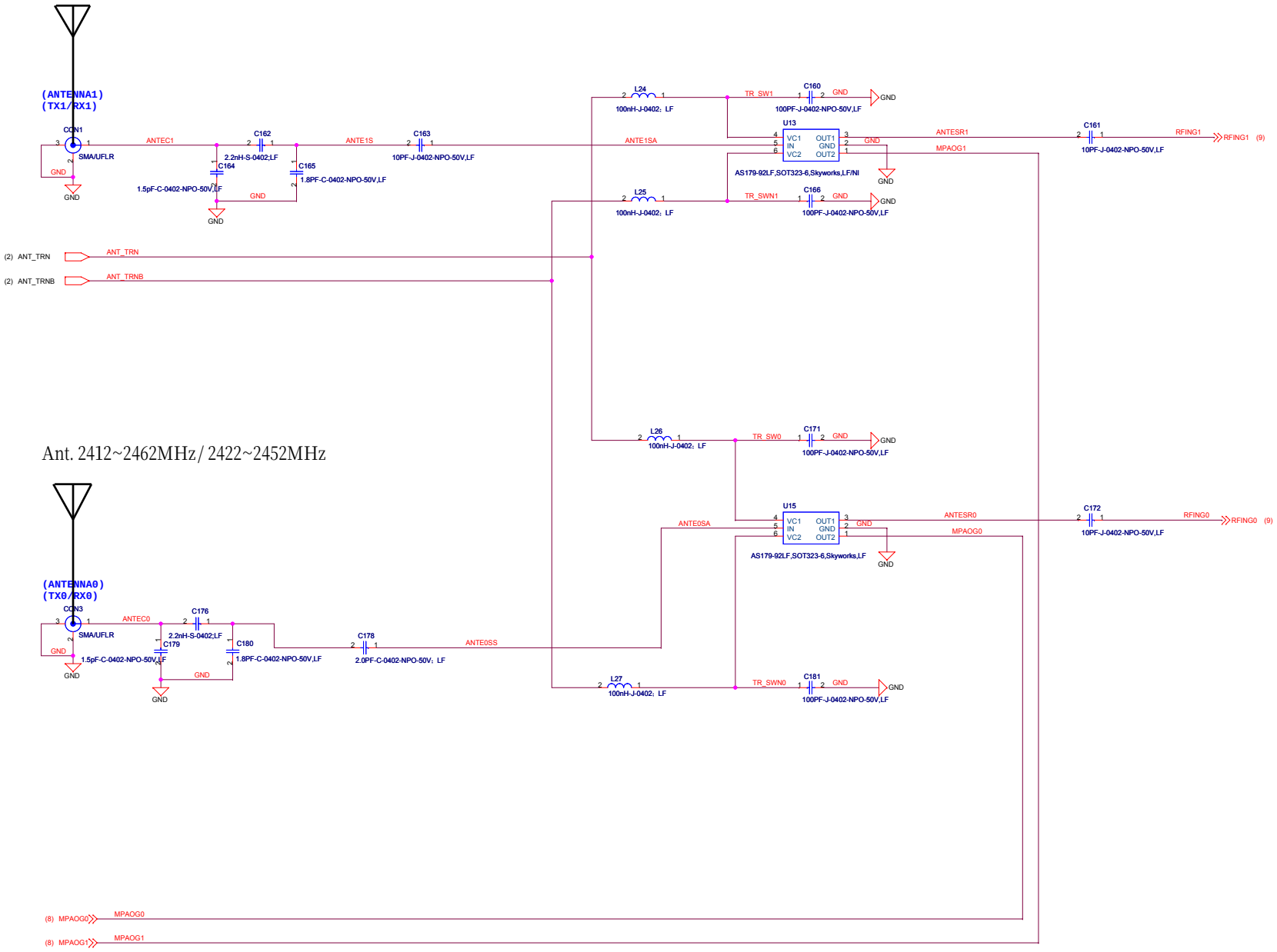
Size: C	Document Number: 31-PA-RW.SCH	Rev: 0.1
Date: Thursday, June 18, 2009	Sheet 8 of 14	





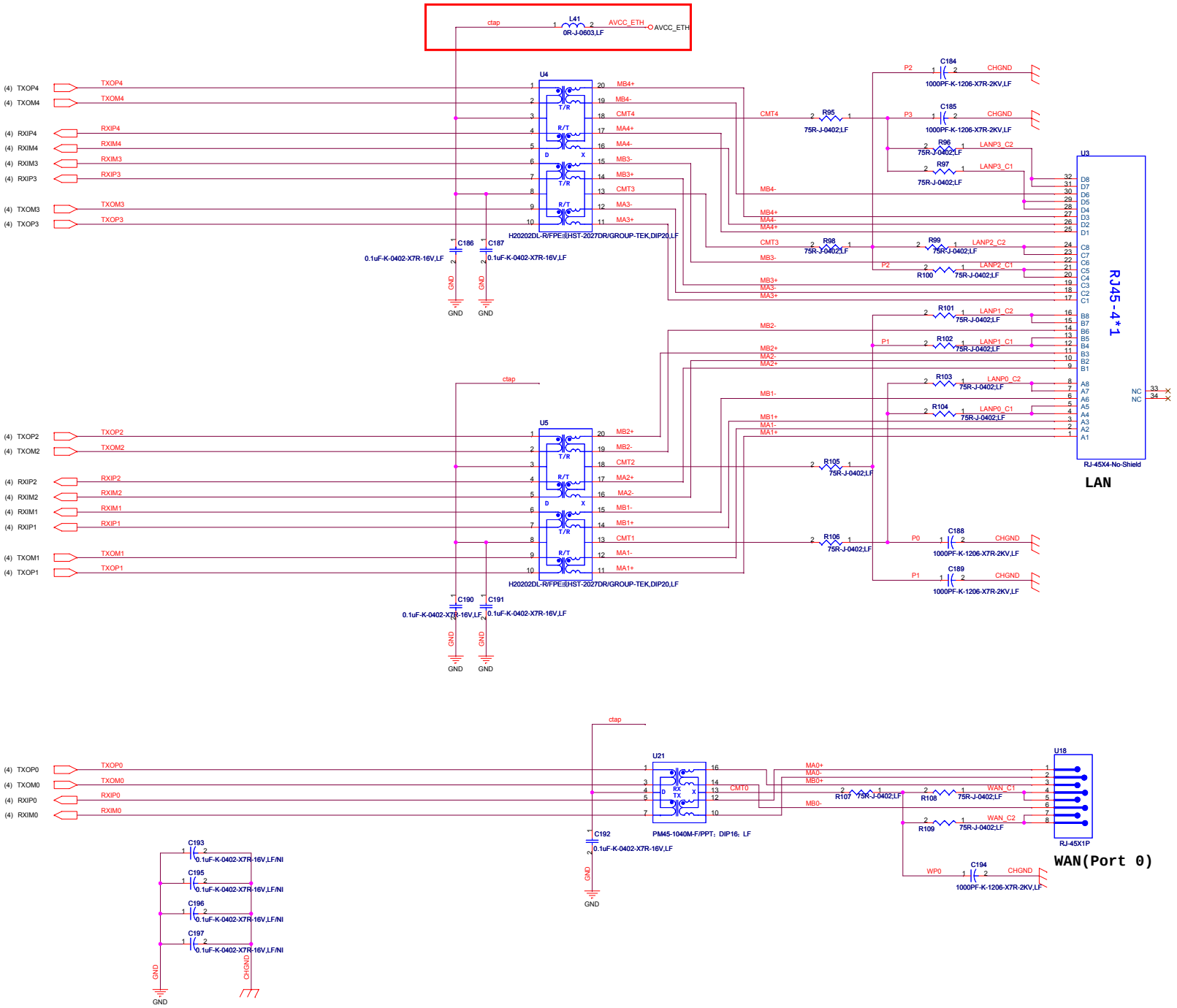
TENDA		
Title	W368R	
Size B	Document Number 32-LNA.SCH	Rev 0.1
Date: Thursday, June 18, 2009	Sheet 9 of 14	

Ant. 2412~2462MHz/ 2422~2452MHz



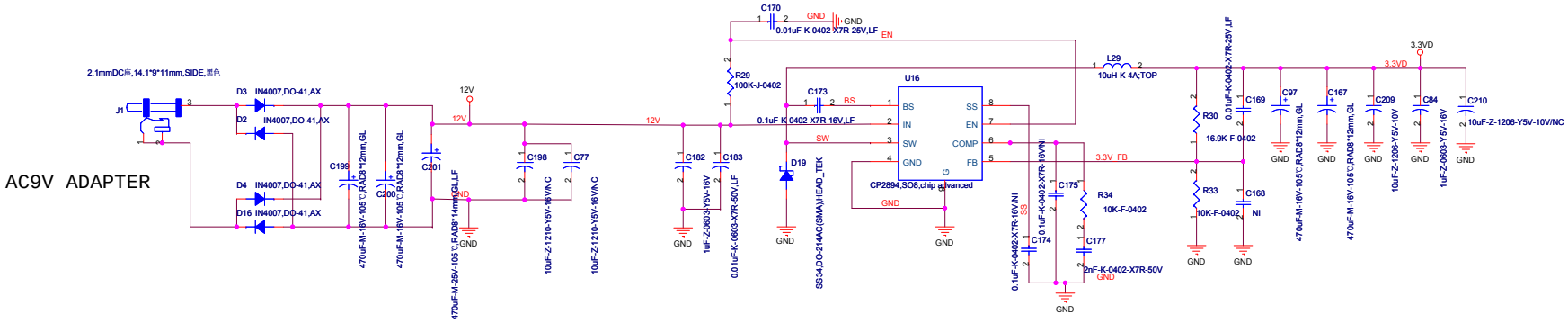
Ant. 2412~2462MHz/ 2422~2452MHz

Title	TENDA W368R	
Size C	Document Number 33-Front End.SCH	Rev 0.1
Date: Thursday, June 18, 2009	Sheet 10 of 14	

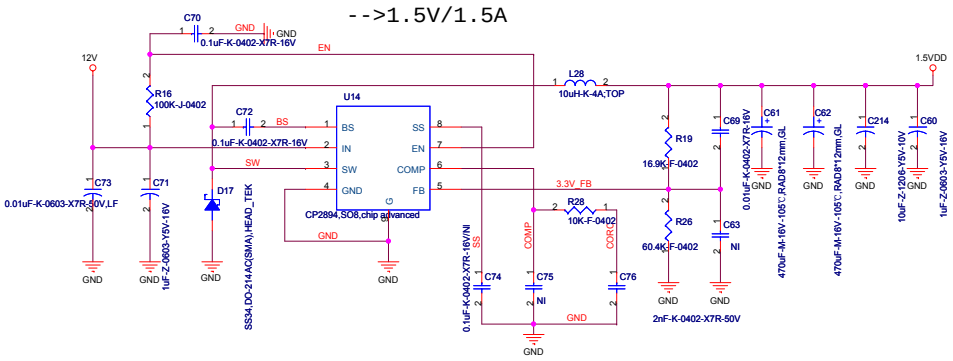


TENDA			
Title	W368R		
Size C	Document Number 4-XMER-RJ45.SCH		Rev 0.1
Date: Thursday, June 18, 2009	Sheet 11 of 14		

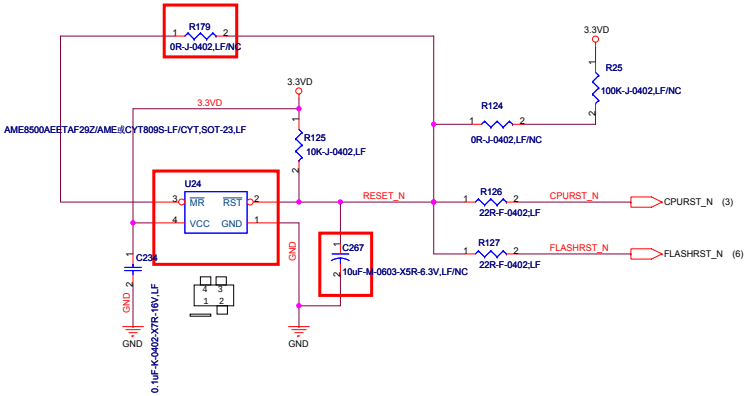
-->3.3V/1.5A

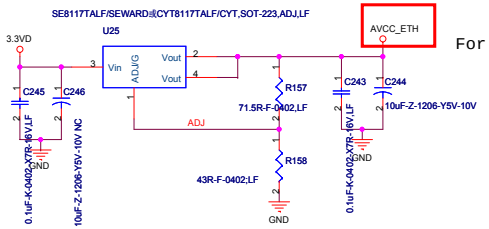


-->1.5V/1.5A



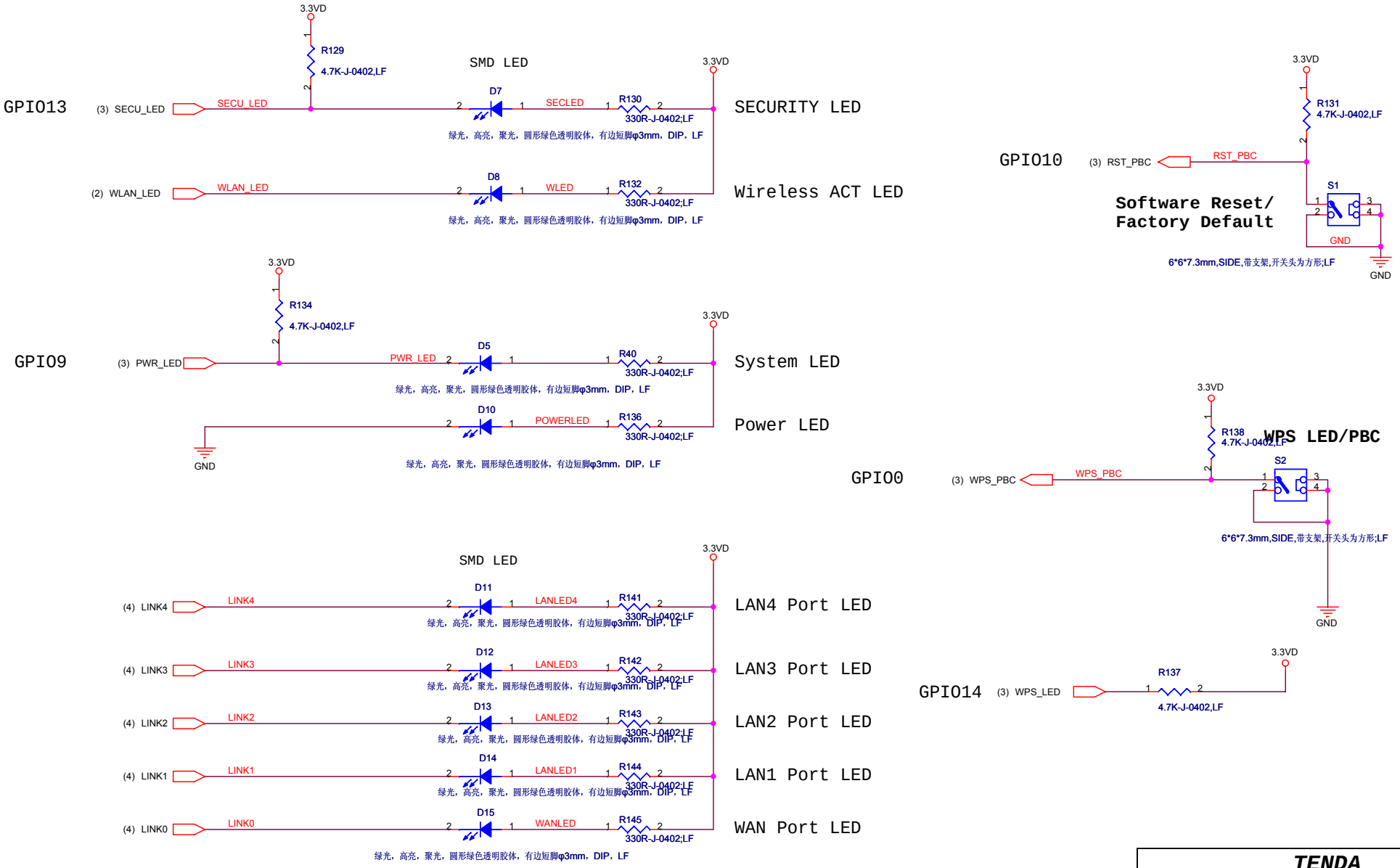
Reset Circuit



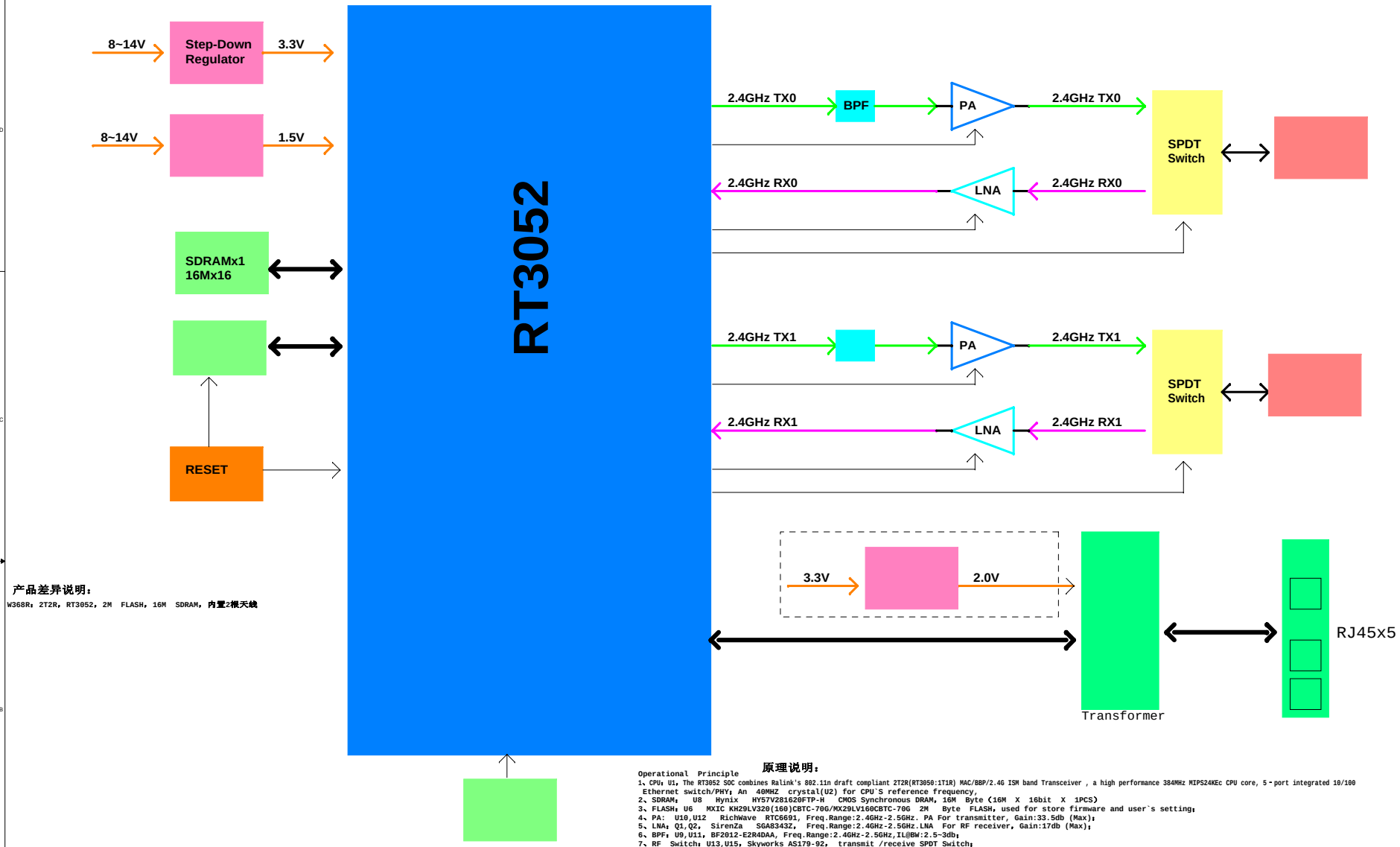


For Transformer

	TENDA	
Title	W368R	
Size C	Document Number 5-POWER-RESET.SCH	Rev 0.1
Date: Thursday, June 18, 2009	Sheet 12 of 14	



TENDA		
Title	W368R	
Size B	Document Number 6-LED.SCH	Rev 0.1
Date: Thursday, June 18, 2009	Sheet 13 of 14	



产品差异说明：

W368R：2T2R，RT3052，2M FLASH，16M SDRAM，内置2根天线

原理说明：

Operational Principle

1、CPU：U1，The RT3052 SOC combines Ralink's 802.11n draft compliant 2T2R(RT3050:1T1R) MAC/BBP/2.4G ISM band Transceiver , a high performance 384MHz MIPS24KEc CPU core, 5-port integrated 10/100 Ethernet switch/PHY；An 40MHZ crystal(U2) for CPU`S reference frequency,

2、SDRAM： U8 Hynix HY57V281620FTP-H CMOS Synchronous DRAM，16M Byte（16M X 16bit X 1PCS）

3、FLASH：U6 MXIC KH29LV320(160)CBTC-70G/MX29LV160CBTC-70G 2M Byte FLASH，used for store firmware and user`s setting；

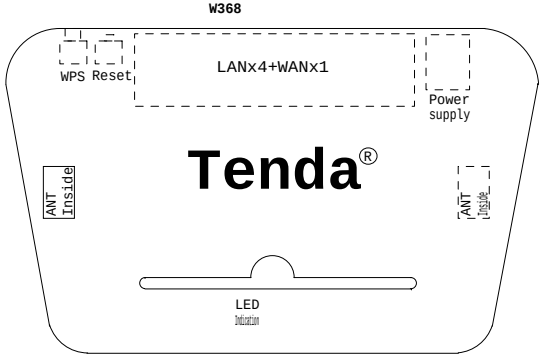
4、PA： U10，U12 RichWave RTC6691，Freq.Range:2.4GHz-2.5GHz. PA For transmitter，Gain:33.5db (Max)；

5、LNA：Q1，Q2， SirenZa SGA8343Z， Freq.Range:2.4GHz-2.5GHz.LNA For RF receiver，Gain:17db (Max)；

6、BPF：U9，U11，BF2012-E2R4DAA，Freq.Range:2.4GHz-2.5GHz,IL@BW:2.5~3db；

7、RF Switch：U13，U15，Skyworks AS179-92， transmit /receive SPDT Switch；

8、Power part: U16 and U14，CP2894 Step-Down PWM Converter，used for transfer DC8~14V to DC3.3V and DC1.5V ；；U25 SE8117TALF LDO used for transfer DC3.3V to DC2.0V；



TENDA		
Title	W368R	
Size C	Document Number RT3052 AP Block	Rev 0.1
Date: Thursday, June 18, 2009	Sheet 14 of 14	