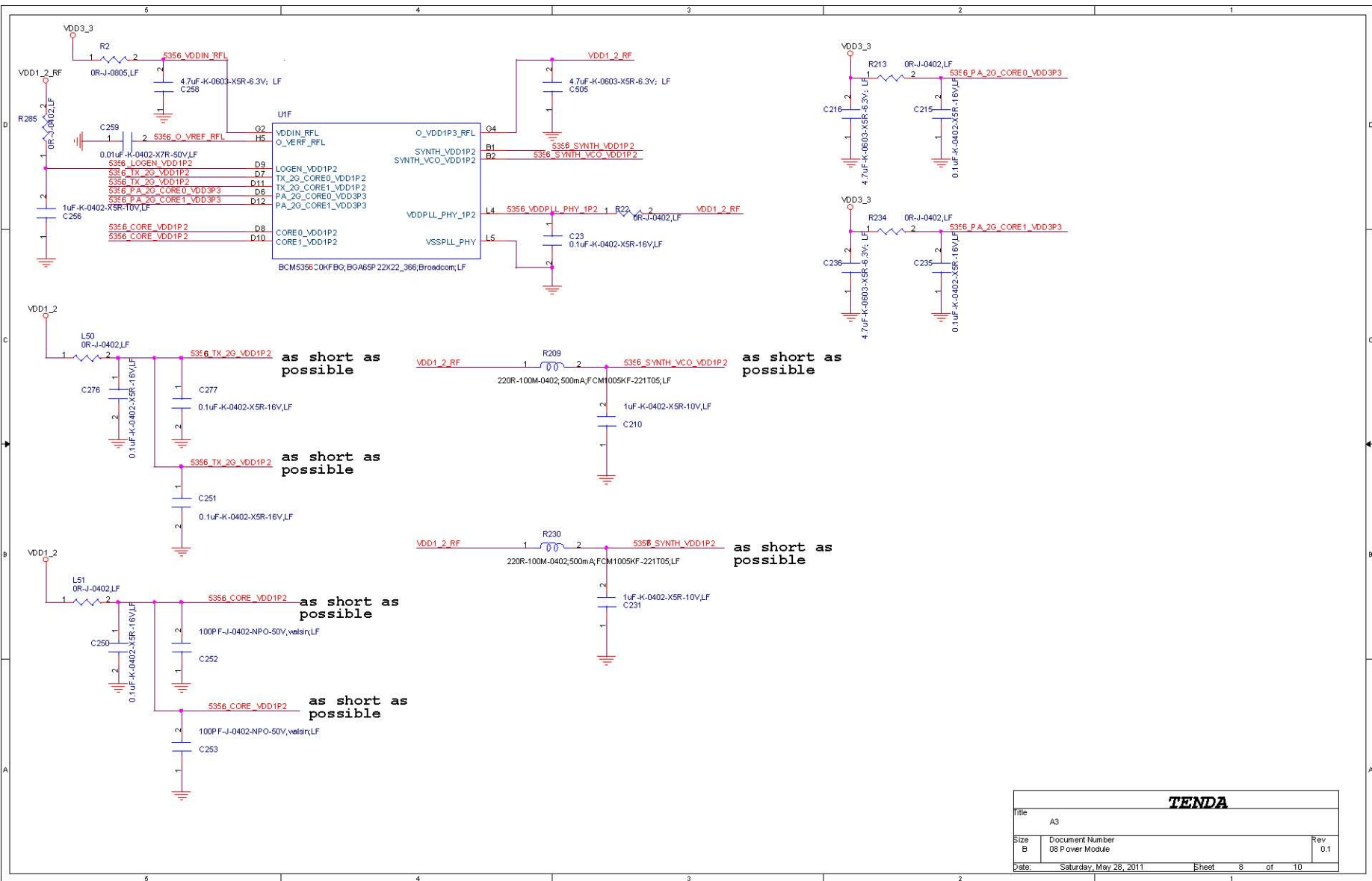
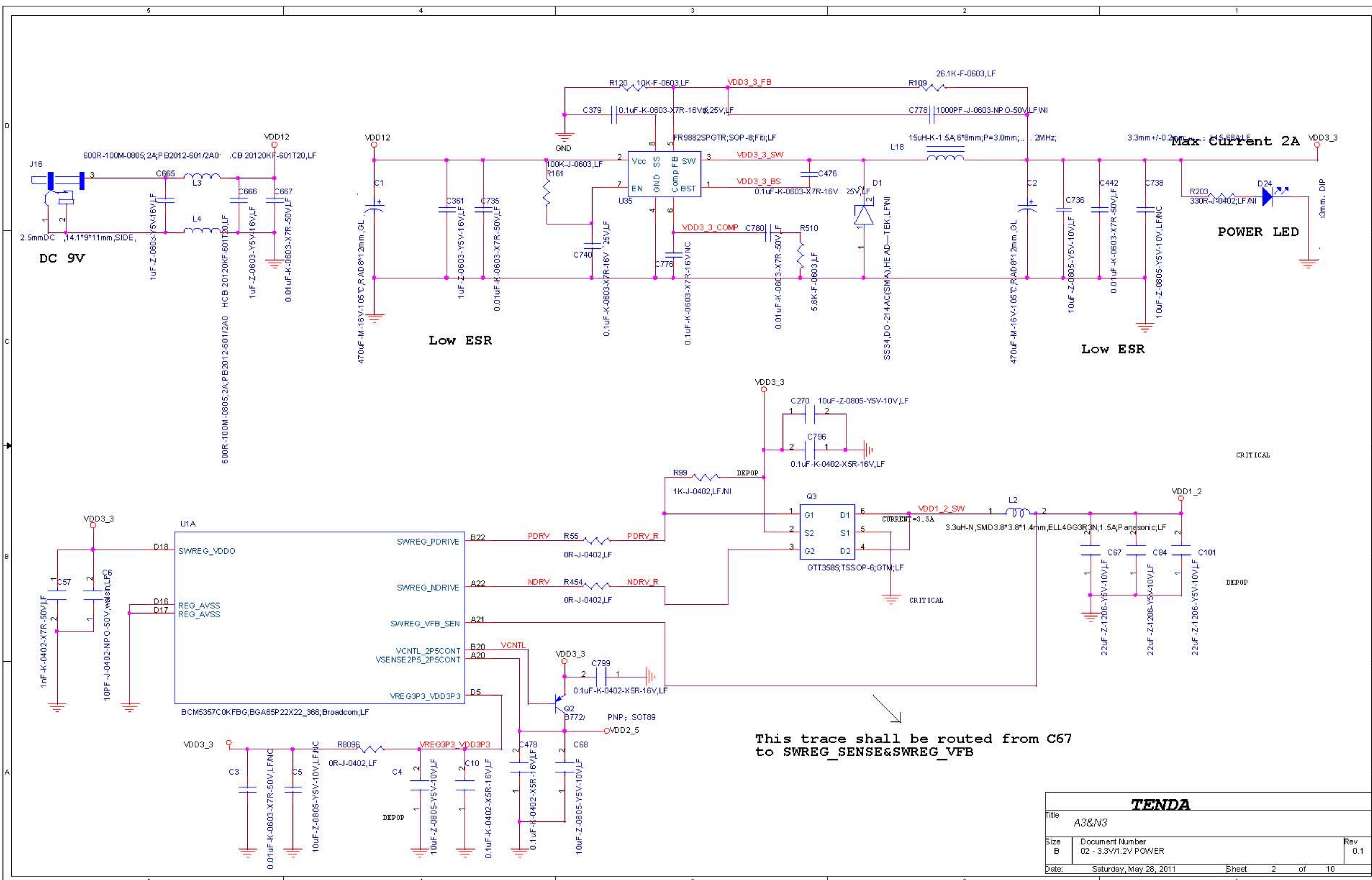


Strapping Description

| PIN NAME | DEFAULT | SETTING | DESCRIPTION | VALUE = 0 | VALUE = 1 |
|------------------------------|---------|---------|--|--------------------------------|--------------------------------|
| GPIO [17:16] | 10 | 10 | Boot Type 00: DDR boot 01: ROM boot 10: Serial Flash boot 11: NAND boot | | |
| GPIO14/mimophy_core0_ant_shd | 0 | 0 | Flash Type | ST Serial Flash | Atmel Serial Flash |
| gpio19/mimophy_core1_ant0_tx | 0 | 0 | Clock Ratio | mips:pl301a:pl301b=133:133:133 | mips:pl301a:pl301b=533:266:133 |
| mimophy_core0_ant0_tx | 1 | 1 | DDR I or II Mode | DDR2 mode | DDR1 mode |
| mimophy_core0_ant0_rx | 0 | 0 | NAND Flash Present | NAND Flash not present | NAND Flash Present |
| mimophy_core1_ant1_tx | 0 | 1 | DDR1 Class | DDR1_sst1_class1 | DDR1_sst1_class2 |
| mimophy_core1_ant1_rx | 0 | 0 | MIPS_Endian | Little Endian | Big Endian |

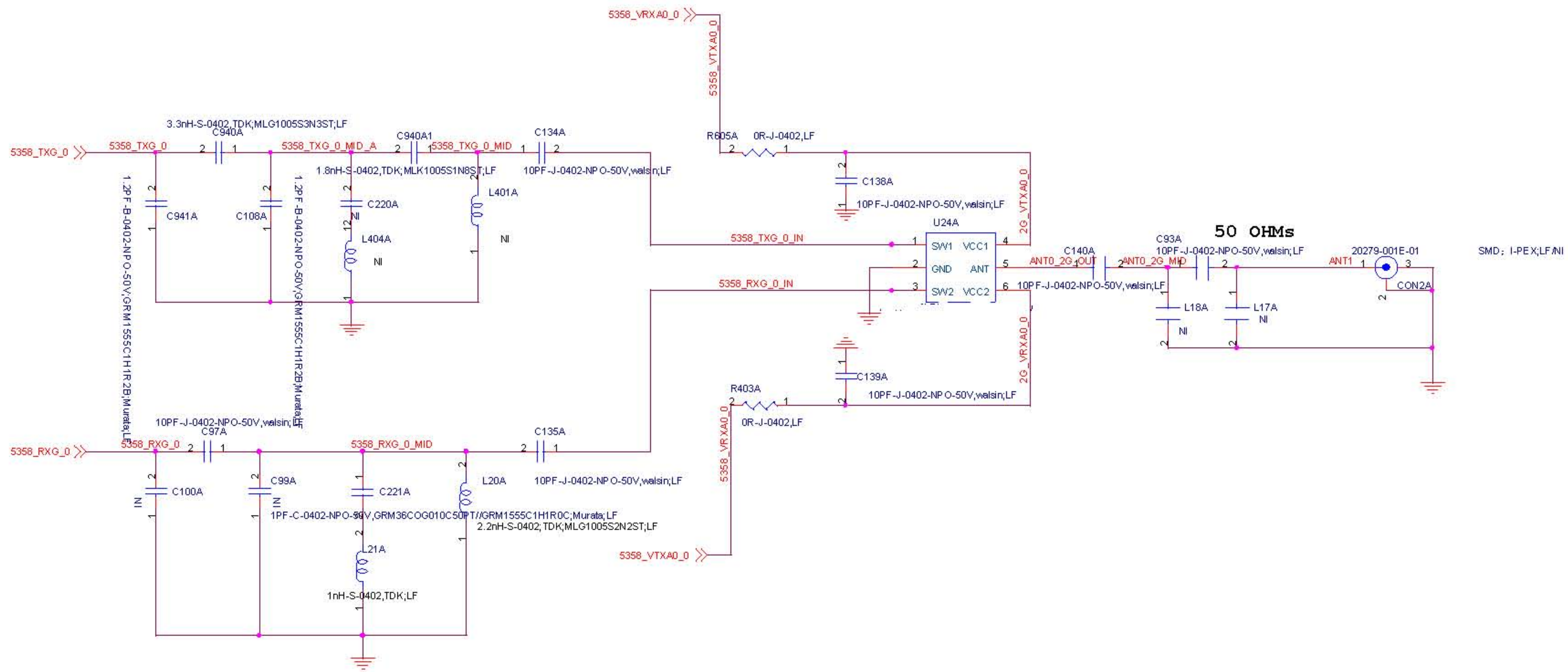
| | | |
|---------------------------------|--|------------|
| TENDA | | |
| Title A3&N3 | | |
| Size B | Document Number 04 - Boot Strapping | Rev 0.1 |
| Date: Saturday, May 28, 2011 | Sheet 4 | of 10 |





This trace shall be routed from C67 to SWREG_SENSE & SWREG_VFB

| | | |
|--------------|------------------------|---------------|
| TENDA | | |
| Title | A3&N3 | |
| Size | Document Number | Rev |
| B | 02 - 3.3V/1.2V POWER | 0.1 |
| Date: | Saturday, May 28, 2011 | Sheet 2 of 10 |



SMD: I-PEX,LF,NI

| | | |
|--------------|------------------------|---------------|
| TENDA | | |
| Title | A3&N3 | |
| Size | Document Number | Rev |
| B | 03 Front End | 0.1 |
| Date: | Saturday, May 28, 2011 | Sheet 3 of 10 |