Circuit Descriptions

ACR320 - Ticket Validator

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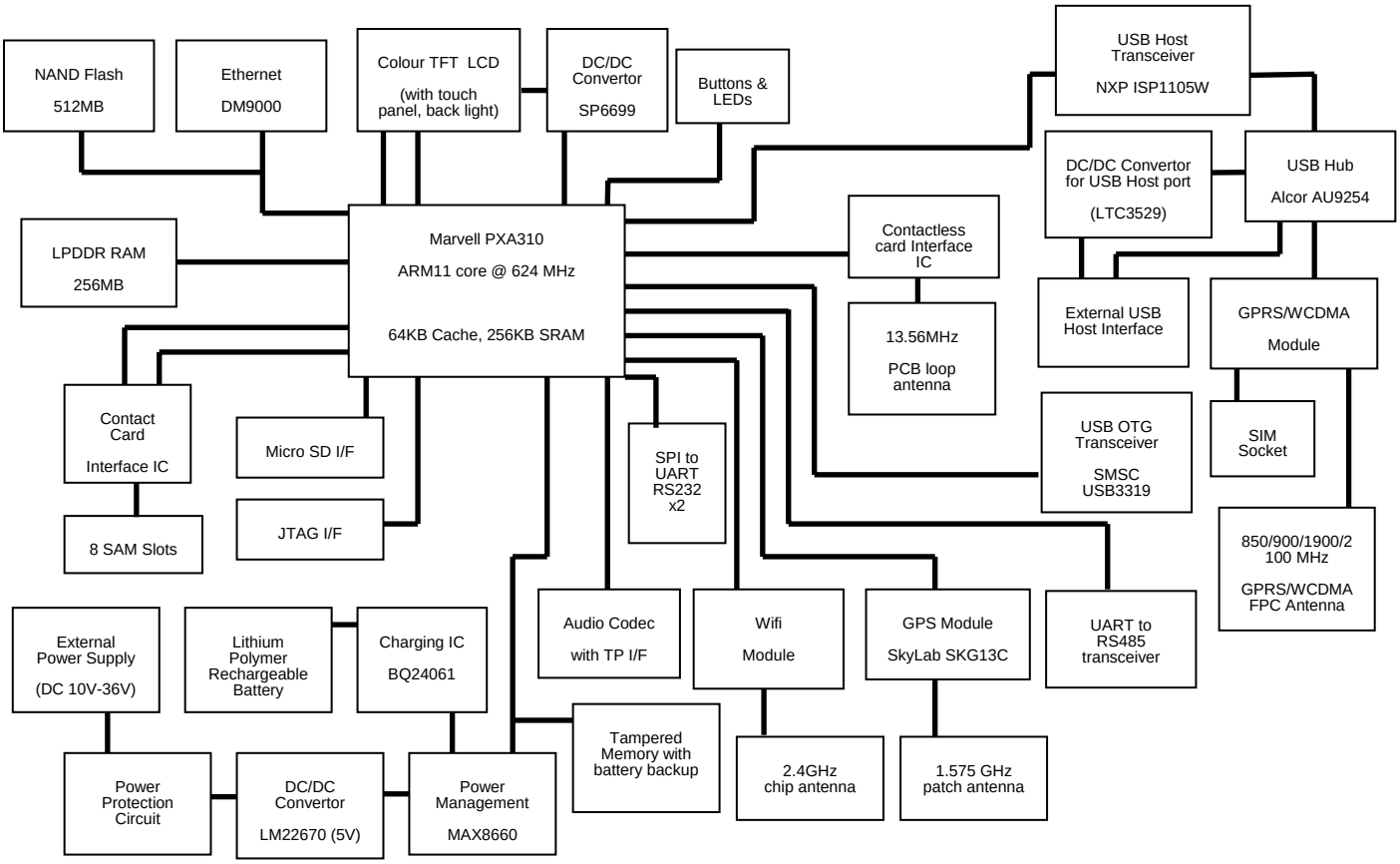
1.0. Introduction

This documents specifies the top level implementations for ACR320, Ticket Validator Project. The validator is a pole-mounted or wall-mounted unit that processes contactless smart cards (CSC) and presents information to the transit patron via a LCD.

The validator shall be a compact device that is meant to operate in standalone mode or in concert with an external host device to provide a comprehensive AFC solution for onboard applications. It has the capability to read and write to CSCs and display information to the patron via LEDs, LCD, and audio. The validator shall support multiple interfaces to communicate with a host or central computer. User buttons shall be available to allow the patron to make selections.

2.0. System Block Diagram



3.0. Hardware Design

3.1. CPU

The Marvell PXA310 CPU is used in our design. PXA310 is with high processing power and low power consumption features which is good for multi-purpose, multi-media and portable applications. It can fit on the requirements of the customer e.g. different kinds of peripherals, multi-media output, processing power, etc.

3.2. LPDDR Memory

LPDDR Memory at 133/166MHz is used in our design. The low voltage operation (1.8V) leads to low current consumption while maintaining high read/write speed. 256Mbytes LPDDR is used according to the requirement from customer. It is connected to the CPU using high speed DDR bus.

3.3. NAND Flash Memory

SLC NAND Flash is supported by PXA310. 512Mbytes NAND Flash is used according to the user requirement. It is connected to the DFI bus of PXA310. It is connected to the CPU via the DFI bus.

3.4. USB Host and Client

An external USB 1.1 Host (High speed) is provided. Because we need another USB host interface for the internal 3G module, a USB hub (AU9254) will be added. The AU9254 is connected to the CPU via the ISP1105 USB transceiver. An external USB 2.0 high speed client port is provided. The USB transceiver USB3319 from SMSC is used which required a 1.8V power and is connected to the CPU via ULPI interface.

3.5. RS232/RS485

The IC MAX3111E converts SPI signal to RS232. An RS232/RS485 port is provided. The RS232/RS485 can be selectable by the hardware IO connector. The RS485 port is provided by converting the UART signal of CPU to RS485 signal using MAX3485 IC.

3.6. Ethernet

DM9000 is used as the ethernet controller. The DFI bus interface is used to interface between CPU and DM9000.

3.7. Wifi

The Wifi module WM-BG-MR-03 from USI is used because of the small in size, low cost and simple hardware requirements. The chipset inside is Marvell 88W8688. Drivers for WM and Linux are provided by the supplier. CPU uses the SDIO interface to control the module for the Wifi function.

A 2.4GHz chip antenna is used. A pi network should be placed between the antenna and the module for further matching.

3.8. 3G / WCDMA / GPRS

The module SIM5215A from SIMCOM is used to satisfy the HSPA/WCDMA/EDGE/GPRS requirements. To optimize the communication speed, USB interface is used. The maximum peak current of the module can be 2A. So, it should be considered in the power circuit design.

A 5 bands FPC antenna is used and the design will be out-sourced to a 3rd party antenna design house.

3.9. GPS

The module SKG13C from Skylab is used due to the high sensitivity and low cost. The module uses the MTK3329 chipset. The UART interface is used. A backup power should be provided even we turn off the main power of GPS module so as to provide warm start feature.

3.10. LCD

A 5.7" TFT LCD from Tianma is used. RGB interface is used to communicate with CPU.

3.11. Audio

The codec IC, WM9713, from Wolfson is used as the audio codec. It equipped with an ADC which can be used as battery level detection. An extra power amplifier, LM4871 from NS, is added to further increase the volume as the unit may be used in crowd environment. A 2W, 8 Ohm mono speaker is used.

3.12. Buttons

4 Buttons are provided. The keyboard interface of CPU is used. Another suspend button is provide for entering/exiting the suspend/sleep mode.

3.13. LED

4 programmable LEDs are provided and connected to the GPIOs of the CPU. And the buttons backlight LEDs are also driven by a single GPIO via a transistor.

3.14. SAM card slots

Two AT83C26 smartcard interface ICs will be use to multiplex the ISO7816 channel of CPU to 8 ISO7816 channels. It also can manage the power supplied to the SAM cards to satisfy Class A/B/C requirements. I2C interface is used to configure the AT83C26 IC.

3.15. Contactless card interface

The RC531 IC is selected for the contactless card interface according to the supported card type requirements and EMV requirements. The SPI interface is used. The contactless card interface IC and antenna will be placed on a dedicated PCB for easy replacement between different solution.

3.16. MicroSD card slots

A MicroSD card slot with the cover can be opened upward is used. CPU uses the MMC interface to access it.

3.17. RTC with SRAM

PCF8583 is selected as the RTC with SRAM (240 bytes). It can work with a tampered switch for storing security sensitive information. Upon releasing the switch, the power of this IC is removed and hence erased the data inside. It is connected to the CPU via I2C interface.

3.18. Rechargeable Battery

A 1800mAh Lithium Ion battery is used. When the external power is removed, this battery can sustain the system to around 2 hours. The BQ24061 charging IC from TI is used for managing the whole charging process and reports the charging status to CPU.

3.19. Power Management

The power management IC MAX8660 from Maxim is chosen because of its simplicity and it works well with Xscale series CPUs. The arrangement of the 8 power outputs are shown below:

Output	Net	Voltage
1 (Buck)	V_3V	3.3V
2 (Buck)	V_1P8V	1.8V
3 (Buck)	V_CORE_APPS	1.4V
4 (Buck)	V_SRAM	1.4V
5 (LDO)	V_MVT	1.8V
6 (LDO)	V_SDIO	3.3V
7 (LDO)	V_CI	1.8/3.3V
8 (LDO)	V8	3.3V

The low battery detection feature of MAX8660 is configured to 3.15V (falling down) by resistor. After low battery level occurs, the LBO signal will be asserted and the CPU will enter sleep mode by hardware.

Diodes are added in first stage of power supply circuit for protecting from high speed surge and reverse voltage. Then a over-voltage protection IC (LM5060Q) is added for protecting voltage from above 36VDC.

A buck DC/DC convertor (LM22670) is added in the next stage for down converting the input supply (10-36V) to 5V before going to the MAX8660. Proper filtering should be applied to sustain under dirty power source of vehicles.

A flip-flop block (TC7W74FK) is added for detecting the insertion of external power while the system is in sleep mode.