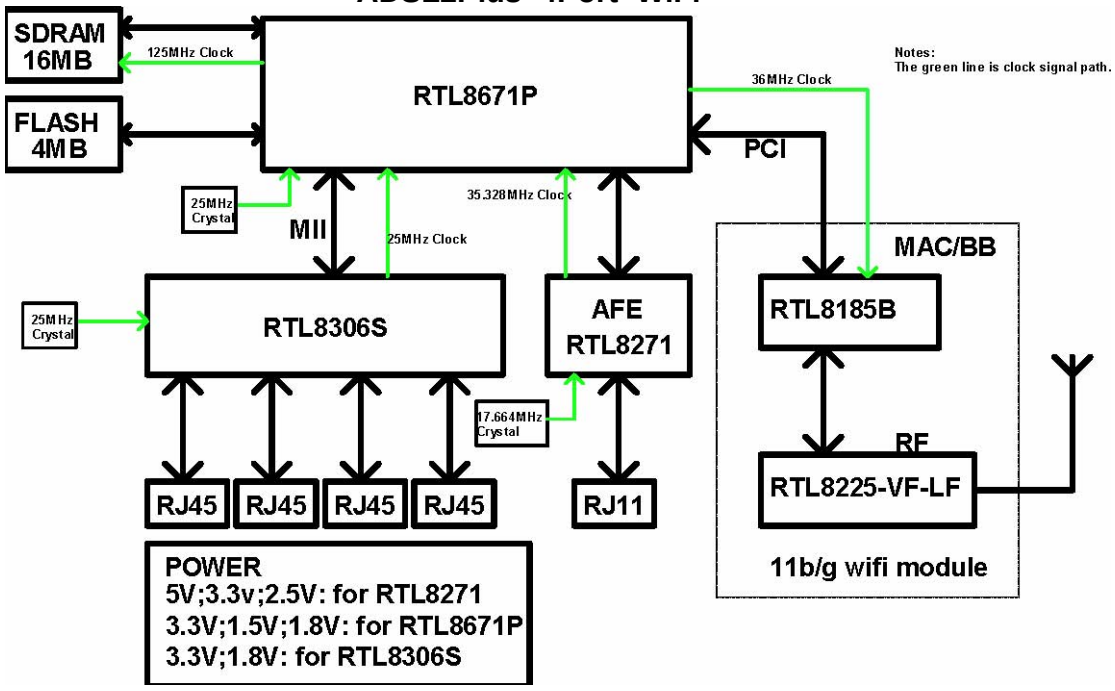
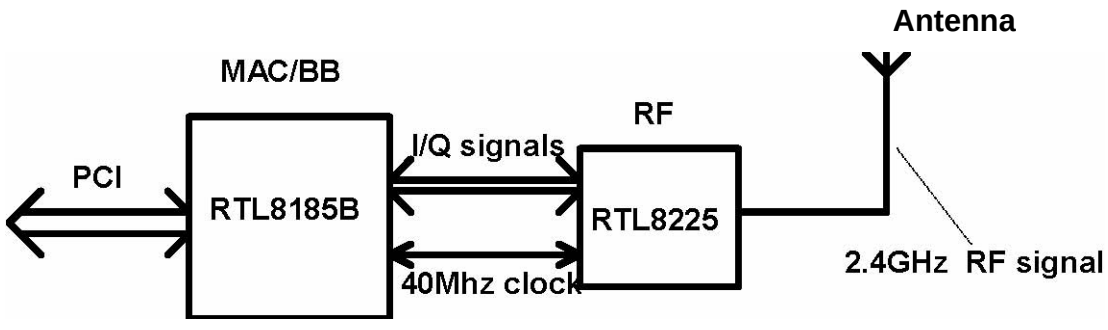
The primary principle of Gaw9.2z39-4 circuit design

Gaw9.2z39-4 is an adsl2+ gateway with 4 Ethernet ports and wifi access point function complied IEEE802.11b/g, this product uses Realtek total solution. The system block diagram is shown bellow. The RTL8671P is an high integrated SOC chip featuring a RISC(CPU), a 10/100Mbps MAC with Ethernet transceiver with MAC mode MII interface(connecting to LAN Switch chip RTL8306S to provide 4 Ethernet ports), and a PCI host/device bridge interface(connecting to an IEEE802.11b/g RF module). The RTL8271 is ADSL2+ Analog Front End chip. it implements ADSL2+ function mated with the RTL8671P. The power supply section provides 5.0V, 3.3V, 2.5V 1.8V and 1.5V power for the chips on board. When the board power up, the RTL8671P(CPU) reads instruction from Flash to initialize the hardware and boot operation system. The system will automatically run according to the software design after operation system booted up.



ADSL2+ gateway system block diagram The following is the block diagram of 11b/g wifi module



11b/g wifi module block diagram

11b/g wifi module specification

Compliant standard:

IEEE802.11b, IEEE802.11g

Modulation Techniques:

IEEE802.11b: Complementary Code Keying (CCK) IEEE802.11g: Orthogonal Frequency Division Multiplexing (OFDM)

Operating Channel: 802.11b & g

11: (Ch. 1-11) – N. America(default)

13: (Ch. 1-13) – Europe ETSI(option)

14: (Ch. 1-14) – Japan(option)

Frequency range:

2.412 ~ 2.462 GHz – N. America

2.412 ~ 2.472 GHz – Europe ETSI

2.412 ~ 2.484 GHz – Japan

RF Output Power:

IEEE802.11b:18.5dBm±1.5dBm

IEEE802.11g:14.5dBm±1.5dBm

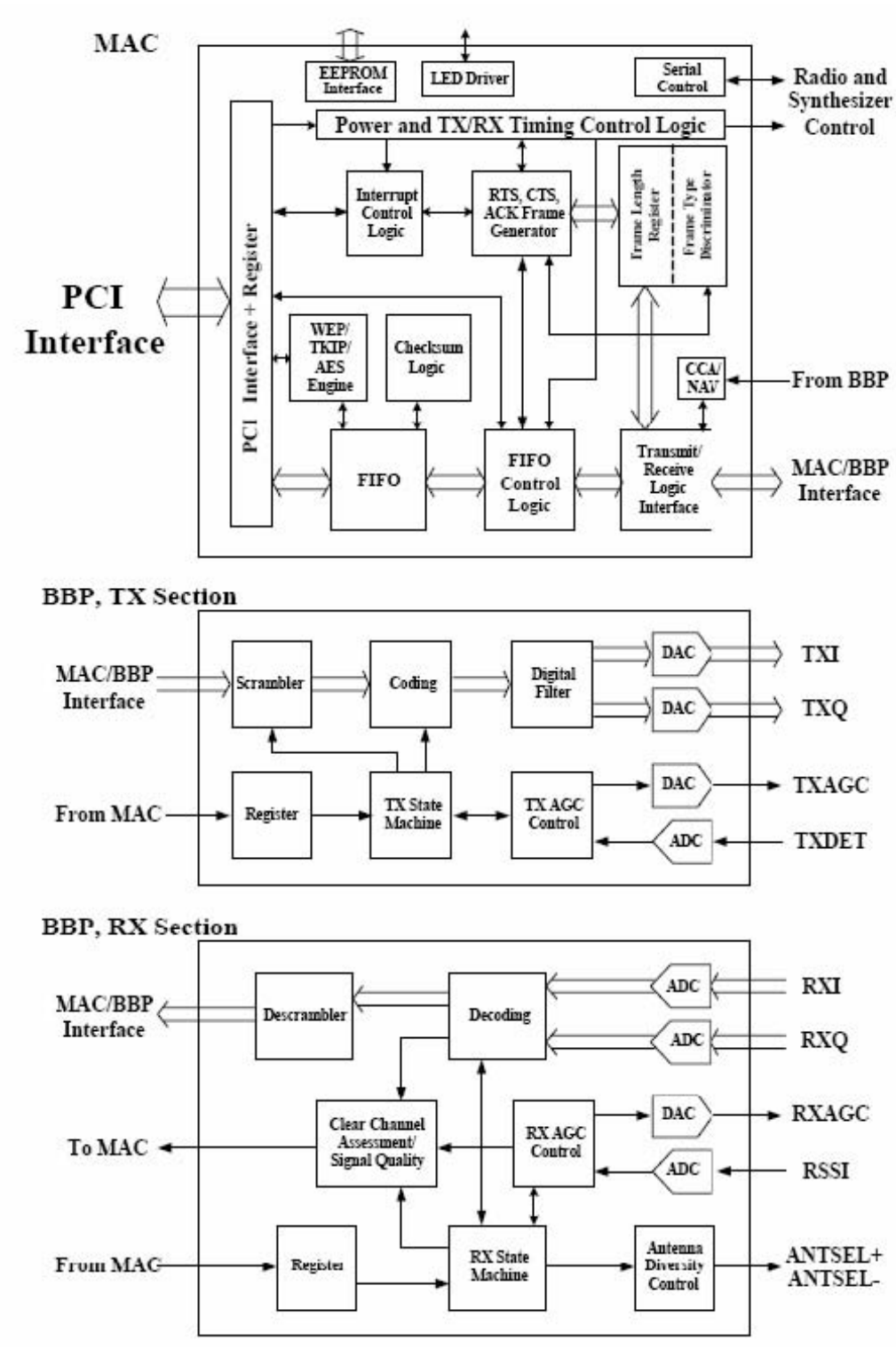
Antenna type:

Single external Omni-Directional wifi Antenna

Antenna gain:

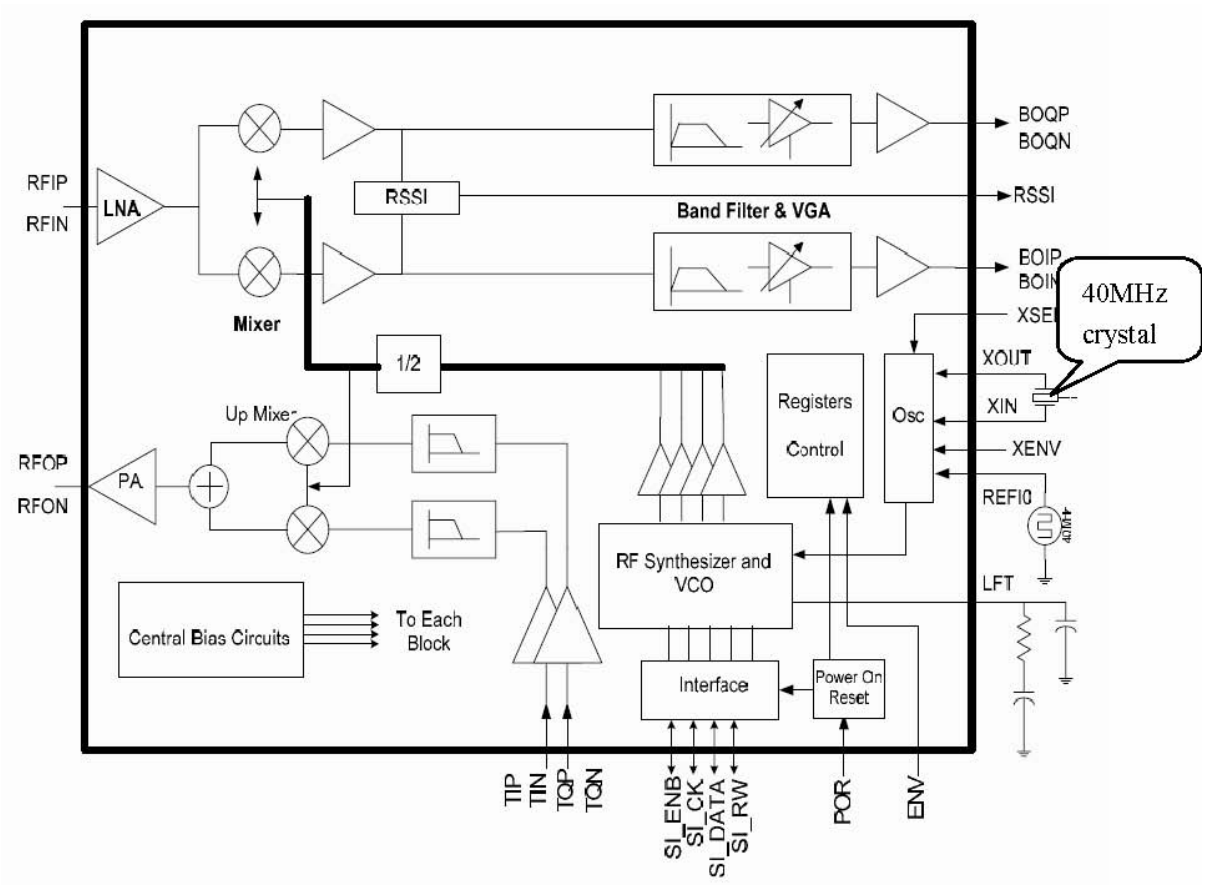
2.0±0.7dBi

The following figure is the RTL8185B chip block diagram



RTL8185B chip block diagram

The following figure is the RTL8225 chip block diagram



RTL8225 chip block diagram