

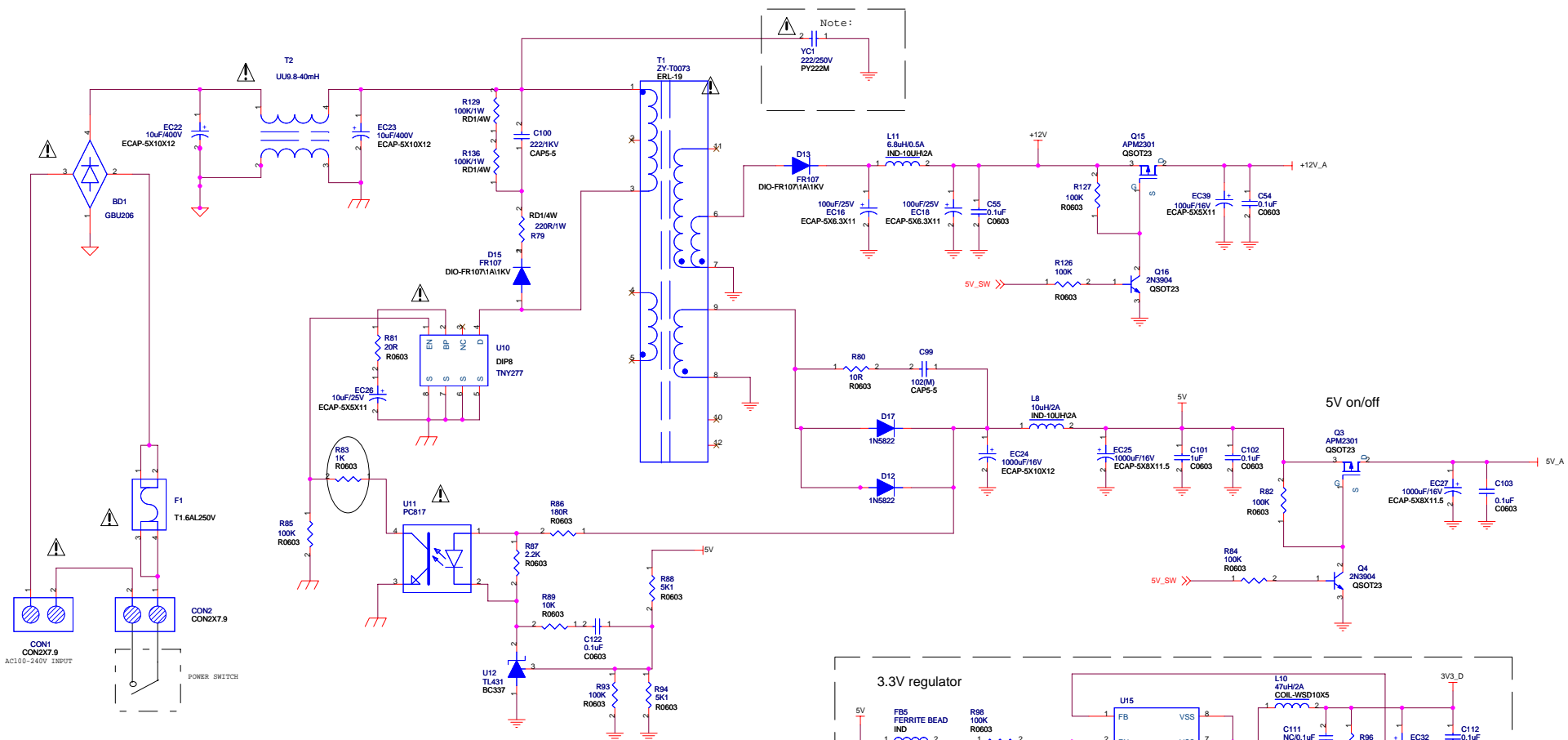
# AT2016 (ZR39741) SCHEMATEIC DIAGRAM

- 01: COVER PAGE
- 02: POWER SUNPPLY
- 03: POWER & GROUND
- 04: GPIO
- 05: SUPER I/O
- 06: DDR
- 07: RF & Video Input
- 08: Audio Output
- 09: Video Output
- 10: FRONT PANEL SW & IRR
- 11: SMART ANTENNA I/F

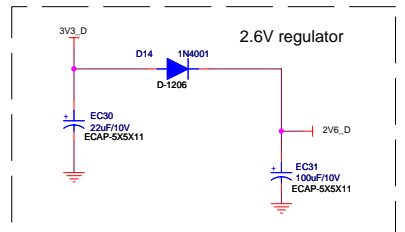
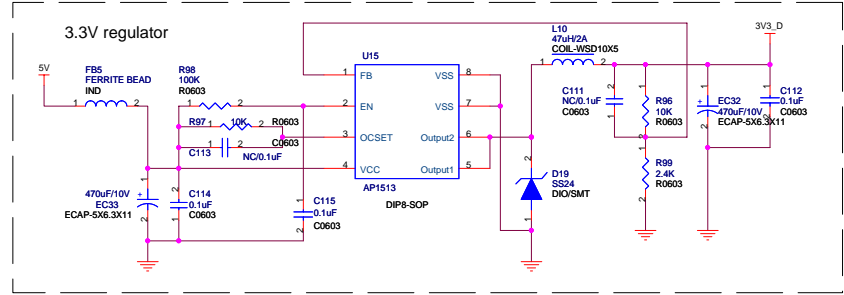
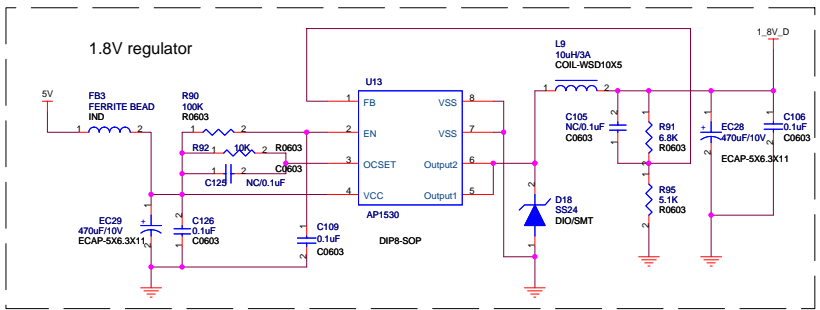
DESIGN:	MODEL: AT2016(ZR39741)	TITLE: COVER PAGE
CHECKED:	PART NO.:	DWG NO: AT2016-YL01-01(A)
APPRD:	SHEET: 1 OF 11	VER: A

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Table NO.: QR-RD-016A

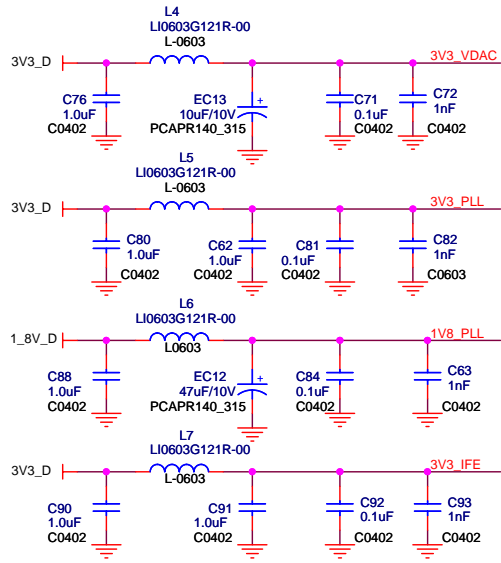


Note:  
 YC1 222/250V PY222M



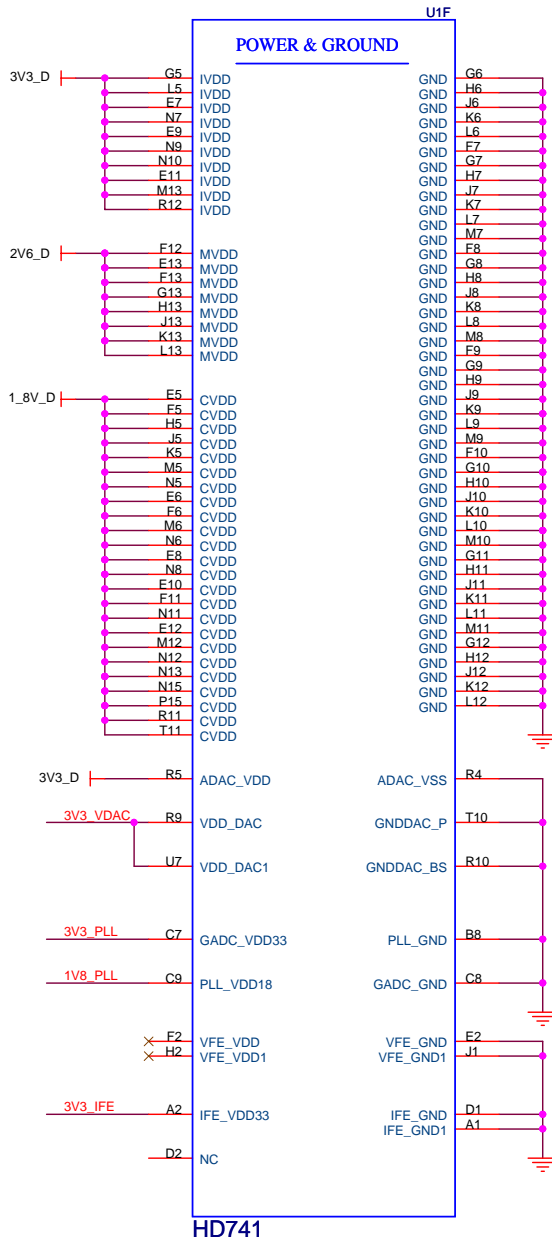
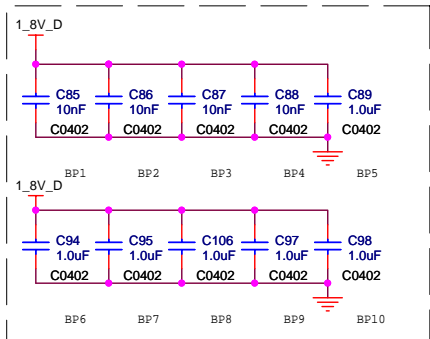
**Power Supply**

DESIGN:	MODEL: AT2016(ZR39741)	TITLE: POWER SUPPLY
CHECKED:	PART NO.:	DWG NO: AT2016-YL01-01(A)
APPRD:	SHEET: 2 OF 11	VER: A



Place cap near pin

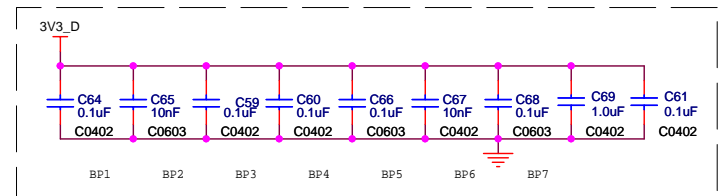
HD-741 1.8V Bypass Caps



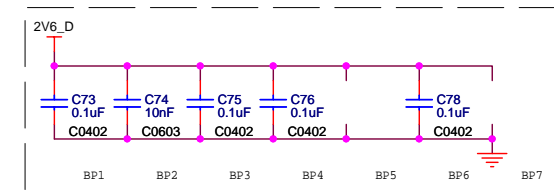
HD741

**Power and Ground 1**

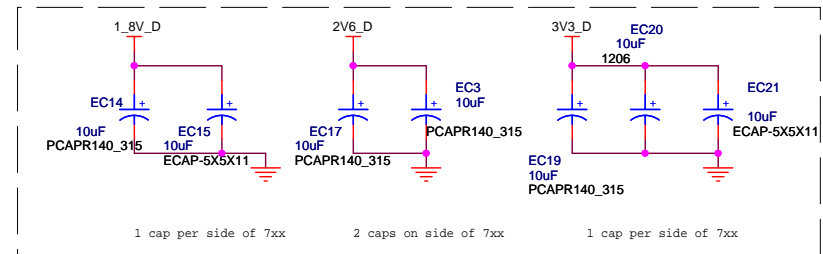
HD-741 3.3V Bypass Caps



HD-741 2.6V Bypass Caps

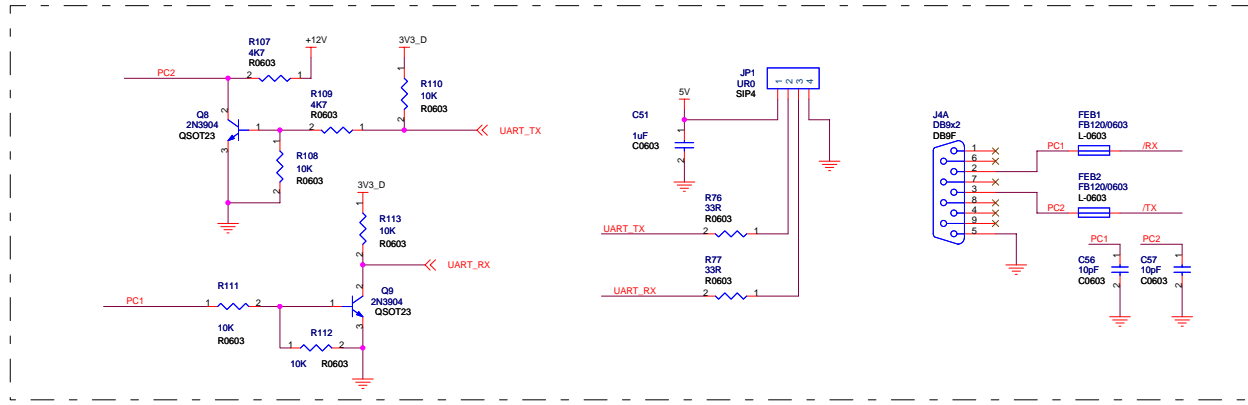
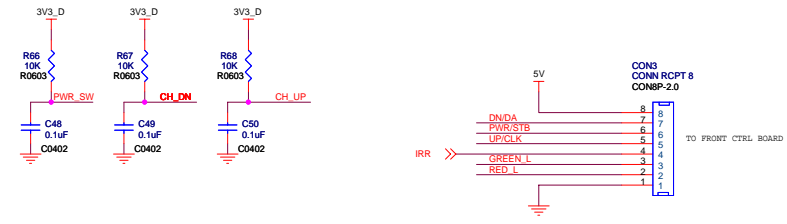
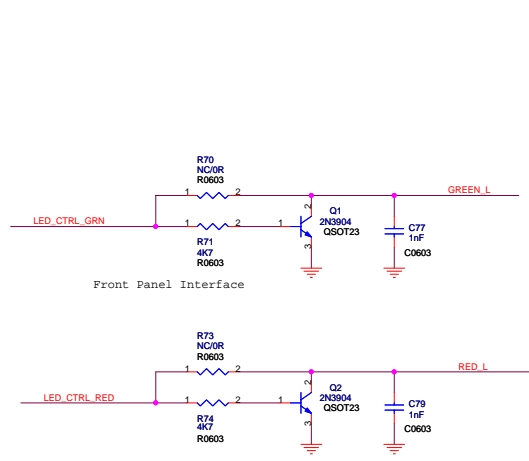
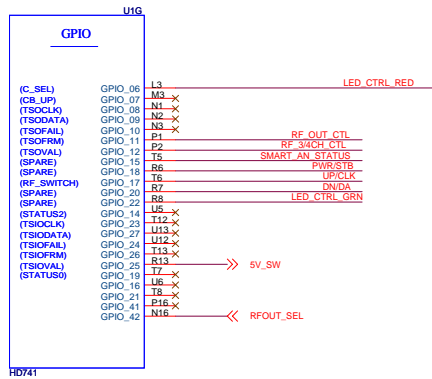


HD-741 Bulk Bypass Caps



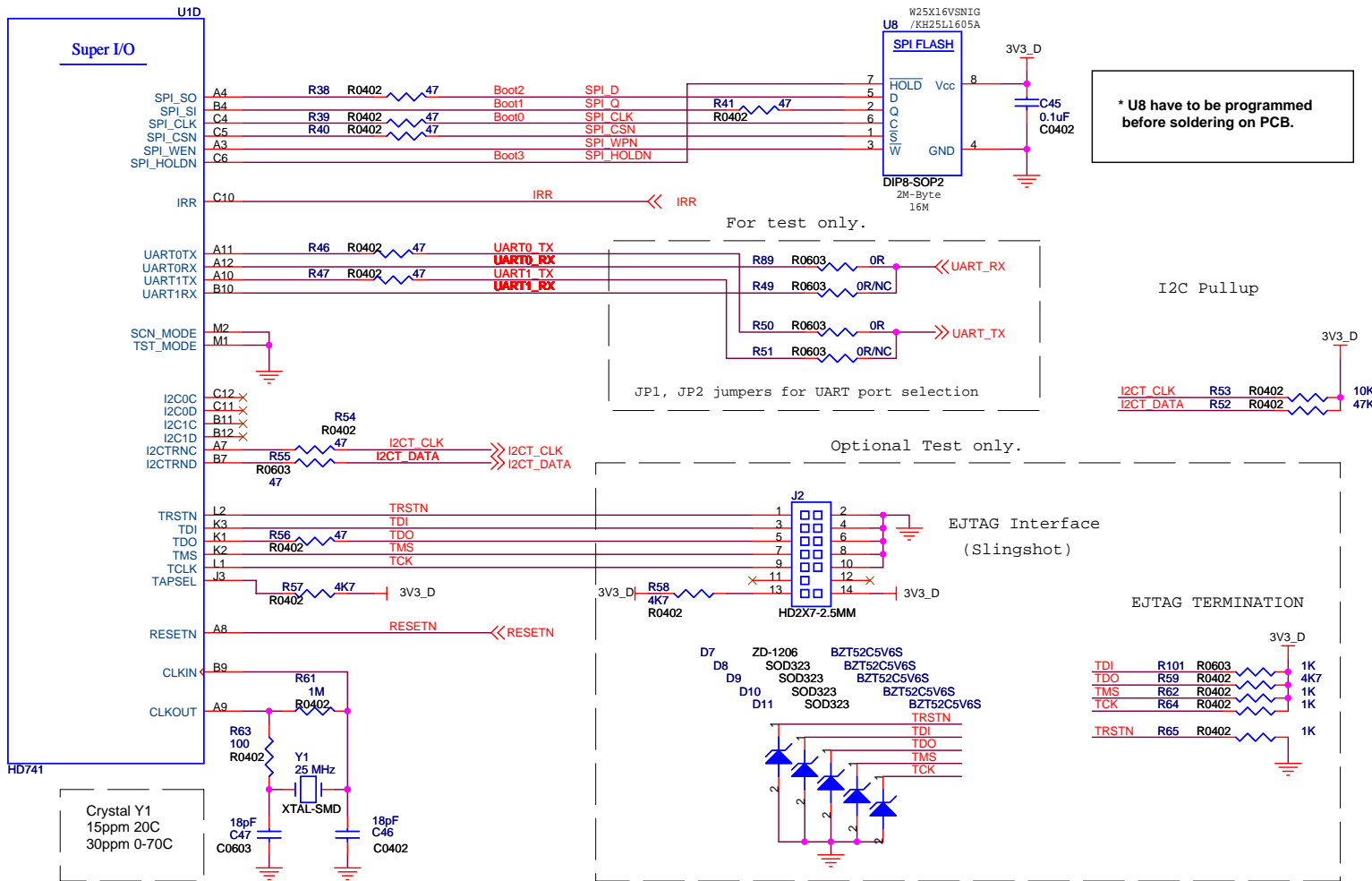
DESIGN:	MODEL: AT2016(ZR39741)	TITLE: POWER & Ground
CHECKED:	PART NO.:	DWG NO: AT2016-YL01-01(A)
APPRD:	SHEET: 3 OF 11	VER: A

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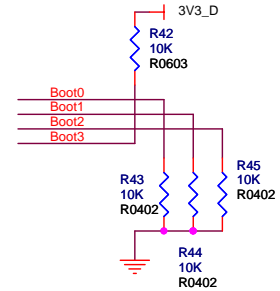
**GPIO**

DESIGN:	MODEL: AT2016(ZR39741)	TITLE: GPIO
CHECKED:	PART NO.:	DWG NO: AT2016-YL01-01(A)
APPRD:	SHEET: 4 OF 11	VER: A

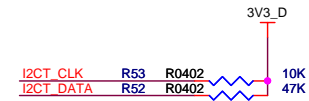


\* U8 have to be programmed before soldering on PCB.

SPI BOOT Setting



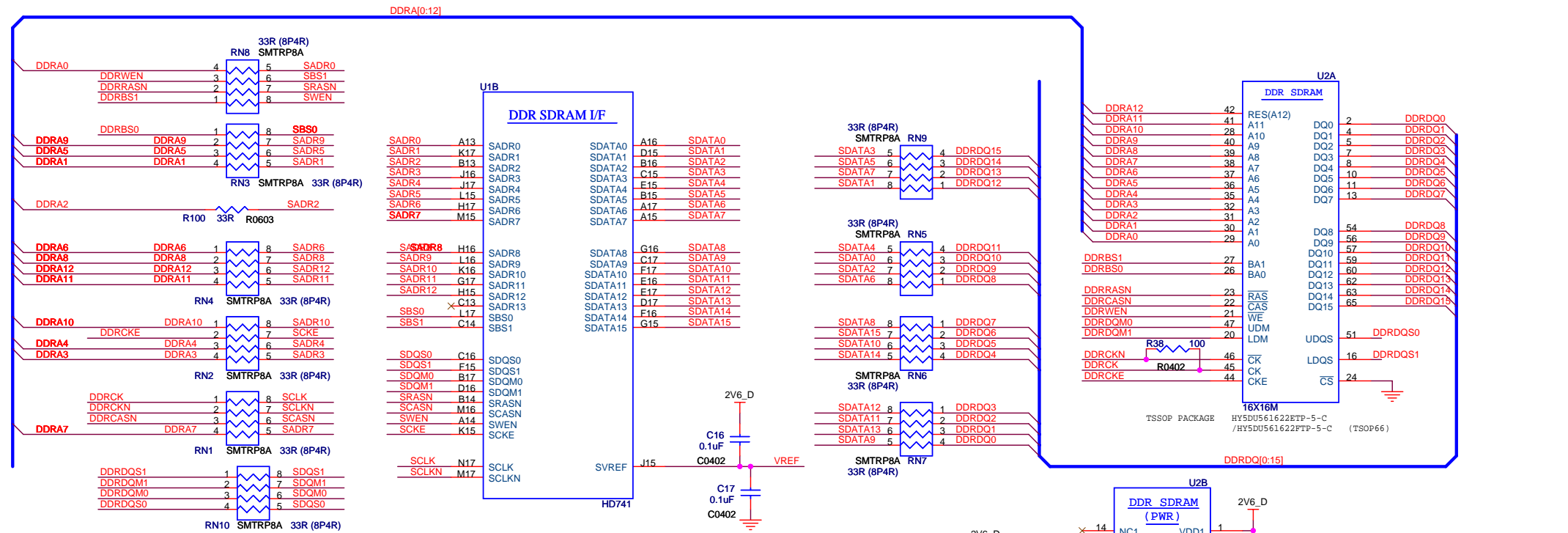
I2C Pullup



Super I/O

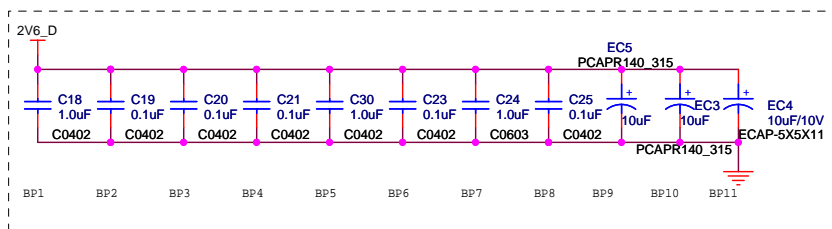
DESIGN:	MODEL: AT2016(ZR39741)	TITLE: Super I/O
CHECKED:	PART NO.:	DWG NO: AT2016-YL01-01(A)
APPRD:	SHEET: 5 OF 11	VER: A

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- DDRWEEN
- DDRWRASN
- DDRBS1
- DDRBS0
- DDRCKE
- DDRCK
- DDRCKN
- DDRCASN
- DDRQ0S1
- DDRQ0M1
- DDRQ0M0
- DDRQ0S0
- DDRQ0S0

DDR Bypass Caps

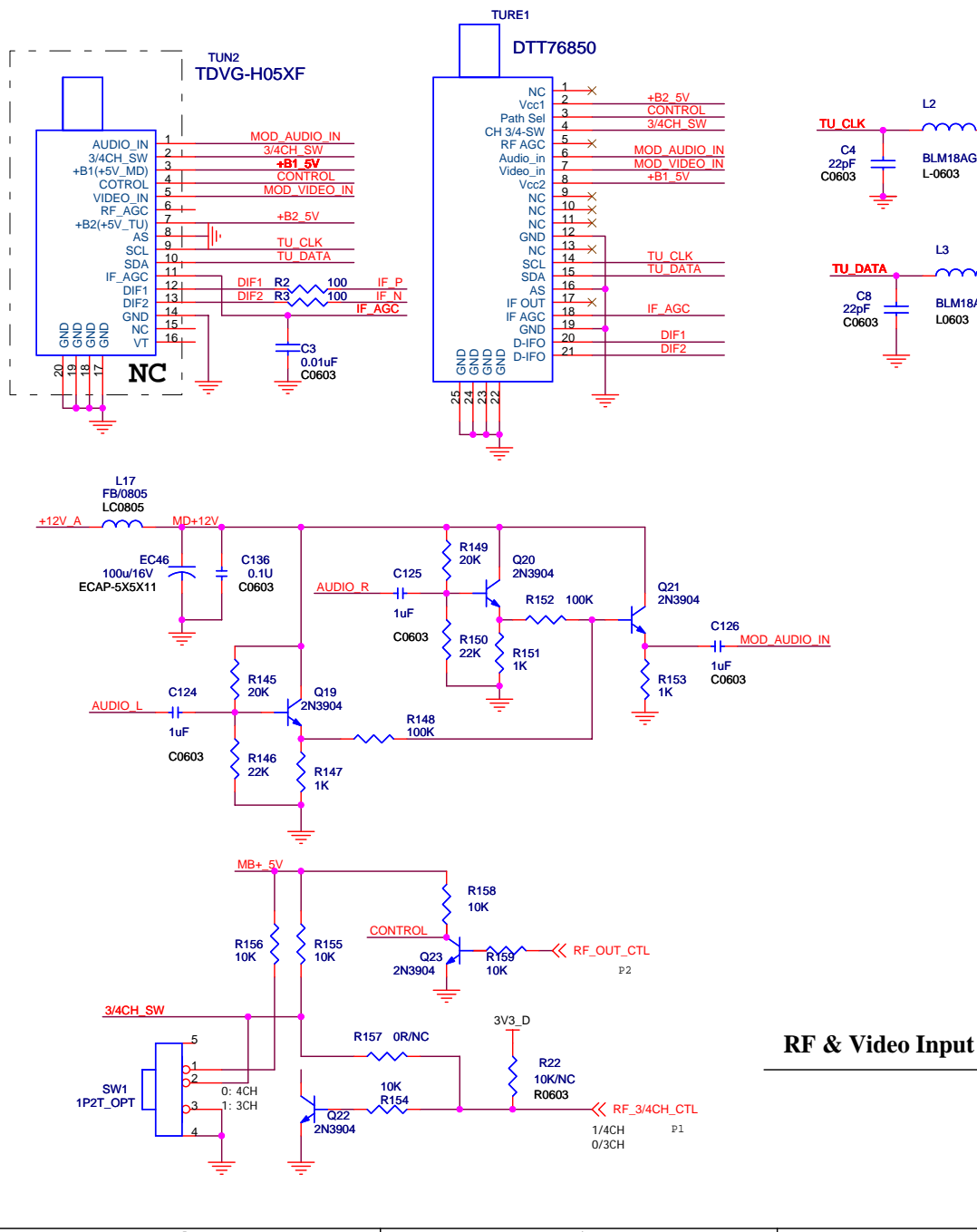


- BP1 = Pin 1 DDR
- BP2 = Pin 3 DDR
- BP3 = Pin 61 DDR
- BP4 = Pin 9 DDR
- BP5 = Pin 55 DDR
- BP6 = Pin 15 DDR
- BP7 = Pin 33 DDR
- BP8 = Pin 18 DDR
- BP9 = Pin 61 DDR
- BP10 = Pin 9 DDR

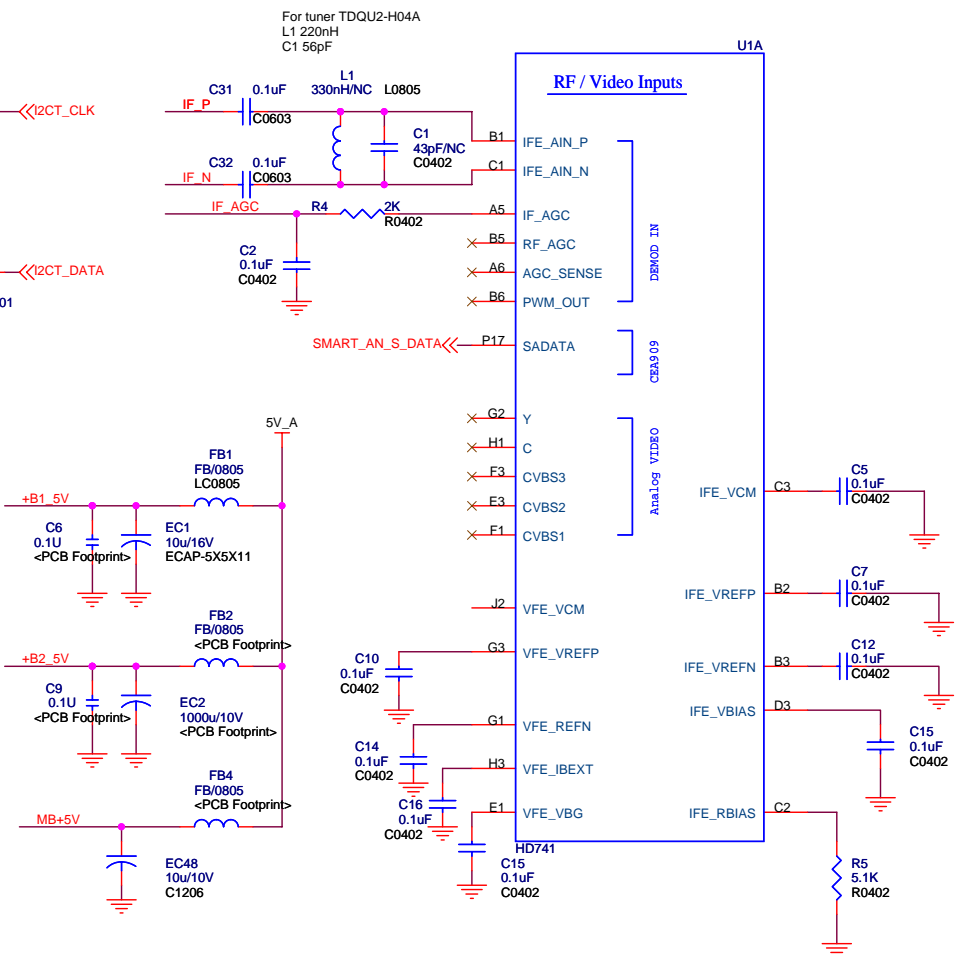
- BP11 = Pin 33 DDR

**DDR**

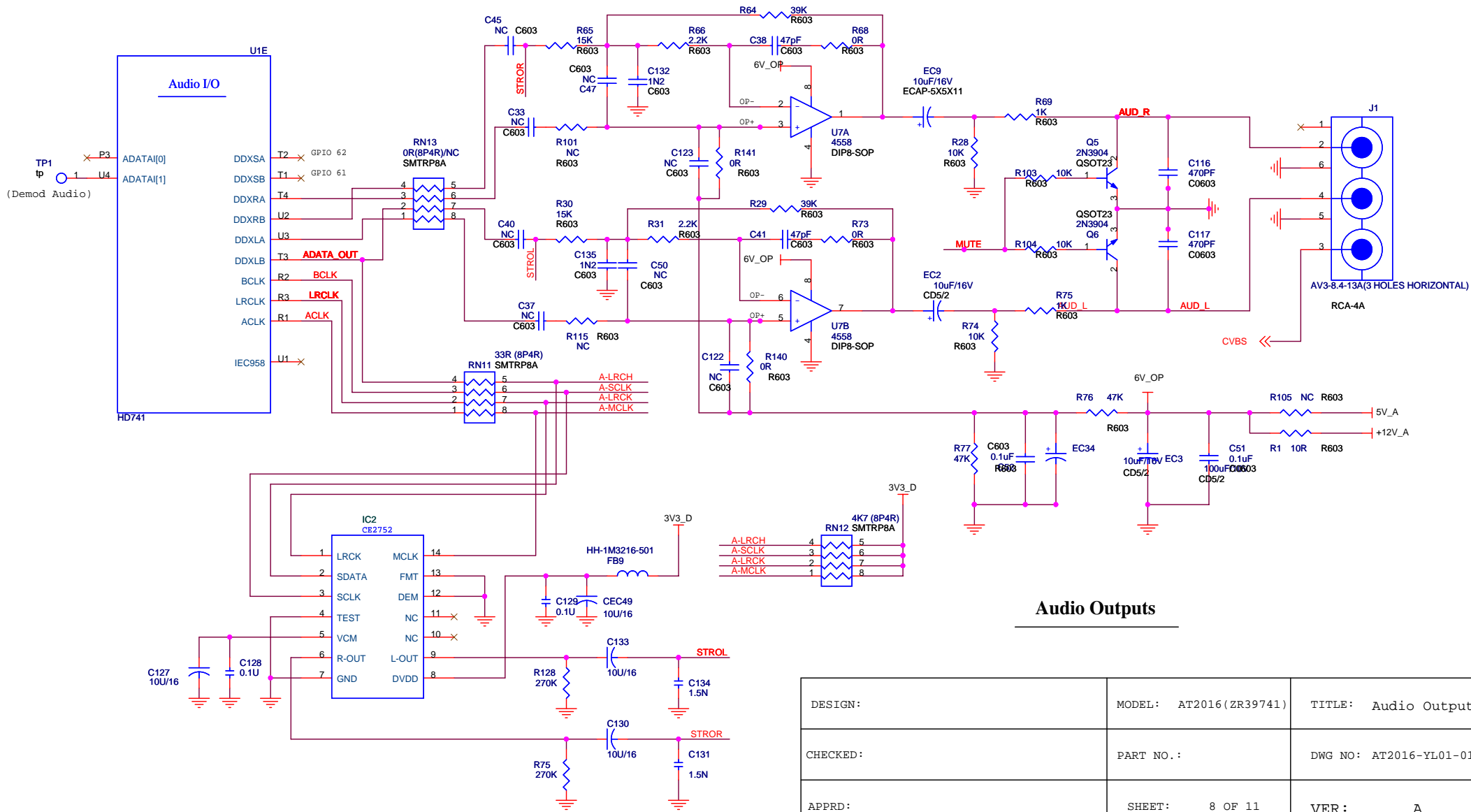
DESIGN:	MODEL: AT2016 (ZR39741)	TITLE: DDR
CHECKED:	PART NO.:	DWG NO: AT2016-YL01-01(A)
APPRD:	SHEET: 6 OF 11	VER: A



**RF & Video Input**



DESIGN:	MODEL: AT2016(ZR39741)	TITLE: RF&Video Inputs
CHECKED:	PART NO.:	DWG NO: AT2016-YL01-01(A)
APPRD:	SHEET: 7 OF 11	VER: A



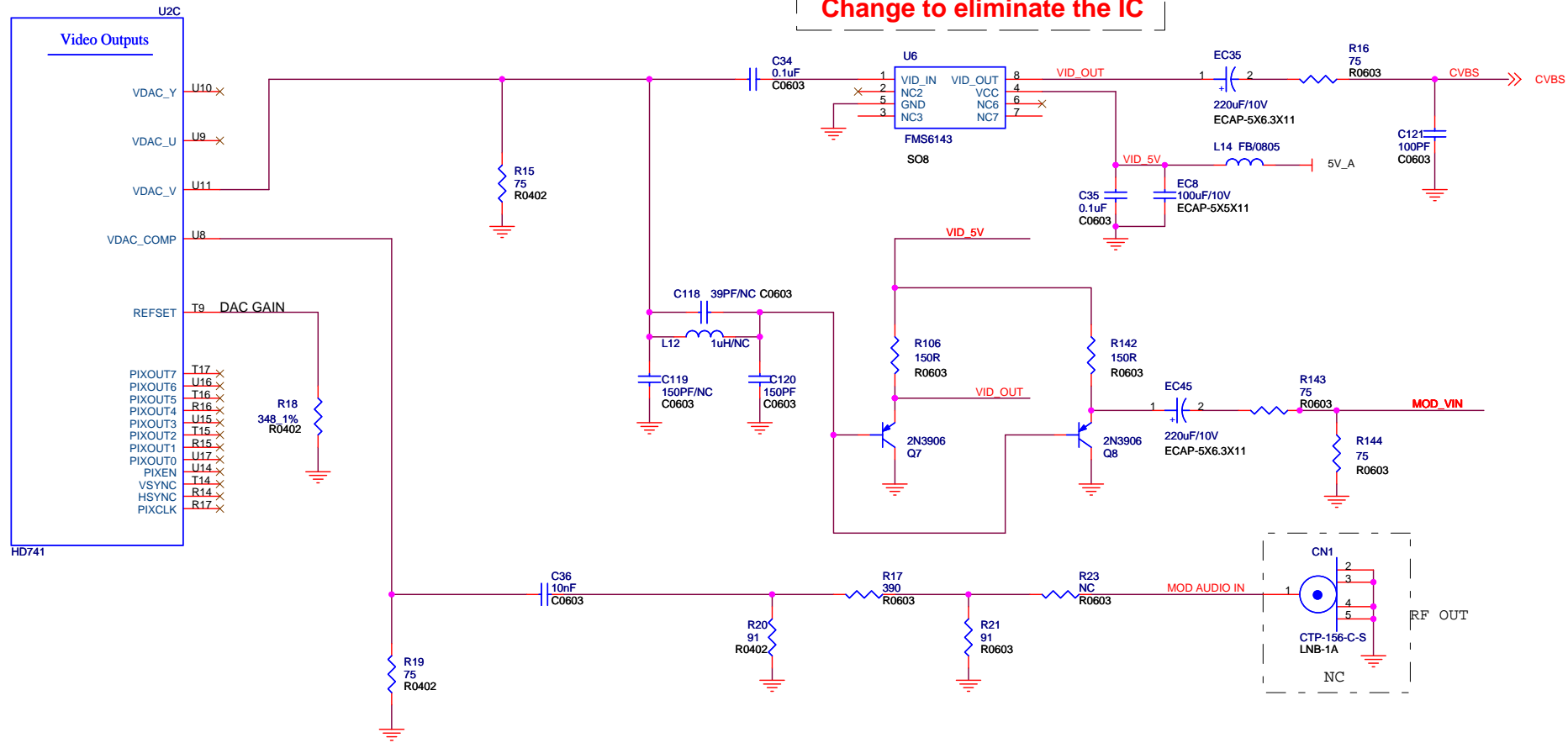
### Audio Outputs

DESIGN:	MODEL: AT2016(ZR39741)	TITLE: Audio Output
CHECKED:	PART NO.:	DWG NO: AT2016-YL01-01(A)
APPRD:	SHEET: 8 OF 11	VER: A

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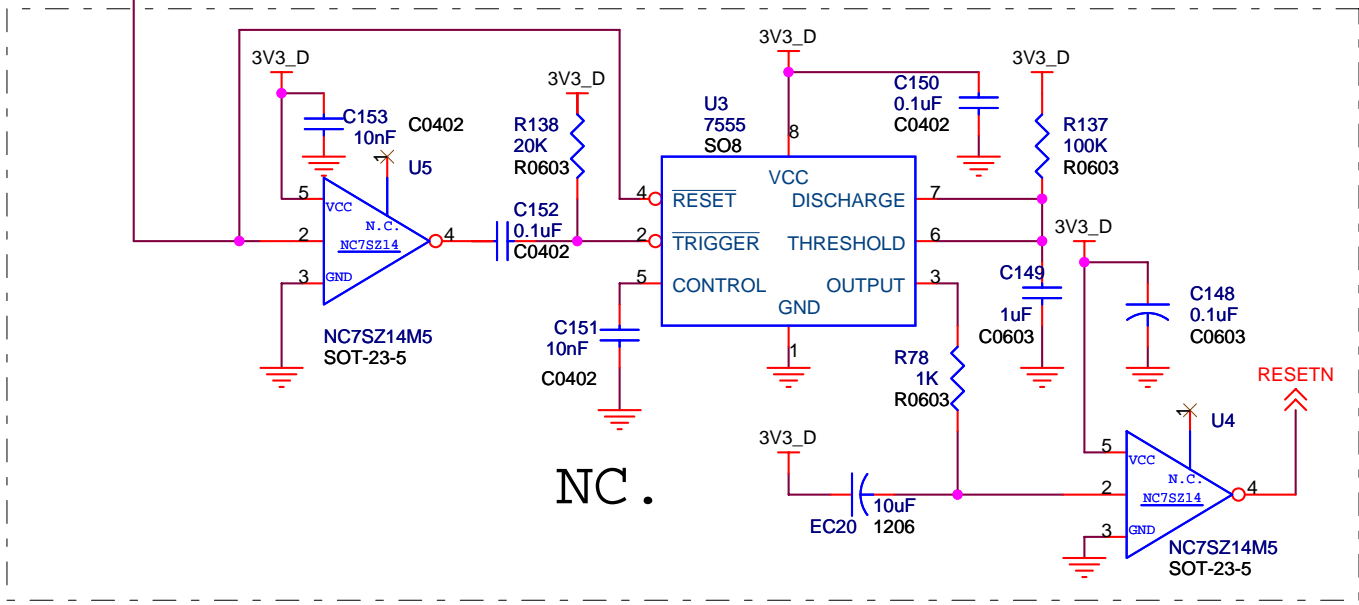
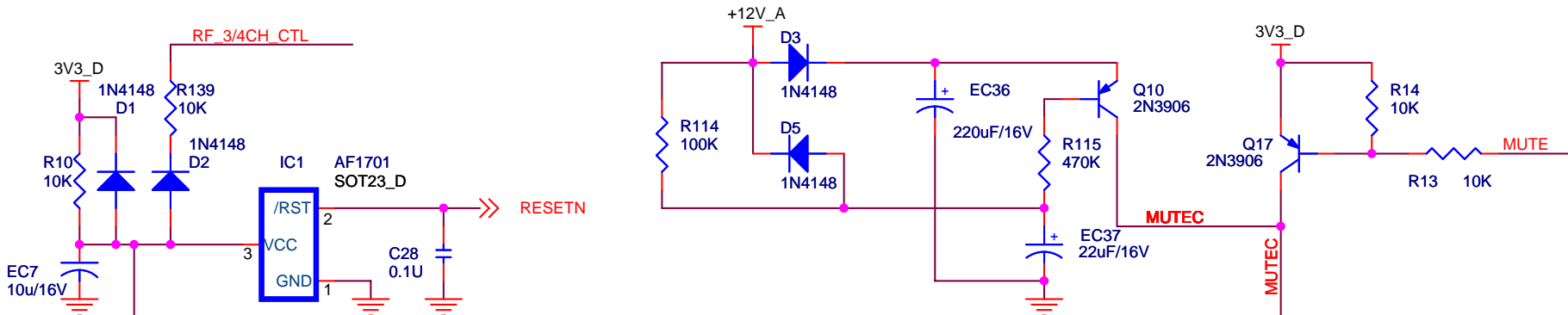


**Change to eliminate the IC**



**Video Output**

DESIGN:	MODEL: AT2016(ZR39741)	TITLE: Video Output
CHECKED:	PART NO.:	DWG NO: AT2016-YL01-01(A)
APPRD:	SHEET: 9 OF 11	VER: A
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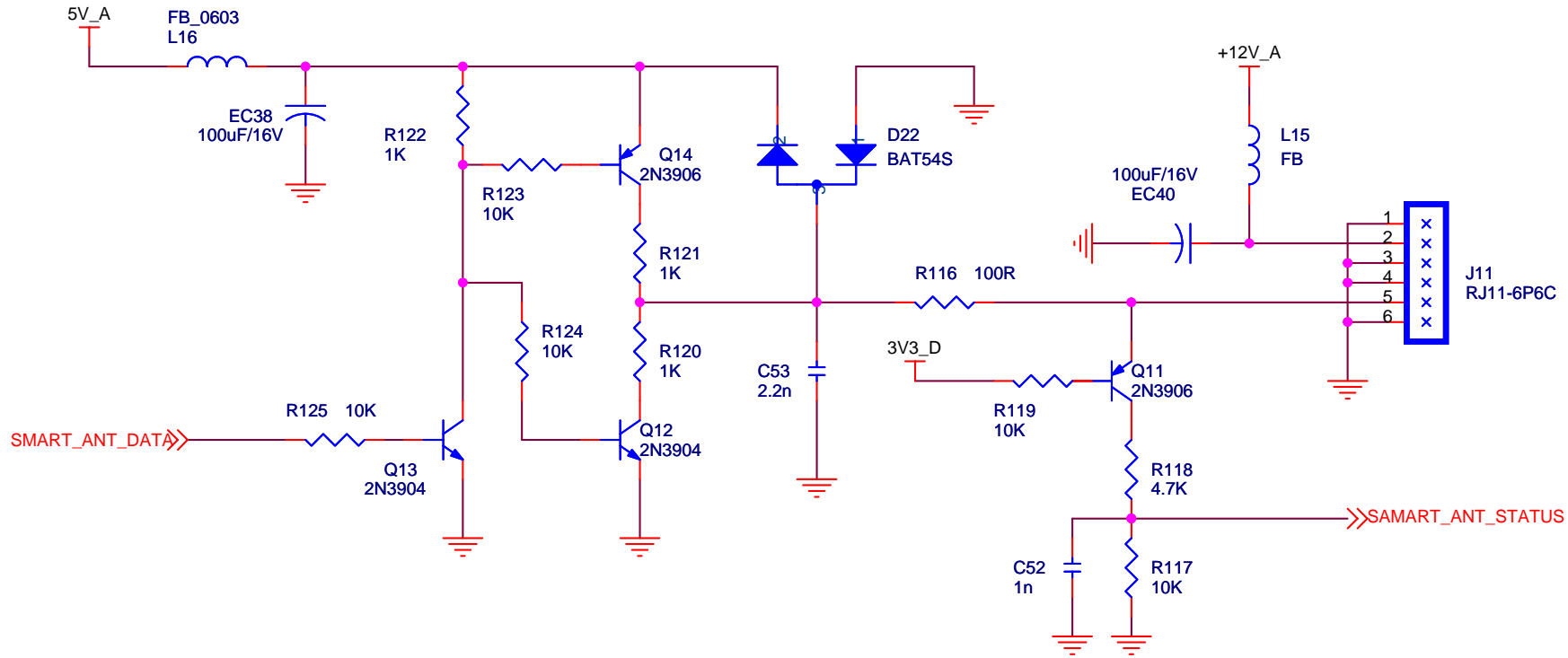


**POWER ON/OFF MUTE**

NC.

**Reset & MUTE**

DESIGN:	MODEL: AT2016(ZR39741)	TITLE: RESET & MUTE
CHECKED:	PART NO.:	DWG NO: AT2016-YL01-01(A)
APPRD:	SHEET: 10 OF 11	VER: A



- SMART ANTENNA I/F

DESIGN:	MODEL: AT2016(ZR39741)	TITLE: SMART ANTENNA
CHECKED:	PART NO.:	DWG NO: AT2016-YL01-01(A)
APPRD:	SHEET: 11 OF 11	VER: A