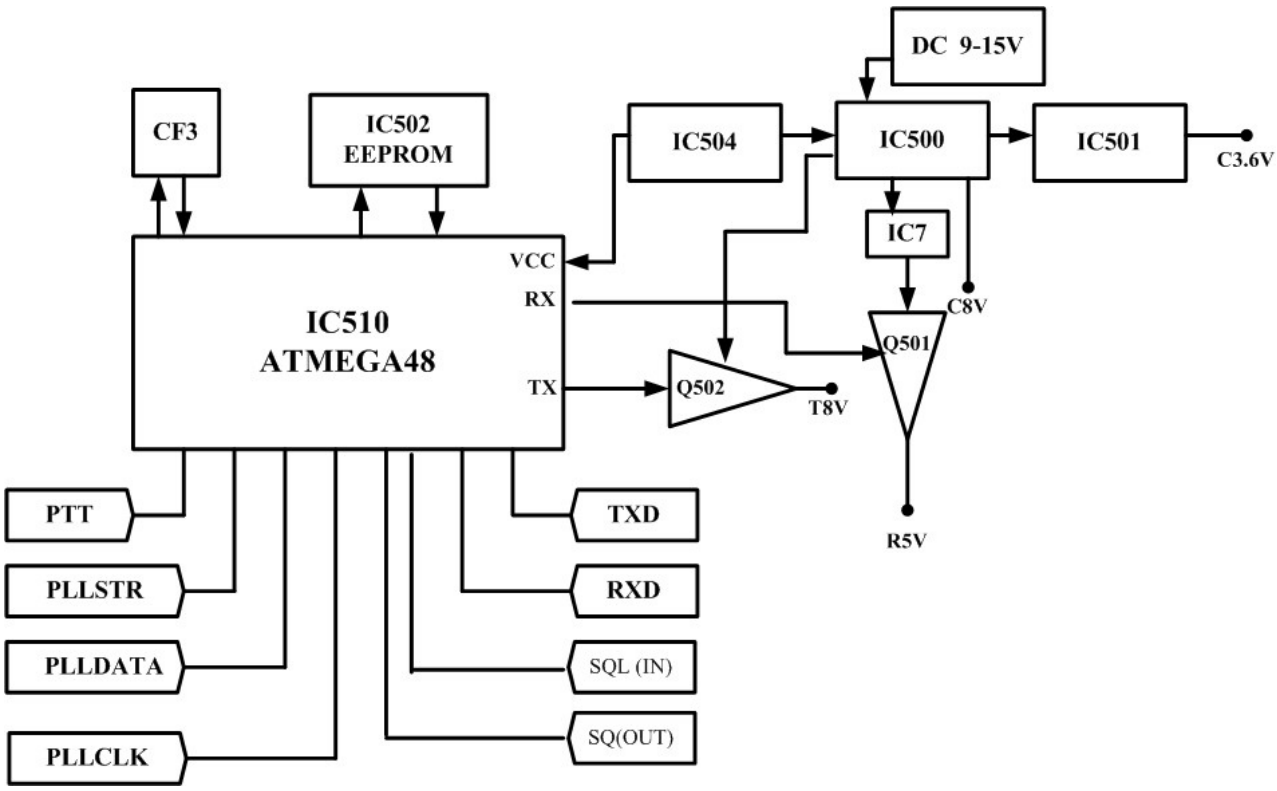
OPERATION DESCRIPTION

The Base Band signal circuits

It contains the CPU, power circuit ,TX signal circuit,RX signal circuit.

The CPU circuit and power circuit

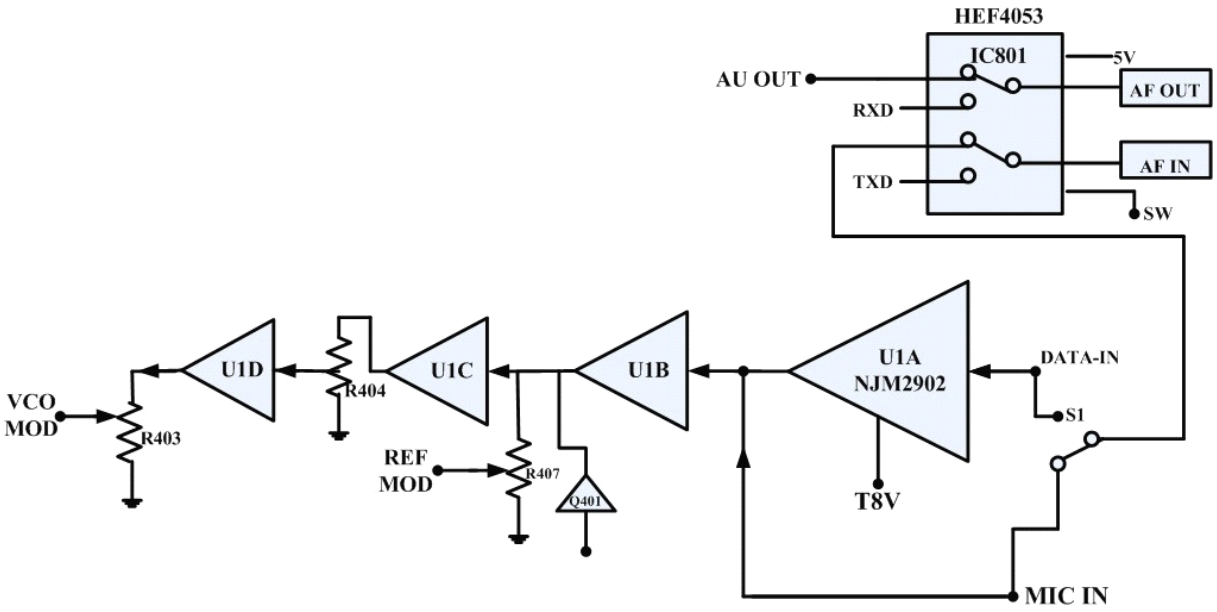


From Block Digram above: The DC power was regulated to 8 volt by IC500 ,and supplied to the RF part. IC504 convert 8 volt to 5volt and supply to IC510. Q500 is RX power supply switch, Q502 is TX power supply switch. IC501 supply 3.6V to PLL IC. Channels can be selected by the switch (CF3). IC510 controls digital frequency

synthesize by PLL STR ,PLL DATA and PLL CCK.

The CPU SQ pin detect the signal from PIN14 of IC2. when there is no receiveing signal, the input level is about 1.2V, and PIN8 of IC510 output high level(5V). When detect input receiving signal, the input level is about 0V, and PIN8 of IC510 output low level(5V).

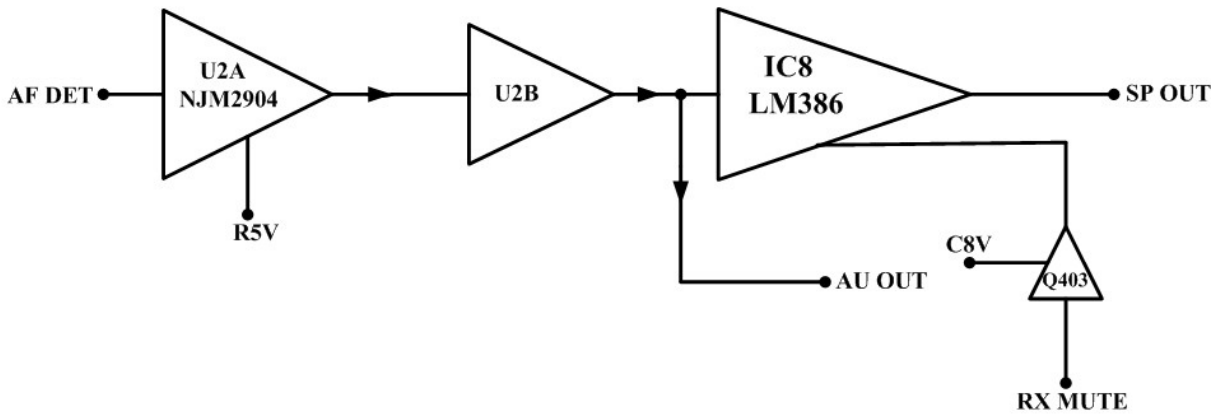
TX signal circuit



From the above Block Diagram : IC801 is audio/Data and UART signal switch. When the SW pin is high ,audio/data signal can go through IC801. S1 is a switch between audio and data input, when transmit audio, MIC IN port is shorted, when transmit data, DATA IN port is shorted. As it was data signal it will pass through

DATA-IN port and amplified by U1A, then it was coupling by C431 and pass to U1B for amplify again;as it was audio signal it will pass through MIC-IN port and amplified by U1B; then it will divide into two signal, one will coupling by C405 R407 and fed to TCXO for TX modulation; the other one was amplified by U1C,after coupling by C428,R404,C427 ;the voice signal is filtered by U1D which is a low pass filter, the output of U1D is then fed to VCO for TX modulation after coupling by C415,R403 again. Q401 is a Wideband /narrow-band switch .

RX signal circuit



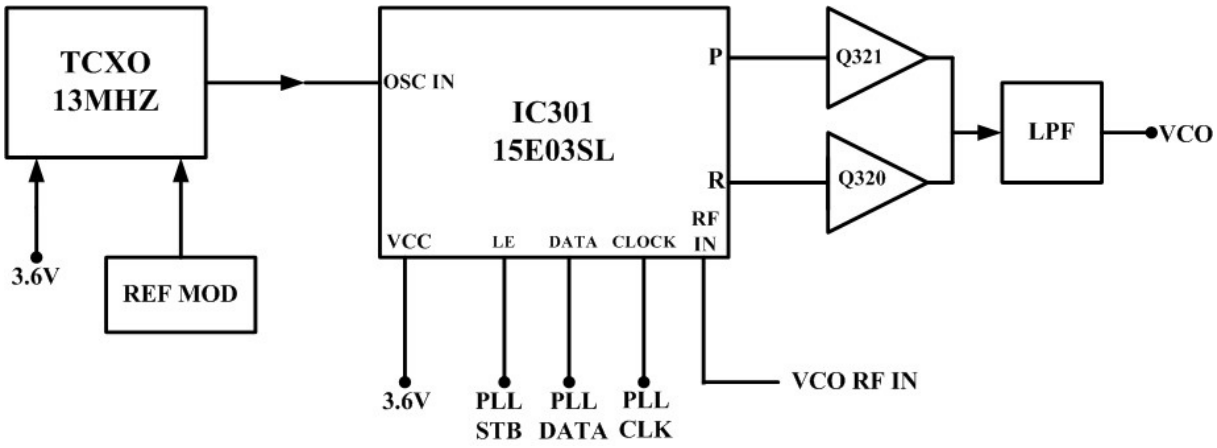
From the above Block Diagram; The resulting AF signal from IC2 enters base band processing chip U2. First coupling by C412 and amplified by U2A ,then it is filtered by U2B which is a low pass filter.After U2B,one signal pass through IC801 and send to COM pin

2, one signal is amplify by audio amplifierIC8, and sent to the horn directly. Q403 is a audio PA switch.

RF circuit

Main include PLL circuit / TX circuit /RX circuit

PLL Frequency Synthesizer



From the above Block Diagram : PLL circuit generates the first local oscillator signal for reception and RF signal for transmission.

1. PLL Circuit

Step frequency of PLL can be 5.0 KHz or 6.25 KHz. A 13MHz reference oscillator signal is divided at IC301 by a counter to generate a 5.0 KHz or 6.25 KHz reference frequency. Output signal

from VCO is buffer amplified by Q301 and divided at IC301 by a frequency divider. The divided signal is compared with 5.0 KHz or 6.25 KHz reference signal in the phase comparator of IC301. The output signal from phase comparator is filtered through a low pass filter(Q320/Q321/ R39/C328/R318/R31/C327/R316/C326) to generate a level D.C., and the level D.C. controls oscillator frequency by controlling VCO.

2. VCO

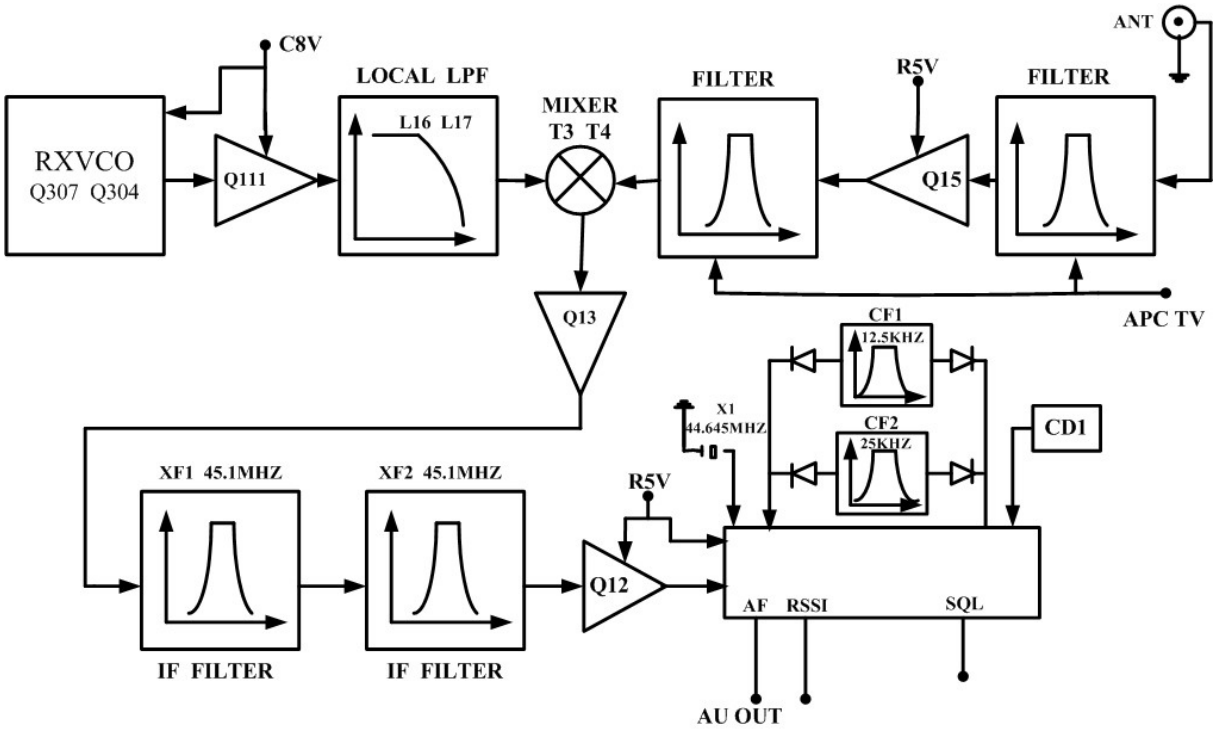
The operating frequency is generated by Q302 in transmit mode and by Q307 in receive mode. Operating frequency generate a control voltage by phase comparator to control varactor diodes so that the oscillator frequency is consistent with the MCU preset frequency(D301、D302、D303 and D304 in transmit mode, and D307、D308、D309 and D310 in receive mode). T/R pin is set high level in receive mode, and low level in transmit mode. The output from Q302 and Q307 is amplified by Q304 and sent to buffer amplifier.

3. Unlock Detector

An unlock condition appears if low level appears at MUXOUT pin

of IC301. Transmission is forbidden if this condition is detected by CPU IC510.

Receiver



The receiver utilizes double conversion superheterodyne (UHF)/(VHF).

1. **Front-end RF Amplifier**

The signal from antenna is amplified at LNA (Q15) after passing through a transmit/receive circuit and a band pass filter（D211/D212/D241/C264/C260/L25/L26）. Before passing the first mixer（T3、T4、TC3）, the amplified signal is filtered through another band pass filter（D208/D209/C240/C257/C258/L23/L24） to remove unwanted signals.

2. **First Mixer**

The signal from RF amplifier is mixed with the first local from PLL frequency synthesizer circuit at the fix mixer (T3、T4、TC3) to create a 45.1MHz first IF signal. The first IF signal is then amplified by Q13 and fed through a crystal filter (XF1) to further remove unwanted signals.

3. **IF Amplifier**

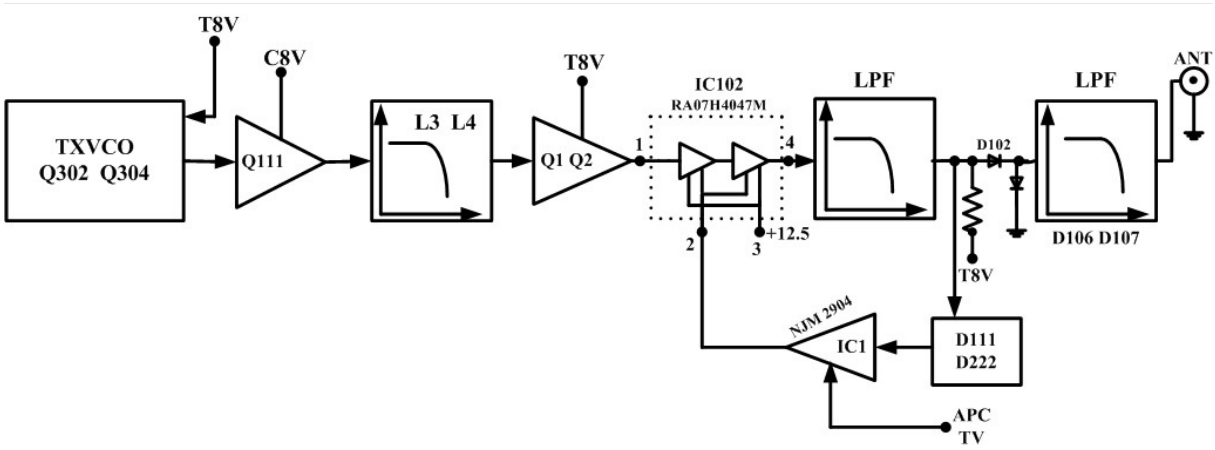
The first IF signal is amplified by Q13 before passing through crystal filter and by Q12 after crystal filter and then enters IF processing chip IC2. The signal from IC2 is mixed with the second

oscillator signal again in IC2 to create a 455 KHz second IF signal. The second IF signal then passes through a 455KHz ceramic filter (wideband: CF2， narrowband: CF1) to eliminate unwanted signals before it is amplified and detected in IC2.

4. Narrowband/Wideband Switch Circuit

Pin W/NCON of IC510 outputs narrowband (high level) and wideband (low level) controlling signal respectively to turn on corresponding diode-connector, and to choose ceramic filter CF2 (wideband) or CF1 (narrowband) to filter useless spurious signal.

Transmitter



1. RF Power Amplifier

The transmit signal from VCO buffer amplifier (Q304、Q111) is

amplified by Q1 and Q2. The amplified signal is then amplified by the power amplifier I102 to create 5.0W RF power.

2. Antenna Switch and LPF

Output signal from RF amplifier passes through a low-pass filter network and a transmit/receive switch circuit comprised of D102，D106 and D107 before it reaches the antenna terminal. D106 and D107 is turned on (conductive) in transmit mode and off (isolated) in receive mode.

3. APC

The automatic power control (APC) circuit stabilizes the transmit output power by detecting the forward and backward power of final stage amplifier. IC1 (2/2) compares the preset reference voltage with the voltage obtained from the regulated power signal. APC voltage is proportional to the forward and backward power. The output voltage controls the bias voltage of power amplifier module. The output power can be controlled by the software.