BGW211

IEEE 802.11b/g WLAN Chip

Rev. 02.02 — 18 October 2006 | Product data

1. Introduction

The BGW211 is a low power, "plug-and-play" System-in-Package (SiP) for 802.11b/g wireless LAN (WLAN), aimed at embedded and mobile applications.

The BGW211 comprises an ARM7TDMI microcontroller with SRAM (Static RAM) and ROM, an 802.11b/g compliant MAC and modem, a highly integrated RF transceiver, a linear power amplifier with internal power calibration, and an RF front end with integrated baluns, filters and switches. The power supply decoupling is fully incorporated in the BGW211, resulting in a low height, small form factor implementation of the complete 802.11b/g function, from SPI and SDIO Host interfaces to the RF antenna(s).

2. Features

General

- "Plug-and-play" IEEE Std 802.11b/g WLAN System-in-Package (SiP) with data rates up to 54 Mbit/sec
- Includes all the baseband and radio functionality, from Host interface up to antenna, needs only external antenna(s) and reference clocks
- Support for IEEE 802.11d automatic channel configuration, 802.11e[1] and WMM[1] Quality of Service enhancements, and 802.11i MAC Security enhancements
- Zero Host load – all WLAN functionality is implemented by the BGW211
- Small dimensions (10 x 15 x 1.25 mm) with an HLLGA 68-pin peripheral footprint
- Lead-free (Pb-free) and RoHS-compliant package
- Footprint compatible with the BGW200 802.11b SiP
- Operating temperature range: -30 to 85 °C
- Wide range of supported clock frequencies with built-in crystal oscillator or an external clock source (13, 19.2, 20, 26, 38.4 and 40 MHz)

[1] The PHY and MAC functionality implemented in the BGW211 is fully compliant with the relevant parts of the published IEEE 802.11 standard and further enhanced with changes detailed in the IEEE 802.11b/d/g/i published amendments. The MAC functionality has also been designed to support the soon to be published IEEE 802.11e amendment as well as the WMM standard. The flexible architecture should allow incorporation of any further changes to these amendments and proposed standards before ratification and publication.

founded by Philips

Power Management

- Supply voltage range:
  - Radio transceiver: 2.8 V to 2.9 V
  - Power amplifier: 2.8 V to 4.5 V
  - Baseband digital parts: 1.1 V to 1.3 V
  - Baseband analog parts: 2.8 V to 2.9 V
  - Baseband peripherals: 1.65 V to 3.6 V
- Low Power
  - Internal or external 32 kHz sleep clock
  - Sleep power consumption: 500 µW
  - Power save mode (300 ms beacon interval): 2 mW
  - 802.11b RX mode power consumption: 350 mW
  - 802.11b TX mode power consumption: 550 mW
  - 802.11g RX mode power consumption: 400 mW
  - 802.11g TX mode power consumption: 650 mW

Radio transceiver

- Fully compliant with IEEE 802.11b/g
- Receiver sensitivity (< 8% PER) at 11 Mbit/s data rate: -87 dBm
- Receiver sensitivity (< 10% PER) at 54 Mbit/s data rate: -74 dBm
- Blocking filter for suppression of GSM (-10 dBm) and DCS (-30 dBm) interfering signals
- Receiver antenna diversity fully supported
- Transmitter maximum output power in 802.11b mode: +17 dBm
- Transmitter maximum output power in 802.11g mode: +17 dBm

Baseband hardware

- IEEE 802.11b/g PHY and MAC
  - Implementation of low-level MAC functionality
  - Support for data rates up to 54 Mbits/s and all specified modulations
  - Direct-link support for mobile-to-mobile communication
  - Digital RX and TX filtering for adjacent channel rejection and spectrum shaping
  - Channel encoding and decoding hardware support
  - Fully digital synchronization (time, frequency, phase)
  - WEP, TKIP (Wi-Fi protected access) and AES-CCM encryption/decryption engine (Wi-Fi protected access 2) with support for 802.11i authentication protocol
- Bluetooth coexistence interface
  - Interfaces to a range of NXP Semiconductors Bluetooth modules
  - Hardware functionality to facilitate connection to 3rd party Bluetooth solutions
  - Hardware support for IEEE 802.15.2 Packet Traffic Arbitration recommendations
- Embedded ARM subsystem
  - ARM7TDMI-S RISC controller featuring low mW/MHz
  - Embedded non-volatile memory: 64 Kbytes of ROM
  - Embedded volatile memory: 128 Kbytes of RAM

- JTAG compliant in-circuit emulation interface

- Microcontroller peripherals:
  - SPI master/slave interface
  - SPI high-speed slave interface with DMA controller
  - SDIO interface with support for SPI, SD1 and SD4 modes
  - UART interface
  - I^2C interface

Software

- Microcontroller firmware
- IEEE 802.11b/g/e/i protocol firmware
- WPA, WPA2 (802.11i) and WMMv2 (802.11e including Scheduled Access) protocol firmware
- Host drivers for the following operating systems:
  - Pocket PC
  - Embedded Linux
  - Symbian
- Configuration utility

3. Applications

- IEEE 802.11b/g WLAN
- Smart Phone/Feature Phone with embedded WLAN
- Personal digital assistant (PDA) with embedded WLAN
- SDIO WLAN Network Interface Card (NIC)
- Voice over IP (VoIP) cordless phone
- Mobile gaming
- Portable Media Players including networked MP3 player
- Networked Digital Camera and Photo Frame
- Digital Media Adapter and Receiver
- Networked TV, Settop Box, DVD Recorder, PVR, Media Drive, and other consumer electronics appliances

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
BGW211EG	HLLGA68 (10 x 15)	Plastic laminate-based surface mount periphery package, 68 pins, Body 10 x 15 x 1.25 mm, weight: 418 mg, Pb and Halogen free	SOT858-1

5. Block diagram

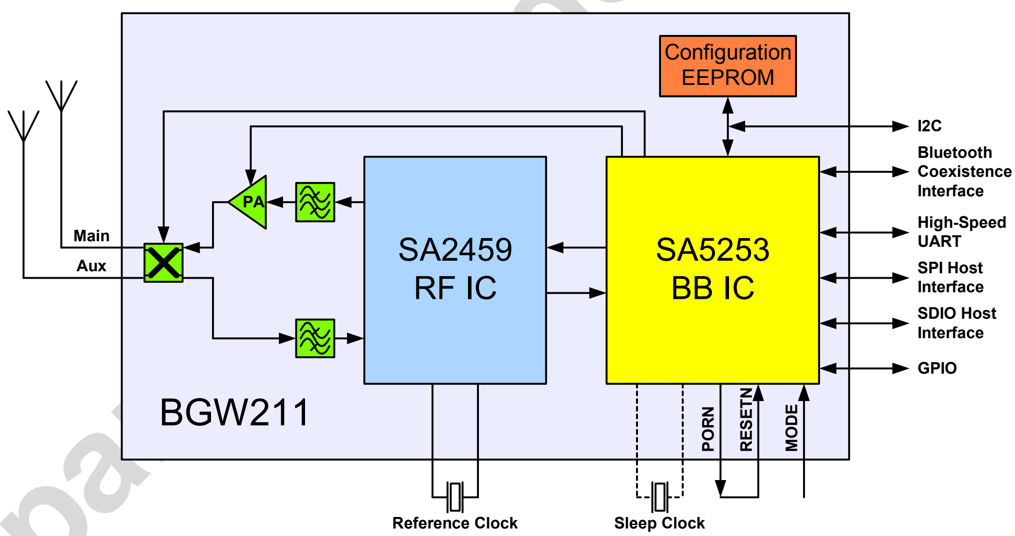


Fig 1. Block diagram

6. Pinning information

6.1 HLLGA68 package (SOT858-1)

6.1.1 Pinning

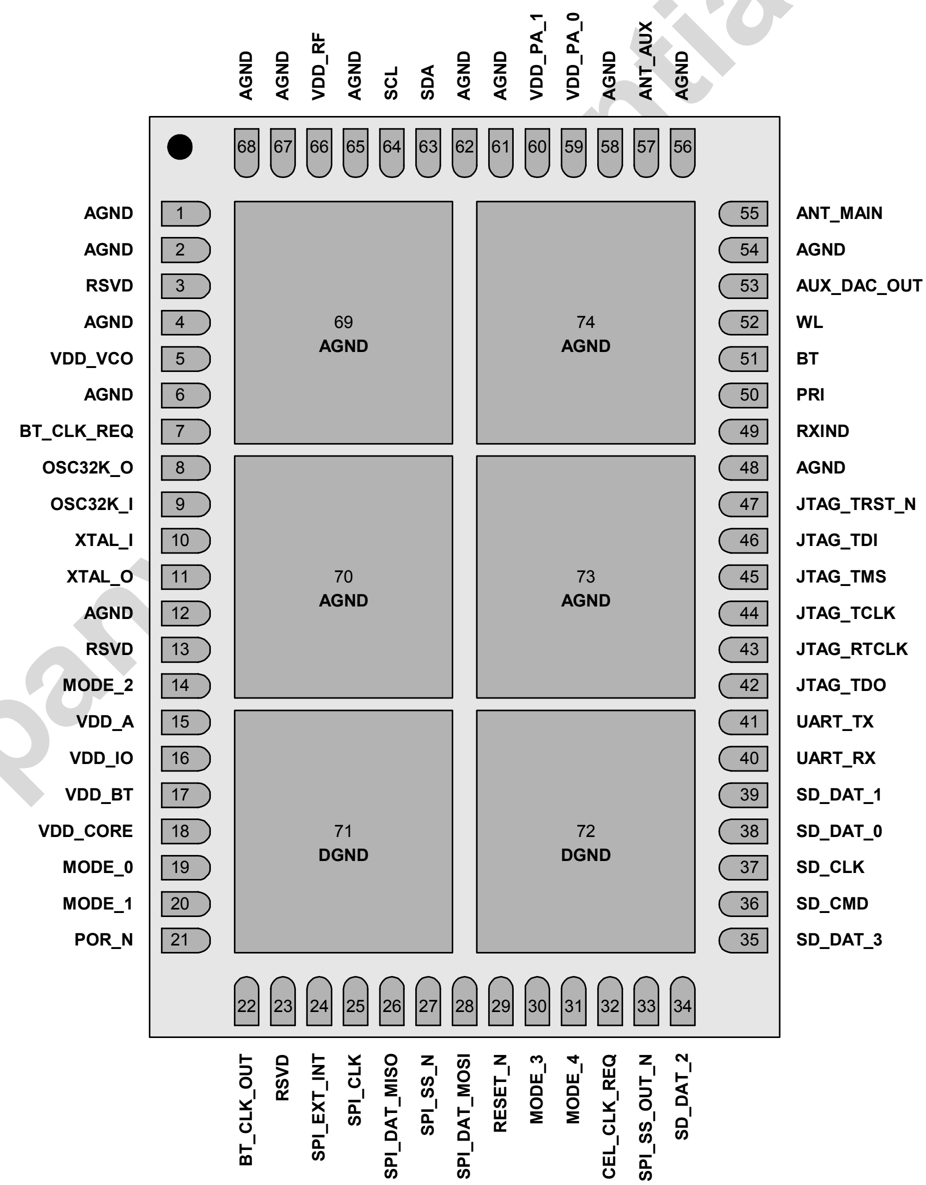


Fig 2. BGW211 pin configuration (top view)

6.1.2 Pin description

Table 2: Pin description

"Circuit" column: pu/pd = pull-up/pull-down; "Reset" column: I = input mode; pl = plain input; pu = pull-up; pd = pull-down;

Symbol	Pin	Type	Circuit	Reset	Supply	Description
SPI Interface						
SPI_CLK	25	I/O	digital I/O, 1 ns slew rate, programmable pu/pd	I pl	VDD_IO	SPI clock, bi-directional
SPI_SS_N	27	I/O	digital I/O, 3 ns slew rate, programmable pu/pd	I pl	VDD_IO	SPI slave select, input
SPI_EXT_INT	24	I/O	digital I/O, 1 ns slew rate, programmable pu/pd	I pl	VDD_IO	SPI external interrupt, output
SPI_DAT_MISO	26	I/O	digital I/O, 4 mA direct drive, programmable pu/pd	I pl	VDD_IO	SPI data (master in / slave out), bi-directional
SPI_DAT_MOSI	28	I/O	digital I/O, 1 ns slew rate, programmable pu/pd	I pl	VDD_IO	SPI data (master out / slave in), bi-directional
SPI_SS_OUT_N	33	I/O	digital I/O, 3 ns slew rate, programmable pu/pd	I pu	VDD_IO	SPI slave select
SDIO Interface						
SD_CLK	37	I/O	digital I/O, 1 ns slew rate, programmable pu/pd	I pl	VDD_IO	SD clock, input
SD_CMD	36	I/O	digital I/O, 1 ns slew rate, programmable pu/pd	I pl	VDD_IO	SD command, bi-directional
SD_DAT_0	38	I/O	digital I/O, 1 ns slew rate, programmable pu/pd	I pl	VDD_IO	SD data bit [0], bi-directional
SD_DAT_1	39	I/O	digital I/O, 1 ns slew rate, programmable pu/pd	I pl	VDD_IO	SD data bit [1], bi-directional
SD_DAT_2	34	I/O	digital I/O, 1 ns slew rate, programmable pu/pd	I pl	VDD_IO	SD data bit [2], bi-directional
SD_DAT_3	35	I/O	digital I/O, 1 ns slew rate, programmable pu/pd	I pl	VDD_IO	SD data bit [3], bi-directional
UART Interface						
UART_RX	40	I/O	digital I/O, 3 ns slew rate, programmable pu/pd	I pd	VDD_IO	Debug UART receive, input
UART_TX	41	I/O	digital I/O, 3 ns slew rate, programmable pu/pd	I pd	VDD_IO	Debug UART transmit, output
Antenna RF ports						
ANT_MAIN	55	I/O	RF I/O	—	—	RF main antenna port, 50 Ohm
ANT_AUX	57	I	RF input	—	—	RF auxiliary antenna port, 50 Ohm
Bluetooth coexistence interface						
WL	52	O	digital output, 3 ns slew rate, programmable pu/pd	I pd	VDD_BT	WLAN arbitration signal
BT	51	I	digital input, 3 ns slew rate, programmable pu/pd	I pd	VDD_BT	BT arbitration signal
PRI	50	I	digital input, 3 ns slew rate, programmable pu/pd	I pd	VDD_BT	BT high priority traffic indicator
RXIND	49	O	digital output, 3 ns slew rate, programmable pu/pd	I pd	VDD_BT	WLAN receive indicator

Table 2: Pin description *…continued*

"Circuit" column: pu/pd = pull-up/pull-down; "Reset" column: I = input mode; pl = plain input; pu = pull-up; pd = pull-down;

Symbol	Pin	Type	Circuit	Reset	Supply	Description
JTAG interface						
JTAG_TCLK	44	I	digital input, pull-down	—	VDD_IO	JTAG clock, input
JTAG_RTCLK	43	O	digital output, 4 mA direct drive	—	VDD_IO	Synchronized JTAG clock, output
JTAG_TMS	45	I	digital input, pull-up	—	VDD_IO	JTAG test mode select, input
JTAG_TRST_N	47	I	digital input, pull-down	—	VDD_IO	JTAG reset, input
JTAG_TDI	46	I	digital input, pull-up	—	VDD_IO	JTAG test data, input
JTAG_TDO	42	O	digital output, 4 mA direct drive	—	VDD_IO	JTAG test data, output
Miscellaneous						
XTAL_I	10	I	analog input	—	VDD_RF	Reference crystal oscillator, input
XTAL_O	11	O	analog output	—	VDD_RF	Reference crystal oscillator, output
CEL_CLK_REQ	32	I/O	digital I/O, 3 ns slew rate, programmable pu/pd	I pd	VDD_IO	Cellular reference clock request, output
OSC32K_I	9	I	analog input	—	VDD_CORE	32 kHz crystal oscillator, input
OSC32K_O	8	O	analog output	—	VDD_CORE	32 kHz crystal oscillator, output
RESET_N	29	I	digital input	—	VDD_IO	System reset, input
POR_N	21	O	digital output, 3 ns slew rate	—	VDD_IO	Power-on reset, output
MODE_0	19	I/O	digital I/O, 1 ns slew rate	I pl	VDD_IO	Boot mode selection, input
MODE_1	20	I/O	digital I/O, 1 ns slew rate	I pl	VDD_IO	Boot mode selection, input
MODE_2	14	I/O	digital I/O, 1 ns slew rate	I pl	VDD_IO	Boot mode selection, input
MODE_3	30	I/O	digital I/O, 1 ns slew rate	I pl	VDD_IO	Boot mode selection, input
MODE_4	31	I/O	digital I/O, 1 ns slew rate	I pl	VDD_IO	Boot mode selection, input
BT_CLK_REQ	7	I/O	digital I/O, 3 ns slew rate, programmable pu/pd	I pd	VDD_IO	Bluetooth reference clock request, input
AUX_DAC_OUT	53	O	analog output	—	AVDD	Auxiliary DAC, output
SDA	63	I/O	digital I/O, 3 ns slew rate, programmable pull-up	I pu	VDD_IO	I2C interface data line
SCL	64	I/O	digital I/O, 3 ns slew rate, programmable pull-up	I pu	VDD_IO	I2C interface clock line
BT_CLK_OUT	22	I/O	digital I/O, 1 ns slew rate	I pl	VDD_IO	Bluetooth reference clock, output

Table 2: Pin description *...continued*

"Circuit" column: pu/pd = pull-up/pull-down; "Reset" column: I = input mode; pl = plain input; pu = pull-up; pd = pull-down;

Symbol	Pin	Type	Circuit	Reset	Supply	Description
Power supply						
VDD_VCO	5	—	—	—	—	VCO analog supply voltage
VDD_A	15	—	—	—	—	Analog supply voltage
VDD_IO	16	—	—	—	—	I/O digital supply voltage
VDD_BT	17	—	—	—	—	Bluetooth digital supply voltage
VDD_CORE	18	—	—	—	—	Core digital supply voltage
VDD_PA_0	59	—	—	—	—	PA analog supply voltage
VDD_PA_1	60	—	—	—	—	PA analog supply voltage
VDD_RF	66	—	—	—	—	RF IC analog supply voltage
AGND	1	—	—	—	—	Analog ground
AGND	2	—	—	—	—	Analog ground
AGND	4	—	—	—	—	Analog ground
AGND	6	—	—	—	—	Analog ground
AGND	12	—	—	—	—	Analog ground
AGND	48	—	—	—	—	Analog ground
AGND	54	—	—	—	—	Analog ground
AGND	56	—	—	—	—	Analog ground
AGND	58	—	—	—	—	Analog ground
AGND	61	—	—	—	—	Analog ground
AGND	62	—	—	—	—	Analog ground
AGND	65	—	—	—	—	Analog ground
AGND	67	—	—	—	—	Analog ground
AGND	68	—	—	—	—	Analog ground
AGND	69	—	—	—	—	Analog ground
AGND	70	—	—	—	—	Analog ground
DGND	71	—	—	—	—	Digital ground
DGND	72	—	—	—	—	Digital ground
AGND	73	—	—	—	—	Analog ground
AGND	74	—	—	—	—	Analog ground
RSVD	3	—	—	—	—	Reserved, do not connect
RSVD	13	—	—	—	—	Reserved, do not connect
RSVD	23	—	—	—	—	Reserved, connect to ground

7. Functional description

7.1 Overview

The BGW211 combines the IEEE 802.11b/g RF transceiver, IEEE 802.11b/g MAC, IEEE 802.11b/g compliant modem, an ARM7TDMI-S microcontroller, embedded memory, interface circuits, and power management in one SiP with embedded software. Together with an antenna and a reference clock, this device forms a complete WLAN solution. The system architecture is ideal for mobile products and requires no load on the Host processor. The Host system can be in sleep mode while the BGW211 WLAN solution processes beacons from the Access Point and then determines to wake up the Host, if appropriate. This allows for very low system power consumption in standby mode.

The BGW211 is designed to be used for 802.11g wireless links, operating in the globally available ISM band, between 2412 and 2484 MHz. The radio is a low power, fully integrated, zero-IF transceiver. The low noise receiver has a dedicated digital gain control with 90 dB dynamic range in 3 dB steps with integrated channel filters and DC offset cancellation. The frequency generation comprises an integrated RF VCO with supply voltage regulator, a sigma-delta fractional-N synthesizer and an integrated low power crystal oscillator with an external crystal. The transmitter chain has integrated reconstruction filters and a sliding bias driver amplifier with 20 dB gain control in 1 dB steps. The power amplifier is a highly linear InGaP HBT MMIC with 32 dB small signal gain. The advanced bias control and compensation circuitry together with production calibration data stored on the internal EEPROM ensures stable performance over a wide temperature range. The RX/TX and antenna diversity switching is done by a low loss pHEMT GaAs DPDT switch with high linearity and isolation. The BGW211 SiP integrates the radio front-end components on a low cost organic substrate together with the radio supply decoupling. The device is a “plug-and-play” SiP whose robust design requires no manufacturing trimming resulting in a cost optimized solution. The RF antenna ports have a normalized 50W impedance and each can be connected directly to an external 50W matched antenna.

The 802.11b/g baseband consists of the 4 main subsystems. An ARM subsystem (EAS) containing the ARM7TDMI core and an I/O subsystem which is responsible for processing the non-real-time parts of the WLAN protocol and interfacing to the Host processor via the SDIO or SPI2 interface. A MAC subsystem has a RISC processor for processing the real-time portion of the WLAN protocol and a Data Flow Controller (DFC) which interfaces with the ARM protocol processor and the DSP core. A DSP subsystem (PHY) uses the OnDSP core and is responsible for physical layer processing of the IEEE 802.11b/g protocol. A South Subsystem (SSS) contains supporting peripheral units such as the clock generation, a timer, a memory block, debug facilities and the general purpose I/O lines.

The BGW211 supports two Host interfaces. The high speed SPI slave (SPI2) interface is ideal for embedded applications since only 5 signal lines are required to connect to the Host controller and the protocol for this interface has a low processing overhead. The SDIO interface can operate in SPI, SD1, and SD4 modes and can be used in an embedded application or in a Secure Digital NIC card. Fig. 3 shows the Host interface mapping for the BGW211.

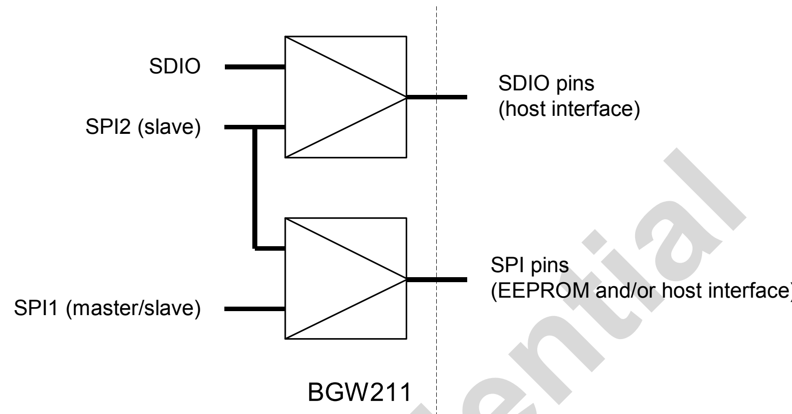


Fig 3. Host interface mapping

The BGW211 is designed to be used as a low-cost, low-power wireless LAN station. Existing WLAN solutions, aimed at the computing market, have made use of the Host processor to implement such functions as fragmentation/defragmentation. The BGW211 implements all WLAN functions internally (implemented in either hardware or firmware) with the result that there is no processing load on the Host controller. This link will be the basis for smart phones and PDAs to communicate with a LAN network through a WLAN access point both for voice (VoIP) and data access as well as for gaming and other portable consumer applications.

8. SA2459 2.4 GHz direct-conversion WLAN transceiver IC

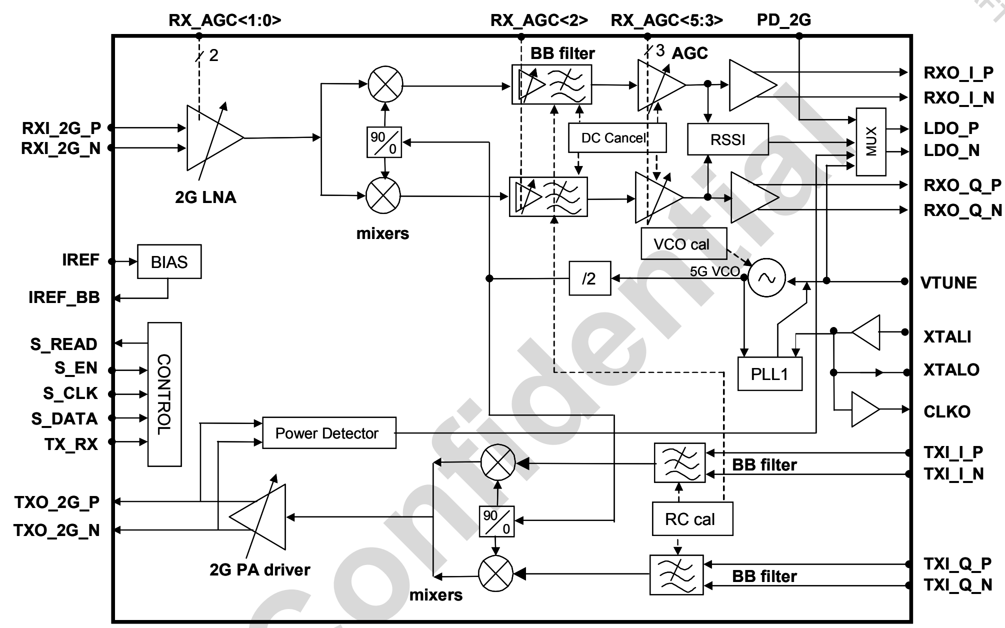


Fig 4. SA2459 block diagram

8.1 Receiver

The receiver front end contains a dedicated differential low noise amplifier (LNA) and I/Q demodulator tuned for 2.4 - 2.5 GHz. The front-end has three gain modes with fast switching.

The receiver analog filter for OFDM signals is a fourth order elliptic filter, which provides more than 57 dB rejection at 32 MHz offset. For CCK signals, a fifth order Butterworth filter provides more than 47 dB rejection at 20 MHz offset. The high dynamic range of the filter fulfils the 802.11b/g specifications. The filter section provides two gain settings.

The receiver baseband variable gain amplifier (VGA) has a 21 dB gain range with a 3 dB step.

8.2 Transmitter

The transmitter analog reconstructive filter is scalable with the DAC sample frequency. A third order filter provides more then 45 dB rejection at 70 MHz offset, or a fourth order filter provides more than 45 dB rejection at 40 MHz offset.

The transmitter I/Q modulator is a single sideband modulator with high linearity, low carrier leakage, and more than 30 dB sideband suppression after calibration.

The transmitter RF VGA has 20 dB gain range with 1 dB step size. The linear output power is -12 dBm in the 2.4 GHz band.

8.3 Frequency generation

The 5 GHz VCO is fully integrated with a self-calibration loop. The integrated supply voltage minimizes frequency pushing to less than 1 MHz/V. The dividers and quadrature generators are integrated on-chip. The LO phase noise is better than -95 dBc/Hz at 100 kHz offset.

The high performance ΣΔ fractional-N frequency synthesizer allows the SA2459 to synthesize the VCO frequency. The programmable integer N ratio has a fractional resolution of 22 programmable bits. The very low close-in phase noise allows a wider PLL loop bandwidth for shorter settling times. The VCO frequency is divided down to 40 MHz via the programmable divider (9.53 Hz LO frequency step programmability at 40 MHz reference) and then compared in a phase/frequency detector (PFD) with a 40 MHz reference clock. The phase error information is fed back to the VCO via the charge pump and integrated loop filter.

An amplifier is integrated to build a crystal oscillator. Externally, only a crystal and a few passive components are required. An external reference clock can also be applied to pin XTAL_I (see section 16.1).

9. SA5253 802.11b/g low-power baseband IC

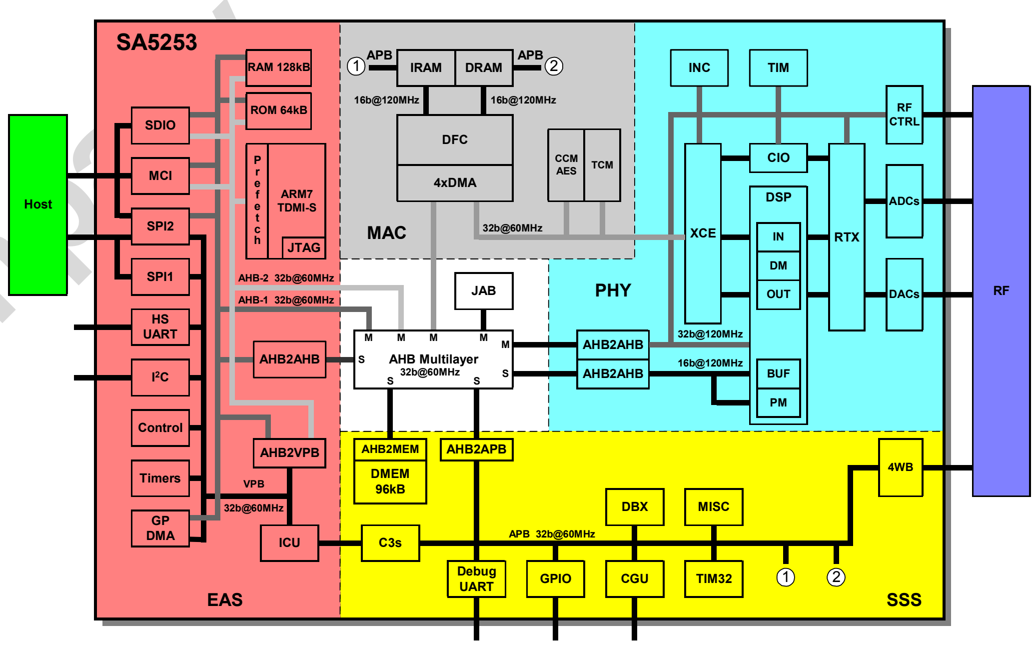


Fig 5. SA5253 block diagram

The SA5253 consists of the following high-level blocks:

- An ARM subsystem (EAS) that contains the ARM7TDMI core and an I/O subsystem. The ARM subsystem is responsible for processing the WLAN non-real-time part of the protocol as well as interfacing to a Host processor via SDIO, SPI2, or MCI interface.
- A subsystem (MAC) including a RISC processor, also known as Data Flow Controller (DFC), that includes encryption and decryption co-processing engines, and a DMA engine with four independent channels. The DFC subsystem interfaces with the ARM protocol processor and the DSP core. The RISC processor is responsible for processing the real-time portion of the wireless LAN protocol.
- A DSP subsystem (PHY) that uses the OnDSP core, and is responsible for physical layer processing (PHY) of the IEEE 802.11b/g protocol. The DSP controls a channel encoding engine (XCE), a filtering block (RTX), and interfaces to the DFC via a mailbox, interrupts, and the XCE block. In addition, it interfaces to the RF chip.
  In addition, the PHY block contains a mixed signal block that includes analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The SA5253 contains two 9-bit ADCs for 40 MHz IQ sampling of the baseband signal provided by the RF chip, specifically of OFDM signals. An RX decimation filter bypass option is implemented to also allow for 20 MHz IQ. A third 9-bit ADC is used for supporting RF calibration and RF measurements. Two 10-bit DACs are used for outputting a baseband signal to the RF chip with a sample rate of 80 MHz. Furthermore, one control DAC is provided for PA bias control.
- A South Subsystem (SSS), containing supporting peripheral units such as the clock generation unit, a timer, a memory block, and debug facilities. In addition, it provides a number of general purpose I/O lines.

In the following, each of the four blocks and their individual units are described in more detail.

9.1 Embedded ARM subsystem - EAS

The EAS subsystem includes the following major components, each described in the following sections:

- ARM Processor with Instruction Memories
- Secure Digital I/O Interface (SDIO)
- Microcontroller Interface (MCI)
- SPI2 Interface
- SPI1 Interface
- High-Speed UART (HSUART)
- I2C Interface (I2C)
- Control Unit (CTRL)
- Timer Unit (TIM)
- General Purpose DMA Unit (GPDMA)

9.1.1 ARM Processor

The SA5253 contains an ARM7TDMI-S RISC core, which is today considered as the standard RISC processor in the telecom industry. This processor is characterized by its extremely low mW/MIPS ratio.

On-chip memories eliminate the need for external SRAM, reducing pin count and system power consumption, while system performance is increased. The SA5253 incorporates 128 kbytes of Instruction RAM and 64 kbytes of Instruction ROM.

The ARM processor handles the communication with the Host via the various possible interfaces, and performs extensive portions of the IEEE 802.11 MAC firmware, reducing the Host overhead to zero. In addition, it handles configuration and control of the MAC, PHY, and SSS blocks.

The EAS subsystem employs two high performance AHB buses for optimized throughput. AHB1 is a multimaster bus used for DMA transfers. AHB2 is a single-master bus used by the ARM processor. A bridge connects the AHB1 bus to the VBP bus, which connects to the lower speed peripherals.

A JTAG compliant interface facilitates ARM7 in-circuit emulation.

9.1.2 Secure Digital Interface - SDIO

The Secure Digital I/O interface has the following features:

- Compliant with SDIO standard
- Supports SPI, SD1 and SD4 modes
- DMA controller
- 8 Mailbox registers (4 Master-to-Slave (M2S) and 4 Slave-to-Master (S2M))
- 9 scratch registers (5 Master-to-Slave (M2S) and 4 Slave-to-Master (S2M))

The SDIO interface of the SA5253 is intended for use as a Host interface. The SDIO clock is independent of the bus clock (no over-sampling) and has a maximum operating frequency of 25 MHz. Most operations are handled by the SDIO block hardware. The role of the SA5253 firmware is to handle interrupts and to specify the location of the DMA data in SA5253 memory.

Eight mailboxes are provided. Four of these are dedicated for the Host to pass information to the SA5253 (M2S). When the Host writes to one of these mailboxes, an interrupt is generated in the SA5253. The remaining four mailboxes are dedicated for the SA5253 to pass information to the Host (S2M). An SDIO interrupt is generated when the SA5253 writes to one of these mailboxes.

Nine scratch registers are provided, five for the Host (M2S) and four for the SA5253 (S2M). These registers are similar to the mailbox registers except that no interrupts are generated when the registers are written.

9.1.3 Microcontroller Interface - MCI

This interface is not connected in the BGW211.

9.1.4 High-Speed Slave Serial Peripheral Interface - SPI2

The serial SPI2 interface of the SA5253 is a high-speed SPI slave interface intended for use as a Host interface. The SPI clock is independent of the bus clock (no over-sampling) and has a maximum operating frequency of 60 MHz. The SPI2 interface has the following features:

- SPI mode 3 slave interface
- Up to 60 Mbit/sec data transfer rate
- 8-bit minimum packet length
- Half duplex operation
- DMA controller
- 8 Mailbox registers (4 Master-to-Slave (M2S) and 4 Slave-to-Master (S2M))
- 9 scratch registers (5 Master-to-Slave (M2S) and 4 Slave-to-Master (S2M))
- Low overhead link protocol
- External signal for interrupting SPI master

9.1.5 Master/Slave Serial Peripheral Interface - SPI1

The Master/Slave SPI interface SPI1 can be configured to work with most SPI master or slave devices. Clock frequency, polarity and phase are configurable by firmware, as is the data bit order (LSB first or MSB first). The SPI1 interface has the following features:

- Master or slave mode operation
- SPI mode 0 and 3 supported in both master and slave modes
- Programmable clock frequency up to 7.5 MHz
- Automatic error checking: write collision, read overrun, mode fault and slave abort

The SPI clock is over-sampled by a factor of 8. The maximum SPI clock frequency is therefore limited to 1/8 of the bus clock.

9.1.6 High-Speed Universal Asynchronous Receiver/Transmitter (HS-UART)

This interface is not connected in the BGW211.

9.1.7 I2C Interface (I2C)

The I2C interface enables the use of external I2C EPROMs and is intended to control an external Power Management Unit (PMU). For these two uses, the I2C interface provides multi-slave capabilities.

The I2C interface has built-in pull-up devices as specified in Table 7. Their pull-up capability is sufficient for communication with the internal I2C EEPROM. If more I2C slave devices are connected externally, additional pull-up resistors should be applied as described in the I2C bus specification.

9.1.8 Control Unit (CTRL)

This block contains several registers for clock gating, power-down control, pull-up/pull-down pad mode selection, SPI control, and some further control functions.

9.1.9 System Timer Unit (TIM)

The SA5253 contains five general-purpose timers and a watchdog timer (WDT). Timers 0, 1, 3, and 4 can be programmed with a start value. Operation can be either single shot or continuous. An interrupt is generated when a timer counts down to zero. Timer 2 is programmed with up to four interrupt compare values. An interrupt is generated when the counter value matches one of the interrupt compare values. Operation can be either single shot or continuous.

The Watchdog timer provides a mechanism to reset the SA5253 if for some reason the firmware becomes locked. A start value is programmed from which the counter counts down to zero. For correct operation of the SA5253, the firmware must reset the start value before it gets to zero. If the counter reaches zero, the SA5253 is reset. An interrupt compare value can be programmed, allowing a warning to be generated prior to the full reset.

9.1.10 General Purpose DMA Unit (GPDMA)

The general purpose DMA engine can be used to move data from one memory location to another with minimal firmware involvement. Uses of the block include fragmentation and defragmentation assistance.

9.2 MAC subsystem - MAC

The MAC subsystem includes a RISC processor, the Data Flow Controller (DFC) with instruction and data memories, encryption and decryption co-processing engines, and a DMA engine with four independent channels. The DFC subsystem interfaces with the ARM protocol processor and the DSP core. The DFC RISC processor is responsible for processing the real-time portion of the wireless LAN protocol.

9.2.1 DFC RISC Controller

The central part of the Data Flow Controller (DFC) is a 16-bit RISC micro-controller core. This controller is a pipelined machine with a 16-bit instruction set, consisting of 53 instructions. Up to 32 general purpose registers are available. A Register Base Pointer facilitates the use of register banks with up to 8 registers, and enables quick context switching for interrupts. The register banks can be freely stored in the Data RAM.

The organization of the Data RAM (DRAM) of the DFC is 128 x 16 bit. Besides being used by the RISC controller, the Data RAM can be accessed by the DMA Engine of the DFC or the APB bus.

The organization of the Instruction RAM (IRAM) of the DFC is 6 K x 16 bit, thus storing up to 6 K instructions. The instruction RAM can be used by the DMA Engine of the DFC, the RISC (for instruction fetching), and the APB bus. This enables loading of program code, which is provided either by the external Host or via the serial interfaces.

9.2.2 DMA Engine

The DMA Engine of the DFC contains four independent DMA channels. The DMA channels connect the AHB Multilayer unit as a master to the TCM and CCM modules of the MAC block, and to the XCE module of the PHY block. The user can program the source and target address, the transfer length, and the mode of operation of each of the channels individually.

The DMA Engine implements simple DMA channels that transfer a number of 16-bit aligned words from a programmed source address to the programmed destination address.

For synchronized DMA operations, channels 0 & 2 and/or channels 1 & 3 can be programmed to operate in a synchronous mode.

9.2.3 Advanced Encryption Standard (AES) / Cipher Block Chaining Message Authentication Code - CCM

The CCM module implements the Advanced Encryption Standard (AES) algorithm and the Counter Mode with CBC-MAC (CCM) algorithm. AES is a block cipher, and CCM is the mode of operation for AES specified in IEEE 802.11i standard. Its features are:

- Counter Mode with CBC-MAC (CCM) algorithm support as specified in the IEEE 802.11i standard
- Advanced Encryption Standard (AES) algorithm support
- 32-bit AHB interface, and three interrupt outputs

The CCM consists of the controller, the data path, and the data buffer.

In order to provide a high degree of flexibility and adaptability to changing standards, the CCM support is broken down into several programmable steps. The programmer has full control over the composition of the data and the number of AES encryption steps used for the MIC initialization. The programmer also defines the composition of the CCM counter. After each MIC initialization step, the current value of the MIC can be read and/or written to. This allows the programmer to interrupt the ongoing operation (e.g. in TX mode), start another one (e.g. in RX mode), and later resume the interrupted operation.

9.2.4 TKIP/CKIP Module - TCM

The TCM Module combines the TKIP and CKIP functionality. It supports the following features:

- WEP encryption/decryption
- Michael calculation with automated appending/checking of the MIC.
- TKIP key permutation
- CKIP key permutation.
- CCX calculation, which incorporates an AES engine.

The keys for WEP can be calculated by the key permutation engine. Full read/write access to the key output register via AHB is provided, so the key can also be written directly without involving the key permutation block. If different connections are to be

serviced, the complete Michael state can be saved and restored. After decryption operations, the status of the last Michael MIC and ICV comparison can also be checked in the status/instruction register.

CKIP and TKIP operations can be started independently from each other through separate instruction registers. A bypass mode is provided - the data is passed from the input to the output FIFO without WEP operation. This can be used for (de-) fragmentation of unencrypted frames.

The CKIP key permutation takes approximately 16 cycles, while the TKIP key permutation takes approximately 55 cycles.

9.3 Physical Layer Subsystem - PHY

The PHY subsystem includes the following major components:

- DSP-300
- XCE (Channel Coder/Decoder, including Viterbi Decoder and Equalizer)
- RTX (Receive/Transmit Filter Unit)
- CIO (Central I/O Unit, controlling access to the IN/OUT-RAMs of the DSP)
- TIM (Timer Module for DSP)
- INC (Interrupt Controller for DSP)
- RFCTRL (GPIO Control Unit for RF control pins)
- Mixed Signal Block with ADCs and DACs

9.3.1 DSP-300 Core

The DSP-300 core uses a Single Instruction, Multiple Data (SIMD) set, and is based on NXP's patented Tagged Very Long Instruction Word (TVLIW) architecture. The DSP-300 core performs the following functions for the transmit branch:

- Symbol mapping
- OFDM symbol mapping
- Inverse FFT (IFFT)
- Control processing
- RF Front End control

The DSP-300 core performs the following functions for the receiver branch:

- Synchronization (time, frequency, phase)
- FFT
- OFDM symbol demapping
- Soft demapping
- Channel equalization
- Control processing
- RF Front End control

9.3.2 XCE Module

Channel encoding and decoding is performed outside the DSP-300 in peripheral units that are connected to the DSP-300 core by dual-ported memories for user data exchange. The XCE interfaces also to the AHB buses of DFC and DSP.

The units of the XCE Module are divided into three major groups:

- Units for OFDM channel encoding (802.11g)
- Units for OFDM channel decoding (802.11g)
- Units for CCK and DSSS decoding (802.11b)

Each of these functional units has separate clock trees that can be switched on or off to save power when a unit is not in use. The units can be configured by the DSP through control registers that can be written and read via the DSP AHB bus. All control data is double buffered, which enables the programmer to reconfigure the peripheral while it is still operating on current data.

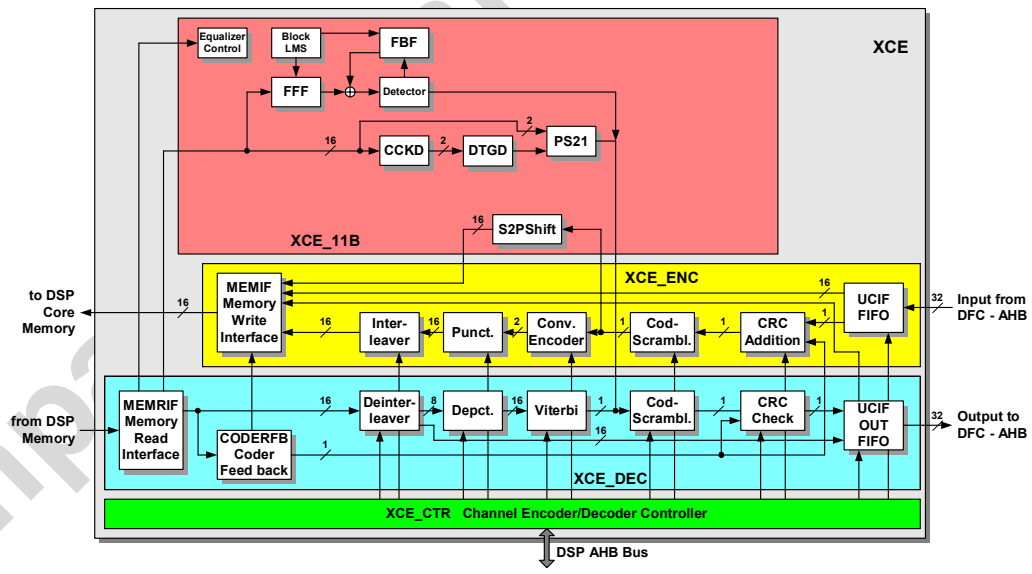


Fig 6. XCE module overview

9.3.3 Encoder

The Encoder (XCE_ENC) consists of the sub-units listed below, which are described in more detail in the following sections:

- Input FIFO
- CRC-Addition
- Scrambling
- Rate 1/2 Convolutional Encoding
- Puncturing
- Interleaving
- Memory Write Interface

9.3.3.1 Input FIFO

The Input FIFO is implemented as a circular buffer with a width of 32 bits and a size of 8 entries. It can be accessed by the DFC DMA engines, and data can be directly sent from the Input FIFO to the DSP memory.

9.3.3.2 CRC Adder

This block allows the last 32 bits at the end of each packet to be replaced by the inverted check sum.

9.3.3.3 Scrambler

The content of each Protocol Data Unit (PDU) train is scrambled with a scrambling code derived from a register of length 7. The initial state of the Scrambler, as well as the number of bits that are not subject to scrambling after initialization, is programmable.

9.3.3.4 Convolutional Encoder

The Convolutional Encoder encodes the input bits by convolving the bits with two polynomials. The number of bits is programmable. After encoding, either six tail bits are added or the following six bits are cleared (programmable).

9.3.3.5 Puncturing

Puncturing is used to reduce the number of coded bits, allowing for different code rates. Puncturing is applied to all bits in the bit stream. The supported puncturing code rates are 1/2 (no puncturing), 2/3, and 3/4.

9.3.3.6 Interleaver

The purpose of the Interleaver is to place adjacent bits on non-adjacent carriers in order to achieve a high diversity in presence of frequency selective fading. A block interleaver is used, where the block length equals the number of bits in one OFDM symbol. The modulation options for the Interleaver are BPSK, QPSK, 16-QAM, and 64-QAM.

9.3.3.7 Memory Write Interface

This interface is used for storing data into the DSP-300 Input Memory. It also generates addresses for the outgoing data stream. The start and end addresses are programmable.

9.3.4 Decoder

The Decoder (XCE_DEC) consists of the sub-units listed below, which are described in more detail in the following sections:

- Memory Read Interface
- Deinterleaving
- Depuncturing
- Rate 1/2 Viterbi Decoder
- Descrambling
- CRC-Check
- Output FIFO

9.3.4.1 Memory Read Interface

This interface is used for reading data from the DSP-300. The addresses are provided by the Deinterleaver unit. Words can also be directly sent from the DSP-300 Output Memory to the Output FIFO. A feedback mode allows for bit-wise shifting data from the DSP output memory into the Channel Encoder.

9.3.4.2 Deinterleaver

The Deinterleaver generates addresses to the Memory Read Interface for reading in data. It provides two outputs, one to the decoding logic and a direct output to the Output FIFO. As for the Interleaver, the modulation options are BPSK, QPSK, 16-QAM, and 64-QAM.

9.3.4.3 Depuncturing

Depuncturing is applied to the output bits of the Deinterleaver. The bits that were subject to puncturing are replaced by zeros. Zeros that originate from depuncturing are indicated by a separate signal. The supported depuncturing code rates are 1/2 (no depuncturing), 2/3, and 3/4.

9.3.4.4 Viterbi Decoder

The Viterbi Decoder module decodes a convolutionally encoded stream of data until a specified number of bits have been decoded. The Viterbi module can decode at a bit rate close to the clock rate. The number of bits processed by the Viterbi module is programmable. The module includes an error counter for estimating the uncoded bit error rate of the channel. It compares the hard-decided received bits that originate from convolutional encoding with the first polynomial of the convolutional encoded bits of the output of the Viterbi Decoder.

9.3.4.5 Descrambler

This module is identical to the Scrambler unit in the Encoder path.

9.3.4.6 CRC Checker

The CRC Checker passes a specified number of bits through an LFSR of length 32. The data is inverted prior to passing it through the LFSR. When all 32 bits have been cycled through the LFSR, the contents of the LFSR are read out and XORed with the following 32 bits. The result are 32 zeros, if the check sum is correct. If an error is detected, i.e., if one of the bits after comparing with the CRC was not zero, a flag bit is set. This flag can be read by the DSP-300.

9.3.4.7 Output FIFO

The Output FIFO is implemented as a circular buffer with a width of 32 bits and a size of 8 entries. It can be directly accessed by the DFC DMA engines.

Either words from the DSP-300 or decoded data can be placed into the Output FIFO. If data is received from the Channel Decoder, this data is bitwise collected and grouped into a word. MSB first or LSB first order can be selected. Additionally, the lower or higher octet of the word can be swapped. A feedback mode exists that allows for placing these words into the DSP-300 memory, enabling it to operate on demodulated data.

9.3.5 XCE IEEE802.11b Extension (XCE_11B)

The 802.11b receive part of the XCE module incorporates an adaptive decision feedback equalizer (DFE). It consists of Feedforward Filter (FFF), Feedback Filter (FBF), Least Mean Square block (LMS) for filter coefficient training, and a Detector. The CCK Encoder and Barker Spreader are part of the Detector block, but can also be accessed directly.

The 11b TX hardware generates the Preamble, SFD, and Header, and inserts them into the XCE Scrambler. The CRC16 of the Header is generated on-the-fly. The output of the Scrambler is fed into the CCK Encoder/Barker Spreader. The output of this unit is directly sent to the Sample Rate Conversion unit of the RTX block.

9.3.6 DSP-300 Central Input/Output Unit - CIO

The Central Input/Output Unit (CIO) provides the connection of the DSP-300 Core to the AHB2 bus. In addition, it contains basic peripheral devices such as a Master Watch Counter, two Timers, and the necessary registers to allow proper communication of the DSP-300 with the peripheral modules connected to the AHB2.

9.3.7 Timer Module - TIM

The Timer Module (TIM) consists of two 32-bit wide timers with a programmable prescaler. The prescaler divides the input clock to provide various timer input frequencies. The following modes of operation are available for each timer:

- periodic counter without threshold (wraps around the max. counter value)
- periodic counter with programmable threshold (wraps around the threshold value)
- sequential counter without threshold (stops at the max. counter value)
- sequential counter with threshold (stops at the threshold value)

Up to four interrupts can be generated by the TIM. They are triggered when the programmed threshold (or match) values are reached. Four threshold values can be programmed and used with any of the two timers.

9.3.8 Interrupt Controller - INC

The Interrupt Controller (INC) of the SA5253 receives the interrupt request lines from various modules. It arbitrates and forwards the requests to the DSP in three different ways:

- Direct Interrupts
  The interrupt requests are forwarded directly to the DSP. This way of interrupt processing provides the highest performance.
- Fast Interrupts
  The INC receives the requests and determines the one with the highest priority (Round-Robin scheme). It selects the corresponding preloaded interrupt vector (the absolute address of the interrupt service routine) and forwards the request and the vector address to the DSP. After suspending the current program, the DSP-300 uses the vector address to branch to the respective interrupt service routine. This method provides relatively high performance while using only one interrupt input of the DSP.
- Slow Interrupts
  The INC receives the requests and builds a logical OR of all lines. The output of the OR-gate is connected to an interrupt input of the DSP. After receiving the interrupt

request, the DSP has to read the status register that holds the request bits of all interrupt sources. It then resolves the interrupt priorities by software and calculates the address of the appropriate interrupt service routine.

The INC contains all the necessary registers to program the interrupt requests for polarity, edge or level sensitivity, enable/disable, as well as vector address, and to provide respective status information about active requests and the current vector address. In addition, interrupt emulation by triggering interrupt requests through software is made possible via respective registers.

9.3.9 Receive/Transmit Module - RTX

The Receive/Transmit module (RTX) performs the digital filtering for the receive and transmit paths.

9.3.9.1 Transmit Unit

The Digital TX Filter unit contains DC and I/Q mismatch compensation, upsampling, interpolation filtering, and a selectable reversion of the frequency band. A block diagram of the TX digital filtering and conversion path up to the DACs is given in Fig. 7. The DSP generates a 20 MHz transmit signal into the Output Memory. The DAC clock frequency is 80 MHz.

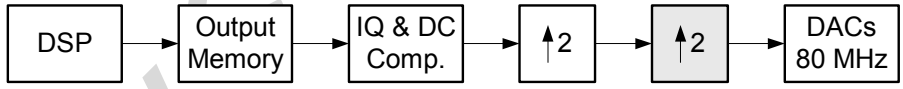


Fig 7. TX digital filtering and conversion path block diagram

9.3.9.2 Receive Unit

The Digital RX Filter unit contains anti-aliasing filtering, down-sampling as well as DC and I/Q mismatch compensation. Fig. 8 shows a block diagram of the RX digital filtering and conversion path up to the ADCs. Two basic operation modes are supported, which are summarized in Table 3.

- IEEE 802.11g operation. ADC sampling is at 40 MHz. RX filter converts to 20 MHz. If an 11b burst is received, the 20 MHz -> 22 MHz sample rate conversion is performed in software
- IEEE 802.11b operation. The ADC runs at 20 MHz, the 20 MHz -> 22 MHz sample rate conversion is performed in software

Table 3: RX operating modes

Mode	Switch A	ADC Clock
RX 802.11g	0	40 MHz
RX 802.11b	1	20 MHz

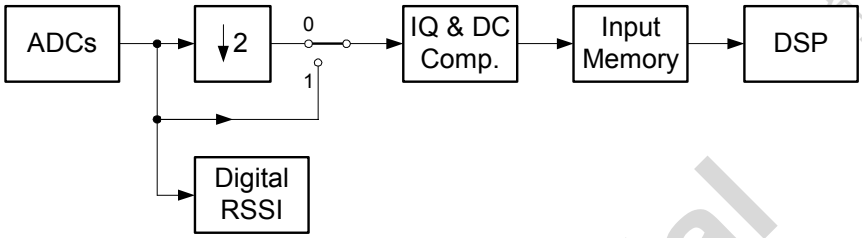


Fig 8. RX digital filtering and conversion path block diagram

9.3.9.3 Receive Signal Strength Indicator Unit (RSSI)

The Receive Signal Strength Indicator unit (RSSI) of the SA5253 supports two ways, analog and digital RSSI, to achieve proper information on the incoming signal strength. Analog RSSI is supported via a dedicated Analog-to-Digital Converter (ADC), which usually is connected to the output of a logarithmic amplifier in the RF Front-End circuitry. Digital RSSI is derived from observation of the digital receive signal of the I and Q ADCs.

9.3.10 Mixed Signal Block

The Mixed Signal Block consists of the following modules:

- Two 9-bit ADCs used for the I and Q inputs of the RX interface. The sampling frequency is 20 MHz for the 802.11b mode and 40 MHz for the 802.11g mode
- A 9-bit ADC used for RSSI measurements
- Two 10-bit DACs used for generating the baseband signal for the RF IC. The DACs are operating with the sample rate of 80 MHz
- A 10-bit low-speed auxiliary DAC
- A 50 MHz XO, used in the slave mode as a reference clock squarer
- A Low-Swing Input Buffer, used as an alternative solution for the reference clock squarer
- A 32 kHz XO, used as a sleep clock generator
- A Low-Frequency Ring Oscillator, used as an alternative solution for the sleep clock generator
- Power-on reset generator

9.3.11 RF Control Block - RFCTRL

This block allows the DSP to program the state of several pins used to control the RF chip. It also has the read access to the GPIO pins of the GPIO module in SSS.

9.4 South subsystem - SSS

The SSS block includes the low performance APB/VPB bus and the System Data Memory (DMEM). The APB is connected to the Multilayer Module (MLM) through an AHB2APB bridge. The DMEM memory is directly connected to the Multilayer through an AHB bus.

Further units in the SSS block are the Core Communication Center units (C3s), the Clock Generation Unit (CGU), a Timer Unit (TIM32), the General Purpose I/O control (GPIO), the 4-Wire Bus unit (4WB), a Bluetooth Coexistence Interface (BT), as well as debug facilities (Debug UART and DBX).

9.4.1 System Data Memory - DMEM

The DMEM provides 96 kbytes of SRAM.

9.4.2 Core Communication Center Units - C3

C3 stands for Core Communication Center, which facilitates the communication between cores. In general, a C3 is a combination of a mailbox, a counter, and an external-event detector. A C3 can be used to exchange data between different cores via its mailbox functionality. The SA5253 incorporates four C3 units.

The C3 waits for an event or a combination of events. After receiving an event, an interrupt will be asserted. An event might be either a mailbox write access, or the counter being equal to zero, or when an external interrupt input toggles. In order to allow any combination of those three event causes, it is possible to select which event is used to generate an interrupt.

9.4.3 Clock Generation Unit - CGU

The Clock Generation Unit (CGU) provides the internal clocks for the 802.11b/g Low-Power Baseband. It contains the on-chip PLL. The PLL output frequency is a programmable multiple of the input frequency. The CGU generates the internal frequencies from an input frequency of 13, 19.2, 20, 26, 38.4 or 40 MHz. While the PLL operates at 480 MHz, the clock divider provides the required internal frequencies of 120 MHz and 60 MHz for the digital logic, as well as the frequencies of 20, 40, and 80 MHz for the AD/DA converters.

In power save mode, the digital parts of the SA5253 can run with a low-frequency sleep clock.

In addition to the clock generation, the CGU performs power-up reset control and synchronization.

9.4.4 Timer Unit - TIM32

The 32 kHz Timer is driven by an external sleep clock and is responsible for waking up the system from sleep mode. The TIM32 provides a 32-bit clock counter and a 32-bit alarm time register.

9.4.5 General Purpose I/O - GPIO

The General Purpose I/O module (GPIO) controls the eight GPIO pins of the SA5253 baseband chip. All pins are individually configurable for input or output mode. In addition, pull-up, pull-down, or plain operation can be selected. Registers are provided to allow data to be written to and read from the GPIO pins.

9.4.6 Multilayer Module - MLM

The Multilayer Module provides a pseudo cross-connect for the backbone bus system of the SA5253. It provides a low-cost, high-speed implementation of the multi-layer AHB-protocol. In the SA5253, the MLM connects 5 master devices and 4 slave devices, each of which has a width of 32 bits.

9.4.7 4-Wire Bus Unit - 4WB

The 4WB unit is used to exchange control and status information with the RF chip. It uses four signal lines for clock, enable, data in, and data out signals.

9.4.8 WLAN/Bluetooth Coexistence Interface - BT

The Bluetooth Coexistence Interface (BT) provides four signals, and has the following features:

- Interfaces to a range of NXP Semiconductors Bluetooth modules
- Hardware functionality to facilitate connection to 3rd party Bluetooth solutions
- Hardware support for IEEE 802.15.2 Packet Traffic Arbitration recommendations.

10. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{stg}	Storage temperature		-55	125	°C
V_{dd_pa}	Supply voltage power amplifier		-0.3	5.5	V
V_{dd_rf}	Supply voltage analog RF		-0.3	3.0	V
V_{dd_vco}	Supply voltage analog VCO		-0.3	3.0	V
V_{dd_a}	Supply voltage analog		-0.3	3.0	V
V_{dd_io}	Supply voltage digital I/O		-0.5	4.6	V
V_{dd_bt}	Supply voltage digital Bluetooth I/O		-0.5	4.6	V
V_{dd_core}	Supply voltage digital core		-0.5	1.5	V
V_I	Input voltage		-0.5	V_{dd_io} + 0.5	V
I_{lu}	Latch-up current[1]	$V_I < 0$ or $V_I > V_{dd\_io}$	-	100	mA
V_{ESD}	Electrostatic Discharge Voltage	HBM[2] MM[3] CDM[4]	-2000 -200 -200	2000 200 200	V V V

[1] JEDEC standard JESD78, IC Latch-Up Test.

[2] JEDEC standard JESD22-A114-B, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).

[3] JEDEC standard JESD22-A115-A, Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM).

[4] JEDEC standard JESD22-C101-B, Field-Induced Charged-Device Model (CDM) Test Method For Electrostatic Discharge Withstand Thresholds Of Microelectronic Components.

11. Recommended operating conditions

Table 5: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{dd_pa}	Supply voltage power amplifier		2.8	3.3	4.5	V
V_{dd_rf}	Supply voltage analog RF		2.8	2.85	2.9	V
V_{dd_vco}	Supply voltage analog VCO		2.8	2.85	2.9	V
V_{dd_a}	Supply voltage analog		2.8	2.85	2.9	V
V_{dd_io}	Supply voltage digital I/O		1.65	3.3	3.6	V
V_{dd_bt}	Supply voltage digital Bluetooth I/O		1.65	3.3	3.6	V
V_{dd_core}	Supply voltage digital core		1.1	1.2	1.3	V
T_{amb}	Ambient temperature		-30	25	85	°C

12. Static characteristics

Table 6: Static characteristics: supply pins

Nominal supply voltages, T_{amb} = -30 °C to 85 °C, typical values at T_{amb} = 25 °C unless stated otherwise

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
Power amplifier supply						
V_{dd_pa}	Supply voltage		2.8	3.3	4.5	V
$I_{dd\_pa(sleep)}$	Sleep[2] supply current		-	5	-	µA
$I_{dd\_pa(rx)}$	Receive supply current		-	5	-	µA
$I_{dd\_pa(tx)}$	Transmit supply current	54 Mbits/sec, maximum output power	-	90	-	mA
Analog RF supply						
V_{dd_rf}	Supply voltage		2.8	2.85	2.9	V
$I_{dd\_rf(sleep)}$	Sleep[2] supply current		-	1	-	µA
$I_{dd\_rf(rx)}$	Receive supply current	54 Mbits/sec	-	25	-	mA
$I_{dd\_rf(tx)}$	Transmit supply current	54 Mbits/sec	-	35	-	mA
Analog VCO supply						
V_{dd_vco}	Supply voltage		2.8	2.85	2.9	V
$I_{dd\_vco(sleep)}$	Sleep[2] supply current		-	< 1	-	µA
$I_{dd\_vco(rx)}$	Receive supply current	54 Mbits/sec	-	15	-	mA
$I_{dd\_vco(tx)}$	Transmit supply current	54 Mbits/sec	-	15	-	mA
Analog supply						
V_{dd_a}	Supply voltage		2.8	2.85	2.9	V
$I_{dd\_a(sleep)}$	Sleep[2] supply current		-	20	-	µA
$I_{dd\_a(rx)}$	Receive supply current	54 Mbits/sec	-	60	-	mA
$I_{dd\_a(tx)}$	Transmit supply current	54 Mbits/sec	-	30	-	mA
Digital I/O supply						
V_{dd_io}	Supply voltage		1.65	3.3	3.6	V
$I_{dd\_io(sleep)}$	Sleep[2] supply current		-	2	-	µA
$I_{dd\_io(rx)}$	Receive supply current		-	2	-	mA
$I_{dd\_io(tx)}$	Transmit supply current		-	< 1	-	mA
Digital Bluetooth I/O supply						
V_{dd_bt}	Supply voltage		1.65	3.3	3.6	V
$I_{dd\_bt(sleep)}$	Sleep[2] supply current		-	< 1	-	µA
$I_{dd\_bt(rx)}$	Receive supply current		-	< 1	-	mA
$I_{dd\_bt(tx)}$	Transmit supply current		-	< 1	-	mA
Digital core supply						
V_{dd_core}	Supply voltage		1.1	1.2	1.3	V
$I_{dd\_core(sleep)}$	Sleep[2] supply current		-	200	-	µA
$I_{dd\_core(rx)}$	Receive supply current	54 Mbits/sec	-	90	-	mA
$I_{dd\_core(tx)}$	Transmit supply current	54 Mbits/sec	-	85	-	mA

[1] All measurements are made with the BGW211 evaluation board.

[2] Sleep is defined as the low-power state where the system is inactive but still able to wake up to receive beacons.

Table 7: Static characteristics: digital pins

V_{dd_io} = 3.3V, T_{amb} = -30 °C to 85 °C, typical values at T_{amb} = 25 °C unless stated otherwise

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input characteristics						
V_{IL}	Low-level input voltage		-	-	0.3 * V_{dd_io}	V
V_{IH}	High-level input voltage		0.7 * V_{dd_io}	-	-	V
I_{IN1}	Input leakage current, plain inputs		-	-	<1	µA
I_{IN2}	Input current, inputs with pull-down devices	3.0 V ≤ V_{dd_io} ≤ 3.6 V, V_{IH} = V_{dd_io}	25	50	85	µA
		1.65 V ≤ V_{dd_io} ≤ 1.95 V, V_{IH} = V_{dd_io}	5	12	25	µA
I_{IN3}	Input current, inputs with pull-up devices	3.0 V ≤ V_{dd_io} ≤ 3.6 V, V_{IL} = 0V	25	50	85	µA
		1.65 V ≤ V_{dd_io} ≤ 1.95 V, V_{IL} = 0V	5	12	25	µA
Output characteristics						
V_{OL}	Low-level output voltage	V_{dd_io} = 3.3 V, I_{OL} = 3 mA	-	-	0.4	V
		V_{dd_io} = 1.8 V, I_{OL} = 1.5 mA	-	-	0.4	V
V_{OH}	High-level output voltage	V_{dd_io} = 3.3 V, I_{OL} = -5 mA	2.9	-	-	V
		V_{dd_io} = 1.8 V, I_{OL} = -2.8 mA	1.4	-	-	V
R_{OUT}	Output Impedance[1]	3.0 V ≤ V_{dd_io} ≤ 3.6 V V_{OUT} = 0.5 * V_{dd_io}	40	-	60	Ω
		1.65 V ≤ V_{dd_io} ≤ 1.95 V V_{OUT} = 0.5 * V_{dd_io}	75	-	215	Ω
I_{OSL}	Short circuit current, output low	3.0 V ≤ V_{dd_io} ≤ 3.6 V	-	-	104	mA
		1.65 V ≤ V_{dd_io} ≤ 1.95 V	-	-	34	mA
I_{OSH}	Short circuit current, output high	3.0 V ≤ V_{dd_io} ≤ 3.6 V	-	-	185	mA
		1.65 V ≤ V_{dd_io} ≤ 1.95 V	-	-	66	mA

[1] In order to achieve the required performance of the Host interfaces at Vdd_io = 1.8V, the PCB trace length of the output signals should not exceed 100 mm and the capacitive load should not exceed 5 pF.

13. Dynamic characteristics

13.1 Receiver characteristics

Table 8: Receiver characteristics

Nominal supply voltages, T_{amb} = -30 °C to 85 °C,typical values at T_{amb} = 25 °C unless otherwise stated, all receiver characteristics apply to both the main and auxiliary antenna connectors

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver sensitivity in 802.11b mode						
	1 Mbit/s	PER < 8%, PSDU = 1024 bytes, in-band noise at antenna connector = -174 dBm/Hz	-	-95	-93	dBm
	2 Mbit/s		-	-92	-88	dBm
	5.5 Mbit/s		-	-90	-86	dBm
	11 Mbits/s		-	-87	-83	dBm
Receiver sensitivity in 802.11g mode						
	6 Mbit/s	PER < 10%, PSDU = 1000 bytes, in-band noise at antenna connector = -174 dBm/Hz	-	-91	-89	dBm
	9 Mbit/s		-	-90	-88	dBm
	12 Mbit/s		-	-87	-83	dBm
	18 Mbit/s		-	-86	-82	dBm
	24 Mbit/s		-	-83	-79	dBm
	36 Mbit/s		-	-80	-76	dBm
	48 Mbit/s		-	-75	-71	dBm
	54 Mbits/s		-	-74	-70	dBm
Maximum input level						
	Maximum input signal level in 802.11b mode	PER < 8%	-10	-	-	dBm
	Maximum input signal level in 802.11g mode	PER < 10%	-10	-	-	dBm
Adjacent channel rejection (ACR) in 802.11b mode						
	1 Mbit/s	PER < 8%, PSDU = 1024 bytes, in-band noise at antenna connector = -174 dBm/Hz	37	-	-	dB
	2 Mbit/s		37	-	-	dB
	5.5 Mbit/s		37	-	-	dB
	11 Mbits/s		37	-	-	dB
Adjacent channel rejection (ACR) in 802.11g mode						
	6 Mbit/s	PER < 10%, PSDU = 1000 bytes, in-band noise at antenna connector = -174 dBm/Hz	18	-	-	dB
	9 Mbit/s		17	-	-	dB
	12 Mbit/s		15	-	-	dB
	18 Mbit/s		13	-	-	dB
	24 Mbit/s		10	-	-	dB
	36 Mbit/s		6	-	-	dB
	48 Mbit/s		2	-	-	dB
	54 Mbits/s		1	-	-	dB
Carrier sense						
	Carrier sense level		-62	-	-	dBm

Table 8: Receiver characteristics *…continued*

Nominal supply voltages, T_{amb} = -30 °C to 85 °C,typical values at T_{amb} = 25 °C unless otherwise stated, all receiver characteristics apply to both the main and auxiliary antenna connectors

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tolerable delay spread						
	Tolerable delay spread in 802.11b mode, 1 - 2 Mbit/s	PER < 8%, exponential delay profile	200	-	-	ns
	Tolerable delay spread in 802.11b mode, 5.5 Mbit/s	PER < 8%, exponential delay profile	100	-	-	ns
	Tolerable delay spread in 802.11b mode, 11 Mbit/s	PER < 8%, exponential delay profile	50	-	-	ns
	Tolerable delay spread in 802.11g mode, 6 - 36 Mbit/s	PER < 10%, exponential delay profile	200	-	-	ns
	Tolerable delay spread in 802.11g mode, 48 - 54 Mbit/s	PER < 10%, exponential delay profile	100	-	-	ns
Out-of-band signal blocking						
	824 - 915 MHz signal blocking	Out-of-band signal level resulting in 1 dB sensitivity loss	-10	-	-	dBm
	1710 - 1910 MHz signal blocking		-30	-	-	dBm
	1920 - 1980 MHz signal blocking		-30	-	-	dBm

13.2 Transmitter characteristics

Table 9: Transmitter characteristics

Nominal supply voltages, T_{amb} = -30 °C to 85 °C,typical values at T_{amb} = 25 °C unless otherwise stated, all receiver characteristics apply to both the main and auxiliary antenna connectors

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Linear output power						
	Maximum output power in 802.11b mode		12	17	19	dBm
	Maximum output power in 802.11g mode, 6 - 36 Mbit/s		12	17	19	dBm
	Maximum output power in 802.11g mode, 48 - 54 Mbit/s		10	15	17	dBm
	Output power dynamic range in 802.11b mode		-	25	-	dB
	Output power dynamic range in 802.11g mode		-	25	-	dB
	Output power control resolution		-	1	-	dB
Transmit spectrum mask						
	802.11b spectrum mask at maximum output power	$\|f - fc\| < 11$ MHz	-	-	0	dBr
		$11 \text{ MHz} \leq \|f - fc\| < 22$ MHz	-	-	-30	dBr
		$\|f - fc\| \geq 22$ MHz	-	-	-45	dBr

Table 9: Transmitter characteristics *…continued*

Nominal supply voltages, T_{amb} = -30 °C to 85 °C,typical values at T_{amb} = 25 °C unless otherwise stated, all receiver characteristics apply to both the main and auxiliary antenna connectors

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	802.11g spectrum mask at maximum output power	|f - fc| < 9 MHz	-	-	0	dBr
		|f - fc| = 11 MHz	-	-	-20	dBr
		|f - fc| = 20 MHz	-	-	-28	dBr
		|f - fc| ≥ 30 MHz	-	-	-40	dBr
Transmit modulation accuracy in 802.11b mode						
	1 Mbits/s EVM peak	maximum output power, measured with time tracking enabled	-	-	35	%
	2 Mbits/s EVM peak		-	-	35	%
	5.5 Mbits/s EVM peak		-	-	35	%
	11 Mbits/s EVM peak		-	-	35	%
Transmit modulation accuracy in 802.11g mode						
	6 Mbits/s EVM RMS	maximum output power, measured with time tracking enabled	-	-	-5	dB
	9 Mbits/s EVM RMS		-	-	-8	dB
	12 Mbits/s EVM RMS		-	-	-10	dB
	18 Mbits/s EVM RMS		-	-	-13	dB
	24 Mbits/s EVM RMS		-	-	-16	dB
	36 Mbits/s EVM RMS		-	-	-19	dB
	48 Mbits/s EVM RMS		-	-	-22	dB
	54 Mbits/s EVM RMS		-	-	-25	dB
Transmit power-on and power-down ramp time in 802.11b mode						
	Transmit power-on ramp time from 10% to 90% output power		-	-	2	µs
	Transmit power-down ramp time from 90% to 10% output power		-	-	2	µs
Wideband noise						
	869 - 960 MHz	maximum output power	-	-134	-	dBm/Hz
	1805 - 1990 MHz		-	-134	-	dBm/Hz
	2110 - 2170 MHz		-	-132	-	dBm/Hz
Other spectral parameters						
	Carrier suppression		-	-	-15	dBr
	Center frequency leakage		-	-	-25	dBr
	Power spectrum magnitude variation	|f - fc| ≤ 8.3 MHz	-	-	± 2	dB
	Group delay distortion	|f - fc| ≤ 8.3 MHz	-	-	130	nsec
	2nd harmonic level	maximum output power	-	-	-25	dBm
	3rd harmonic level	maximum output power	-	-	-25	dBm
	Spurious emissions at the antenna outside of burst	30 MHz - 1 GHz, measurement bandwidth = 100 kHz	-	-	-57	dBm
		1 GHz - 26.5 GHz, measurement bandwidth = 1 MHz	-	-	-50	dBm
	Phase noise at the antenna port with an unmodulated carrier	at 10 kHz offset	-	-	-85	dBc/Hz
		at 100 kHz offset	-	-	-92	dBc/Hz

14. Power-Up Sequence

Fig. 9 shows the supply voltage ramp-up sequence, and Table 10 describes the power-up sequence timing parameters.

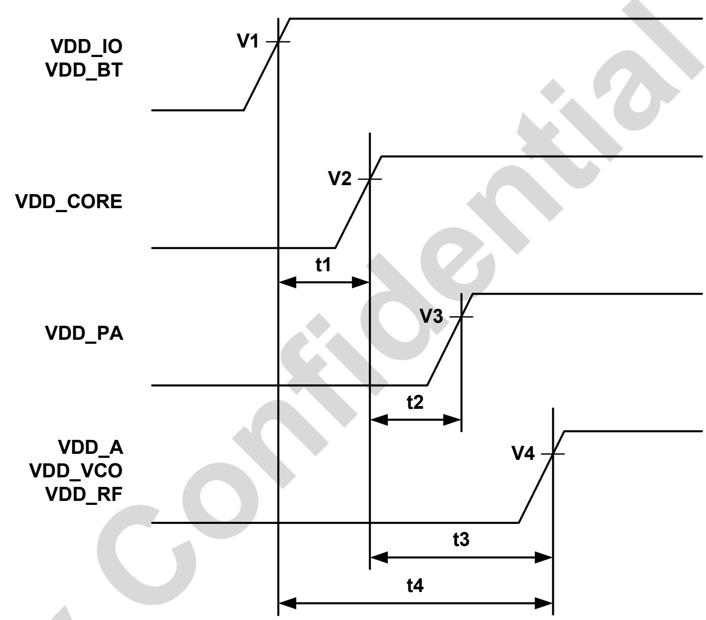


Fig 9. Power-up sequence timing diagram

Table 10: Power-up sequence timing parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V1	Minimum VDD_IO voltage		1.65	-	-	V
V2	Power-on reset high voltage trip level		-	-	1.0	V
V3	Minimum VDD_PA voltage		2.8	-	-	V
V4	Minimum VDD_A voltage		2.8	-	-	V
t1	VDD_IO and VDD_BT to VDD_CORE delay		0	-	-	µs
t2	VDD_CORE to VDD_PA delay		-	-	400	µs
t3	VDD_CORE to VDD_A, VDD_VCO and VDD_RF delay		-	-	400	µs
t4	VDD_IO and VDD_BT to VDD_A, VDD_VCO and VDD_RF delay		0	-	-	µs

15. Reset strategy

The BGW211 has an active-low asynchronous reset input (RESET_N) and a built-in power-on reset (POR) circuit. The power-on reset functionality is compatible with the BGW200 solution, but the external connection between POR_N and RESET_N is not required.

Fig. 10 shows the power-on reset and reset timing diagram, and Table 11 describes the reset timing parameters.

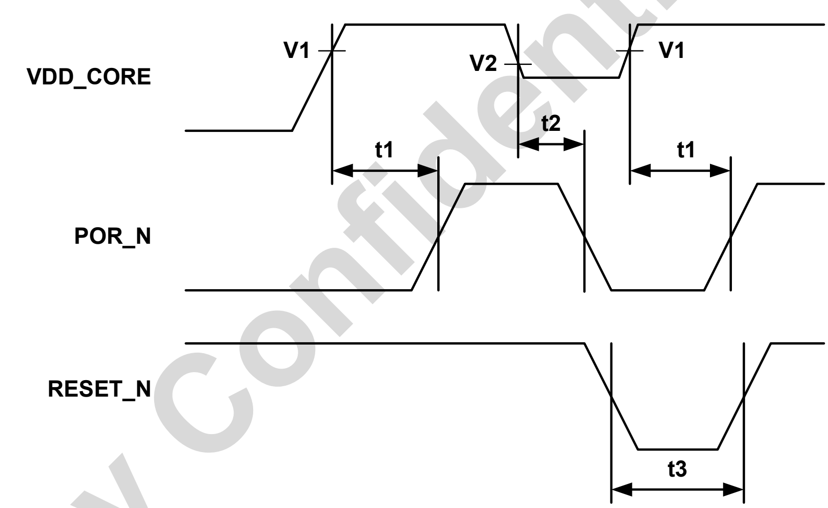


Fig 10. Power-on reset and reset timing diagram

Table 11: Reset timing parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V1	Power-on reset high voltage trip level		-	-	1.0	V
V2	Power-on reset low voltage trip level		-	-	0.9	V
t1	Amount of time during which VDD_CORE > V1 before POR_N becomes high		-	-	2	µs
t2	Amount of time during which VDD_CORE < V2 before POR_N becomes low		-	-	11	µs
t3	Reset pulse width		10	-	-	ns

16. Clock strategy

16.1 Reference clock

The BGW211 supports two sources of the reference clock:

- External reference clock signal (sine wave)
- Internal crystal oscillator (requires an external crystal)

Fig. 11 shows the reference clock activation timing diagram, and Table 12 describes the reference clock parameters.

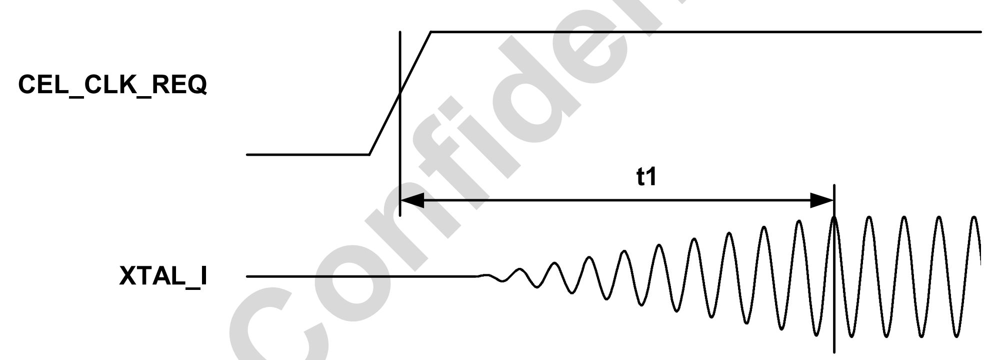


Fig 11. Reference clock activation timing diagram

Table 12: External reference clock parameters[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Reference clock frequency		-	40[2]	-	MHz
	Reference clock frequency error		-	-	± 25	ppm
	Phase noise	at 10 kHz offset	-	-	-140	dBc/Hz
		at 100 kHz offset	-	-	-145	dBc/Hz
	Input resistance	at 40 MHz	-	2.6	-	kΩ
	Input capacitance	at 40 MHz	-	0.7	-	pF
	Input voltage amplitude	peak to peak	0.3	0.8	1.0	V
t1	Reference clock activation time		-	-	800[3]	µs

[1] The reference clock should be AC-coupled and applied to pin XTAL_I.

[2] The following reference clock frequencies are supported: 13, 19.2, 20, 26, 38.4 and 40 MHz.

[3] Software configurable parameter.

16.2 Sleep clock

The BGW211 supports three sources of the sleep clock:

- External sleep clock signal (square wave)
- Internal 32 kHz crystal oscillator (requires an external crystal)
- Internal ring oscillator.

Table 13 describes the external sleep clock parameters. The external sleep clock should be applied to the OSC32K_I pin via a 2 MΩ resistor placed as close as possible to the pin.

Table 13: Sleep clock parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Sleep clock frequency		-	32.768	-	kHz
	Sleep clock frequency error		-	-	± 150	ppm
	Duty cycle		30	-	70	%
	Input signal voltage[1]	low	0	-	0.2	V
		high	1.65	-	3.6	V

[1] Including the external 2 MΩ series resistor.

17. Host Interface Timing

17.1 SPI2 Interface Timing

Fig. 12 and Fig. 13 show the SPI2 interface timing diagrams, and Table 14 describes the SPI2 interface timing parameters.

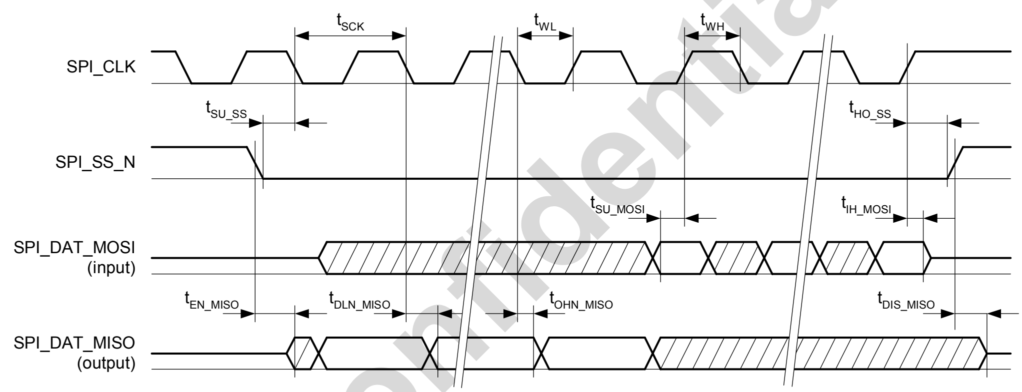


Fig 12. SPI2 interface timing diagram for SPI_DAT_MISO clocked on the negative edge of SPI_CLK

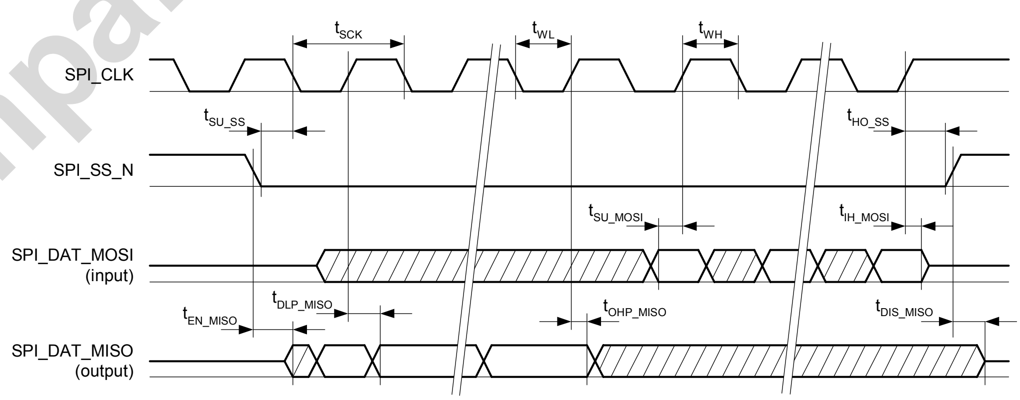


Fig 13. SPI2 interface timing diagram for SPI_DAT_MISO clocked on the positive edge of SPI_CLK

Table 14: SPI2 interface timing parameters

Symbol	Parameter	Conditions	Min	Max	Unit
t_{CLK}	Period of SPI_CLK		16.67	-	ns
t_{WH}	Clock high time		7.8	-	ns
t_{WL}	Clock low time		7.8	-	ns
t_{SU_SS}	Setup time for SPI_SS_N		3.0	-	ns
t_{HO_SS}	Hold time for SPI_SS_N		0.0	-	ns
t_{SU_MOSI}	Setup time for SPI_DAT_MOSI		4.0	-	ns
t_{IH_MOSI}	Input hold time for SPI_DAT_MOSI		0.0	-	ns
t_{EN_MISO}	Output enable time for SPI_DAT_MISO		-	8.0	ns
t_{DIS_MISO}	Output disable time for SPI_DAT_MISO		-	6.0	ns
t_{DLN_MISO}	Output delay for SPI_DAT_MISO (clocked on negative edge of SPI_CLK)	$C_{LOAD} \leq 10$ pF	-	10.0	ns
t_{OHN_MISO}	Output hold time for SPI_DAT_MISO (clocked on negative edge of SPI_CLK)	$C_{LOAD} \leq 10$ pF	0.0	-	ns
t_{DLN_MISO}	Output delay for SPI_DAT_MISO (clocked on positive edge of SPI_CLK)	$C_{LOAD} \leq 10$ pF	-	10.0	ns
t_{OHN_MISO}	Output hold time for SPI_DAT_MISO (clocked on positive edge of SPI_CLK)	$C_{LOAD} \leq 10$ pF	3.0	-	ns

17.2 SDIO interface timing

Fig. 14 shows the SDIO interface timing diagrams, and Table 15 describes the SDIO interface timing parameters.

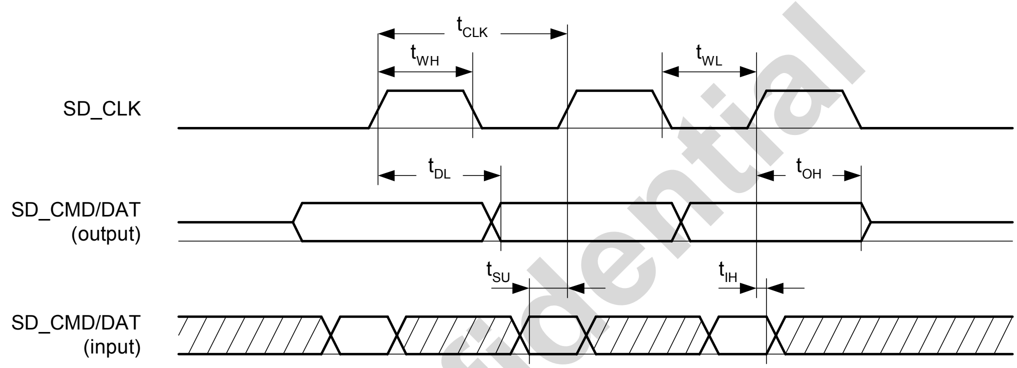


Fig 14. SDIO interface timing diagram

Table 15: SDIO interface timing parameters

Symbol	Parameter	Conditions	Min	Max	Unit
t_{CLK}	Period of SD_CLK		40.0	-	ns
t_{WH}	SD_CLK high time		10.0	-	ns
t_{WL}	SD_CLK low time		10.0	-	ns
t_{DL}	Output delay for SD_CMD/DAT[n]	$C_{LOAD} \leq 10$ pF	-	14.0	ns
t_{OH}	Output hold time for SD_CMD/DAT[n]	$C_{LOAD} \leq 10$ pF	0.0	-	ns
t_{SU}	Input setup time for SD_CMD/DAT[n]		5.0	-	ns
t_{IH}	Input hold time for SD_CMD/DAT[n]		5.0	-	ns

18. Booting mechanisms

The SA5253 baseband chip contains three separate processor cores and several dedicated hardware units. The processor cores are connected to dedicated and shared memory subsystems. After power up and reset, the boot interface has to be selected and set up, the memories have to be filled with firmware data and program code, and the on and off chip peripherals have to be set up. The total firmware size is approximately 240 kbytes.

As the ARM processor has control over most of the on-chip interfaces, it is responsible for booting, and therefore contains a small piece of ROM with the code for transferring the data from the boot interfaces. The boot loader is able to boot via SDIO, SPI2 and from an EEPROM connected to the SPI. The boot interface is selected via external MODE[4:0] pins. These pins are read from the ARM processor at reset.

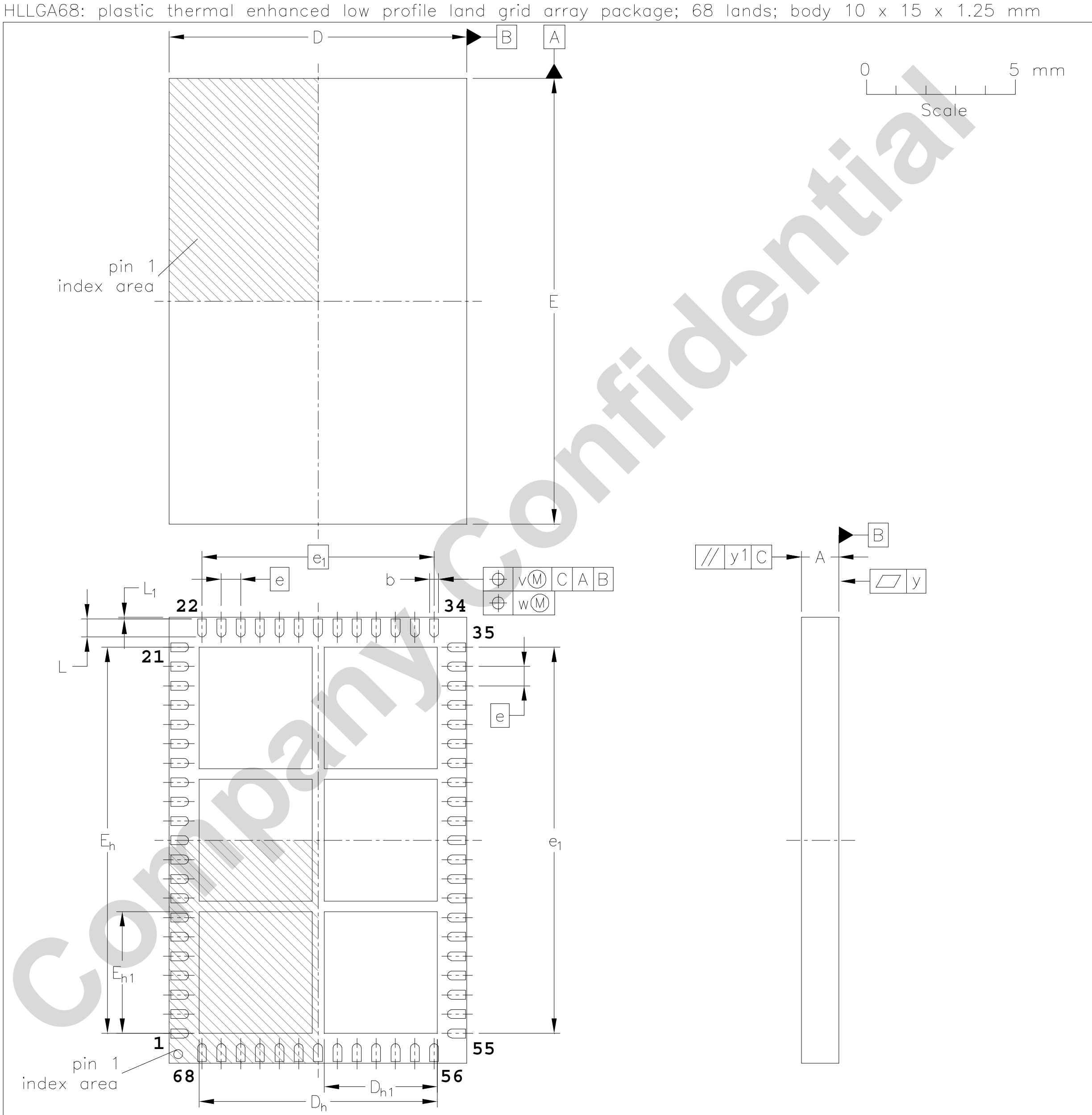
Table 16 shows the supported boot modes.

Table 16: Boot Modes

Mode	Mode[4:0]	Name	Description	Host interface	Comments
0	0 0000		Reserved		
1	0 0001		Reserved		
2	0 0010		Reserved		
3	0 0011	SPI_SCP_H_SPI2	Boot from SPI EEPROM	SPI2 on SPI pins	
4	0 0100		Reserved		
5	0 0101		Reserved		
6	0 0110		Reserved		
7	0 0111		Reserved		
8	0 1000		Reserved		
9	0 1001		Reserved		
A	0 1010	I2C_H_SPI2	Boot from I2C EEPROM	SPI2 on SPI pins	
B	0 1011		Reserved		
C	0 1100		Reserved		
D	0 1101		Reserved		
E	0 1110		Reserved		
F	0 1111		Reserved		
10	1 0000	SPI2	Boot from SPI2 Host interface using SPI pins	SPI2 on SPI pins	BGW200 compatible boot mode
11	1 0001		Reserved		
12	1 0010	SDIO	Boot from SDIO Host interface	SDIO	BGW200 compatible boot mode
13	1 0011	SPI_H_SDIO	Boot from SPI EEPROM or Flash	SDIO	BGW200 compatible boot mode
14	1 0100		Reserved		
15	1 0101		Reserved		
16	1 0110		Reserved		
17	1 0111		Reserved		
18	1 1000		Reserved		
19	1 1001		Reserved		
1A	1 1010		Reserved		
1B	1 1011		Reserved		
1C	1 1100		Reserved		
1D	1 1101	UART40	Boot from UART, use the 40 MHz reference clock as the system clock during the boot process	UART	Debug boot mode
1E	1 1110	UART13_PLL120	Boot from UART, use the 13 MHz reference clock and PLL to generate the 120 MHz system clock during the boot process	UART	Debug boot mode
1F	1 1111		Reserved		

19. Package outline

HLLGA68: plastic thermal enhanced low profile land grid array package; 68 lands; body 10 x 15 x 1.25 mm



UNIT	A	b	D	D_h	D_{h1}	E	E_h	E_{h1}	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	1.3 1.2	0.32 0.28	10.1 9.9	8.1 7.9	3.9 3.7	15.1 14.9	13.1 12.9	4.2 4.0	0.65	7.8	13.0	0.625 0.575	0.05 0	0.1	0.05	0.05	0.1

PACKAGE OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT858-2 PUBLICATION DRAWING		MO-220			05-10-11

Fig 15. HLLGA68 package outline (SOT858-1)

20. Soldering

20.1 Printed Circuit Board and Stencil Design

20.1.1 PCB Layout

20.1.1.1 Solder Land Design

The PCB footprint of the HLLGA package should be preferably copper defined/ Non-Solder-Mask-Defined (NSMD). In HLLGA-QFN style packages, the centre pad is used primarily for grounding and can be used as heat sink with thermal vias. The larger metal plane can be divided to obtain smaller solderlands.

The solder mask clearance around the solderland depends on the capabilities of the PCB suppliers but is generally between 0.05 mm and 0.1 mm. NSMD footprint improves flux outflow during soldering.

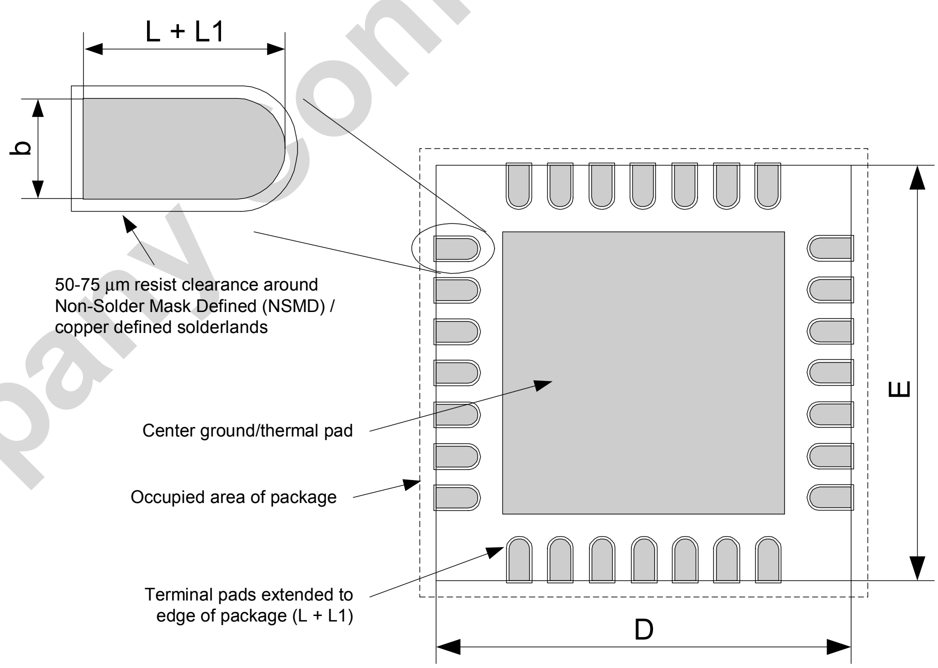


Fig 16. General guideline of PCB solderland design of a HLLGA package; dimensions b, L, L1, D and E are specified in the package outline

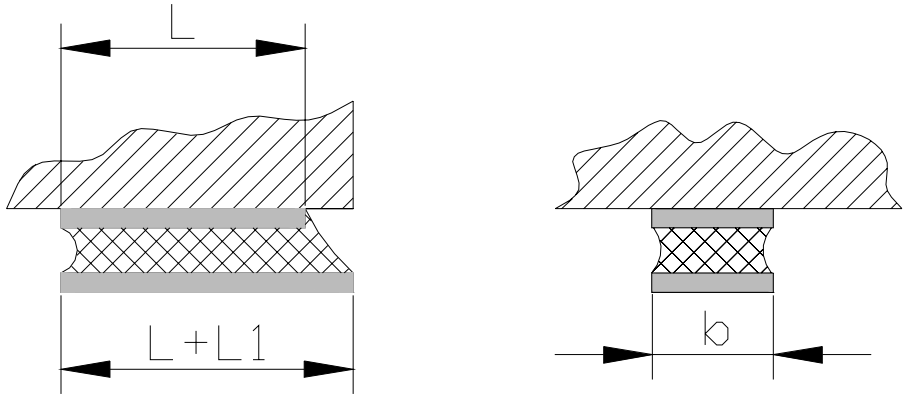


Fig 17. Solder joint shape after board mounting

20.1.1.2 Via Design

Through-hole vias in the ground plane should be plugged and preferably have a top metallization. In case that through hole vias are used to connect the terminal pads, than they should be placed outside the package area to prevent shorts and voids.

Voiding in the solder joints can further be minimized by locating the through hole vias under the stencil web area or close to the corner of the stencil apertures (see Fig. 18).

Microvias can be placed in both, central ground pad and terminal pads. Voiding in the solder joints can further be minimized by locating the microvias under the stencil web area or close to the corner of the stencil apertures.

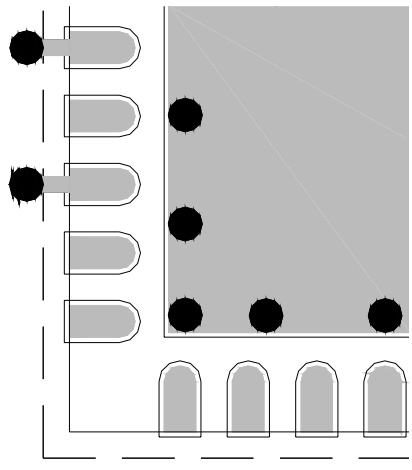


Fig 18. Via placing to connect terminals and center pad

20.1.2 PCB Finish

The packages can be used on a variety of PCB finishes such as immersion gold (Ni/Au) or Hot Air Solder Level (HASL) or Organic Surface Protection (OSP).

Ni/Au finish is recommended. OSP is not recommended in cases that OSP does not withstand a Pb-free or a double-sided reflow application.

20.1.3 Stencil Design

The stencil opening for terminal pads should be 100% of solderland size while the stencil openings of the center/ground pad should be divided in an array, such that 80-90% coverage of the center solderland is achieved. This array of openings minimizes the risk smearing during stencil print and risk of short circuit or voiding during reflow.

Stencil thickness can range from 0.10 mm to 0.15 mm. Using rounded corners, tapered and smoothed walls can further optimize solder paste transfer.

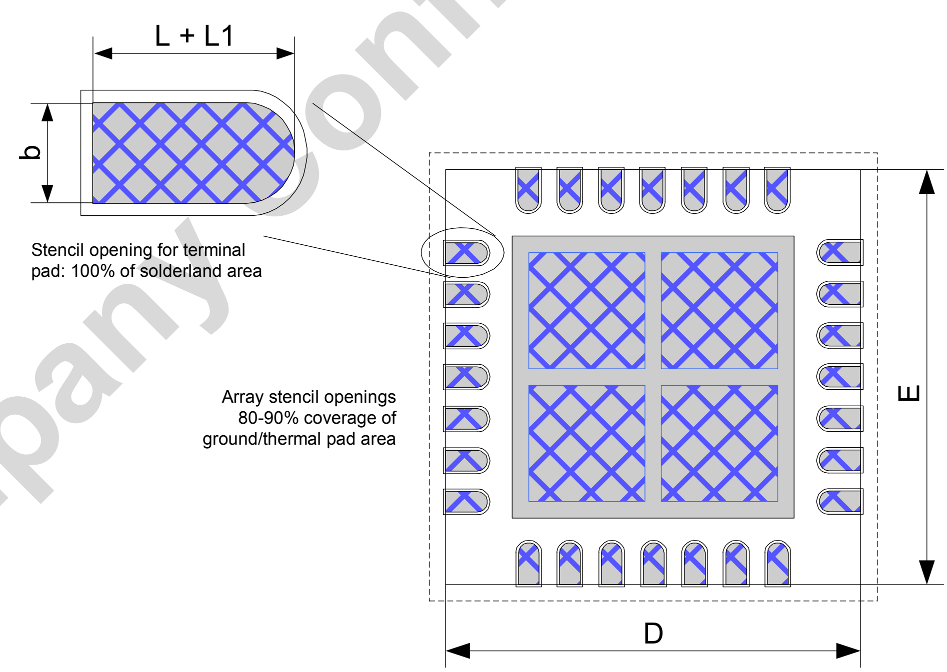


Fig 19. Stencil aperture (hatched area) on solderlands

20.2 Soldering

20.2.1 Solder Paste

Standard (No-clean) Sn/Pb (63%/37%) or Pb-free solder pastes should be used for soldering the package. Solder pastes should be selected based on their printing and reflow behavior. For Pb-free solder paste it is recommended to use "SAC" type solder paste (e.g. SnAg3.8Cu0.7) with melting point of 217°C.

20.2.2 Reflow Profile

Industrial convection reflow oven should be used to mount the packages. The profile depends on the printed circuit board and other components that are used in the customer application. For maximum peak temperature, JEDEC specification should be followed. Following reflow profile and constraints are recommended for eutectic Sn/Pb and Pb-free reflow solders.

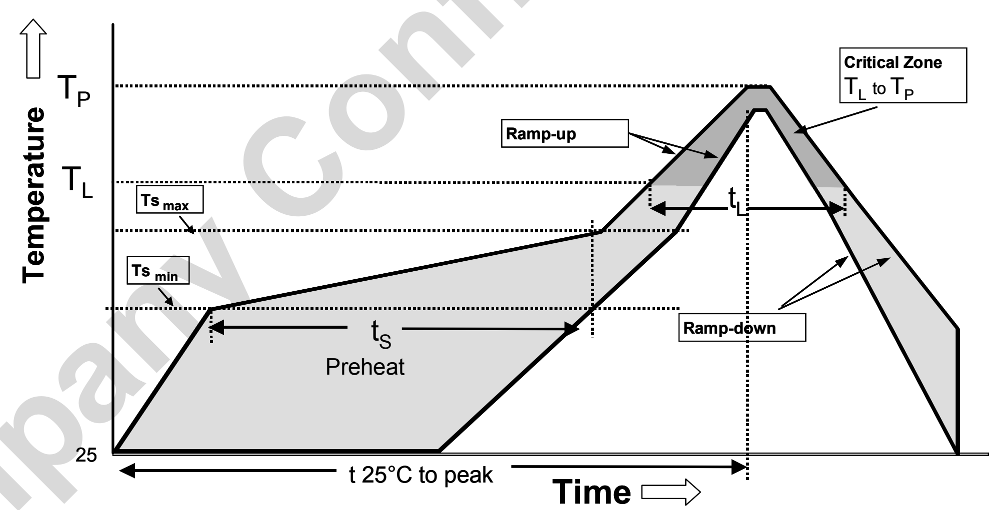


Fig 20. Reflow temperature profile

Table 17: Reflow Soldering Parameters

Parameter	Eutectic Sn/Pb	Pb-free
Average ramp-up rate (Ts_{max} to Tp)	2 °C/second max.	2 °C/second max.[1]
Preheat: – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 100 °C 150 °C 60 - 120 seconds	 150 °C 200 °C 75 - 90 seconds (≤ 0.75 °C/second)
Time maintained above: – Temperature (T_L) – Time (t_L)	 183 °C 60 - 90 seconds	 217 °C 70 - 90 seconds
Max. Peak Temperaure (Tp)	240 + 0/-5 °C	260 + 0 °C

Table 17: Reflow Soldering Parameters *...continued*

Parameter	Eutectic Sn/Pb	Pb-free
Time within 5 °C of actual Peak Temperature (tp)	10 - 30 seconds	20 - 30 seconds
Ramp-Down Rate	> 180 °C: 2 °C/second max. < 180 °C: 6 °C/second max.	> 180 °C: 2 °C/second max.[1] < 180 °C: 6 °C/second max.
Minimum peak temperature (Tp_{min})	205 °C	230 °C
Time 25°C to Tp	4 - 5 minutes	4 - 5 minutes

[1] Ramp-up and -down is lower than specified in JEDEC JSTD-020C.

20.3 Moisture Sensitivity Level

The following minimum moisture sensitivity levels (MSL) are applicable for HLLGA packages.

Table 18: Moisture Sensitivity Levels

Maximum peak temperature (Tmax)	MSL
240 °C	MSL3

20.4 Rework

If rework is needed, then the packages can be removed or reworked using a “BGA” repair station.

The rework process involves the following steps:

- 1) Component Removal
- 2) Site Redress
- 3) Solder Paste Application
- 4) Component Placement
- 5) Component Attachment.

These steps are discussed the following in more detail.

20.4.1 Component Removal

The first step in removal of component is the reflow of solder joints. It is recommended to preheat the PCB to 150 °C using a bottom heater. Heating of the top side of the component should be done using hot air while a special nozzle can be used for this purpose. Excessive airflow should also be avoided since this may cause shifting of adjacent components. Once the joints have reflowed, the vacuum lift-off can start. Because of their small size the vacuum pressure should be kept below 15 inch of Hg. This will prevent damage to the PCB solderland (“pad lift”). The temperature of the package should not exceed 260 °C during this rework process since damage can occur to either the package or the PCB. The temperature profile depends on the customer application.

20.4.2 Site Redress

After the component is removed, the PCB solderland needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and desoldering braid. The width of he blade should be matched to the maximum width of the footprint and the blade temperature should be low enough not to cause any damage to the circuit board.

Flux residues on the PCB can be removed using IsoPropyl Alcohol (IPA).

20.4.3 Solder Paste Application

It is recommended to re-apply solder by dispensing or stencil printing. The amount of solder applied on the terminals should be in the order of 0.08 mg. In case of dispensing, a gage 27 (0.2 mm opening) needle (e.g. white EFD needle) should be used with 0.3 s - 0.4 s shot at 4 bar. For stencil printing a mini stencil of 0.1 mm thickness can be used if application allows room for it.

20.4.4 Component Placement

A BGA repair station has a vacuum pick up tool and usually some component alignment possibilities.

A split-beam optical system should be used to align the component on the solder lands. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes. Manual placement is not recommended, although the package allows 0.1 - 0.15 mm misplacement.

20.4.5 Component Attachment

For re-soldering of the newly placed component, the same profile of bottom and top heating should be applied as described in the step 1), Component Removal.

21. Revision history

Revision history

Rev	Date	Description
02.02	2006 10 18	Format conversion
2.1	2006 09 28	Minor changes
2.0	2006 06 16	Product data initial version

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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