Specification of GD852P Hardware

Version : 1.0

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Content

1.The Introduction of Product

This Product is a type of GSM Telephones, including 96*64 Monochrome LCD Screen。

2. Version

1. 2007/11/7 V1.0

3. The Requirement of Design of GD852P Hardware

3.1 Power Supply

The voltage of CPU is 1.8V，and the voltage of Digital I/O I/F is 2.8V 。

3.2 Screen:

96*64 Monochrome LCD Screen.

3.3 Storage:

4M×16bits NOR Flash+2M×16bits SRAM Storage(TV00560002DDGB TOSHIBA)

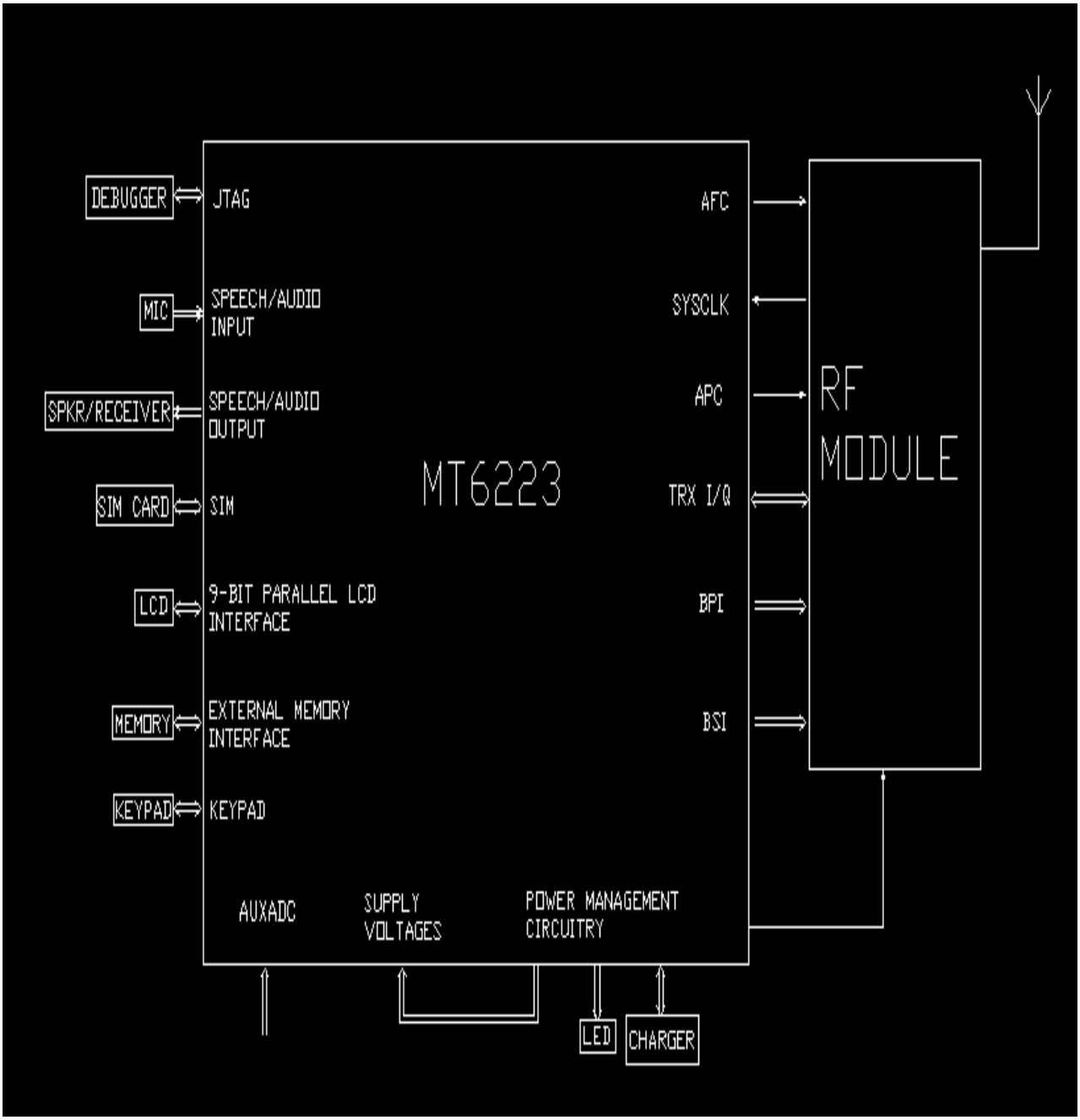
3.4CPU

High-Speed 32 Bit Micro-Controller MT6223 (MediaTek)

3.5 GSM Module

Dual-Frequency Wireless Technique (MTK)

4.The Scheme of GD852P Hardware



5. The Description of Hardcore of GD852P

5.1 CPU MT6223

5.1.1 MT6223 is a kind of high-speed 32 Bit Micro-Processing wafer.

5.1.2 characteristic:

5.1.2.1 Integrated voice-band, audio-band and base-band analog front ends

5.1.2.2 TFBGA 9mm×9mm, 224-ball, 0.5 mm pitch package

5.1.2.3 ARM7EJ-S 32-bit RISC processor

5.1.2.4 High performance multi-layer AMBA bus

5.1.2.5 Java hardware acceleration for fast Java-based games and applets

5.1.2.6 Operating frequency: 26/52 MHz

5.1.2.7 Dedicated DMA bus

5.1.2.8 7 DMA channels

5.1.2.9 320K bits on-chip SRAM

5.1.2.10 On-chip boot ROM for Factory Flash Programming

5.1.2.11 Watchdog timer for system crash recovery

5.1.2.12 3 sets of General Purpose Timer

5.1.2.13 Circuit Switch Data coprocessor

5.1.2.14 Division coprocessor

5.2 Storage Module:

TV00560002DDGB

Characteristic:

5.2.1 Content of FLASH : 4M×16bits

5.2.2 Working Voltage of Write/Read: 2.7-3.3V

5.2.3 Block eraser architecture: 8×4Kwords/127×32Kwords

5.2.4 Bank architecture 16Mbits×4Banks

5.2.5 Boot block architecture: top boot block

5.2.6 Erase/Program cycles: 100，000 cycles typ

5.2.7 Ultra Low Power Consumption：

- Current for Reading：55mA maximum
- Page Read operating：5mA maximum
- Standby Module：10uA maximum

5.3 GSM Specification

On the downlink path, the sub-block between RX mixed-signal module and Baseband Serial Ports is RX Path. It mainly
consists of two parallel digital FIR filter with programmable tap number, two sets of multiplexing paths for loopback modes, interface for RX mixed-signal module, Interference Detection Circuit, I/Q Gain Mismatch compensation circuit, and interface for Baseband Serial Ports.

The purpose of the uplink path inside Baseband Front End is to sink TX symbols, from DSP, then perform GMSK modulation on them, then perform offset cancellation on I/Q digital signals, and finally control TX mixed-signal module to make D/A conversion on I/Q signals out of GMSK Modulator with offset cancellation. Accordingly, the uplink path is composed of uplink parts of Baseband Serial Ports, GSM Encryptor, GMSK Modulator and several compensation circuits including I/Q DC offset, I/Q Quadrature Phase Compensation, and I/Q Gain Mismatch.

General

	Specification
Frequency Range TDMA and AMPS	GSM850 TX :824~849MHz RX:869~894MHz
	PCS1900 TX :1850~1910MHz RX:1930~1990MHz
Channel Spacing	200KHz
Channels	GSM850 : 124 Channels(128~251), PCS1900: 299 Channels(512~810)
	0.3 GMSK Modulation
Transmitter Error Vector Module	Phase rms error: less than 5 degree;
	Phase peak error :less than 20 degree;
Duplex Spacing	GSM850: 45MHz; PCS1900: 80MHz
Frequency Stability	± 0.1ppm
Operating Voltage	DC input: 5.0Vdc +/-10% 500mA
	Battery Operation Voltage: Nominal 3.6Vdc
Transmit Current (Talk mode)	GSM850: Typical 300mA
	PCS1900 : Typical 230mA

Transmitter

	Specification
RF Power Output	GSM850 (33dBm) (power class4)
	PCS1900 (30dBm) (power class1)
Output Impedance	50ohm
Harmonic and Spurious Emissions	Radiated spurious emissions are attenuated below the maximum level of emission of the carrier frequency by at least43+10[log10(mean output power in watts)]

Receiver

	Specification
RX Bit error rate	Less than 2.4 % at -102 dBm (GSM850)
	Less than 2.4 % at -102 dBm (PCS1900)
Channel Hop Time	576.92 usec (TDMA slot)
	4.615msec (TDMA frame)

5.4 Audio Controller Module

5.4.1 Audio

OCP7190 Charactistic

5.4.1.1 Working Voltage:2.2V~5.5V

5.4.1.2 Vdd: 5V,217Hz ;PSRR:62dB

5.4.1.3 Current for Turnoff: 0.1uA

5.4.1.4 Overheat Protector

5.4.1.5 Outer Adjustable Controller

5.4.1.7 BTL output can drive capacitive loads

6. The Description of Circuit of GD852P

The circuit of GD852P includes：

1. CPU Section
2. LCD Section
3. Keyboard Induction Section
4. Storage Section.
5. Audio Controller Section

6.1 CPU Section.

Power and Supply Management:

2.8V to 5.5V Input Range

Charger Input up to 8V

Seven LDOs Optimized for Specific GSM Sub-systems; One LDO for RF transceiver

Two Open-Drain Output Switches to Control the LED and Vibrator

Three NMOS switches to control RGB LEDs

6.2 LCD Section

6.3.1 LCD

96*64 Monochrome LCD Screen

Two LED Light

6.3 Keyboard Scanning Section

MT6223 Special Interface is used for output and input of Keyboard Scanning. The Keystroke includes 0~9, *,#,OK,NO,UP,DOWN,LEFT,RIGHT et al。

6.4 Storage Section

4M×16bits NOR Flash+2M×16bits SRAM Storage

6.5 Audio Controller Section

MT6223 Inner Compositive Coder/Decoder are adopted as Digital/Analogue，Analogue／Digital Coder/ Decoder.

6.6 Keystroke Scanning Section

7. Pin Assign and Function

HA Part	Pin Name	Pin NO	I/O	Connection	Function
JTAG port	JRTCK	U8	O	JRTCK	JTAG test port returned clock output
	JTRST_B	R8	I	JTRST_B	JTAG test port reset input
	JTCK	U9	I	JTCK	JTAG test port clock input
	JTDI	P8	I	JTDI	JTAG test port data input
	JTMS	T9	I	JTMS	JTAG test port mode switch
	JTDO	R9	O	JTDO	JTAG test port data output
RF Parallel Control Unit	BPI_BUS9	U5	IO		
	BPI_BUS8	U4	IO		
	BPI_BUS7	T4	IO	RFVCOEN	RFVCO ENABLE
	BPI_BUS6	R4	IO		
	BPI_BUS5	P3	IO	DCS_ON	DCS ON
	BPI_BUS4	T3	IO	PA_EN	PA ENABLE
	BPI_BUS3	U3	O		
	BPI_BUS2	R3	O		
	BPI_BUS1	T2	O	LB_TX	GSM850 SWITCH
	BPI_BUS0	R2	O	HB_TX	DCS1900 SWITCH
RF Serial Control Unit	BSI_DATA	R5	IO	SYNTHDATA	SYNTH DATA
	BSI_CLK	U6	O	SYNTHCLK	SYNTH CLOCK
	BSI_CS0	T5	O	SYNTHEN	SYNTH ENABLE
PWM Interface	PWM/GPIO25	P7	IO	DISP_LIGHT	LCD BACKLIGHT CONTROL
Parallel LCD Interface	**LCD_D8**	T10	IO	LCD_CLK	LCD CLOCK
	LCD_D7	R10	IO	LCD_SI	LCD DATA
	LCD_D6	P10	IO	LCD_A0	LCD DATA CO
	LCD_D5	U10	IO		
	LCD_D4	U11	IO		
	LCD_D3	T11	IO		
	LCD_D2	R11	IO		
	LCD_D1	U12	IO		
	LCD_D0	T13	IO		
Serial LCD/PM IC Interface	LCD_RSTB/ GPIO8	T12	O	LCD_RST	LCD RESET
	LCD_WR_B	R12	O		
	LCD_RD_B	U13	O		

	LCD_A0	R13	O		
	LCD_CS0_B/ GPIO13	R14	O	LCD_CS	LCD CS
	LCD_CS1_B	U14	O		
SIM Card Interface	SIMIO	B5	IO	SIMDATA	SIM DATA
	SIMCLK	D6		SIMCLK	SIM CLOCK
	SIMRST	C6		SIMRST	SIM RESET
Dedicated GPIO Interface	SYSRST_B	T8	I	/SYSRST	SYSTEM RESET
	WATCHDOG	T14	O	/WATCHDOG	WATCHDOG
Keypad Interface	KCOL0	A13	I	KCOL0	KCOL0
	KCOL1	B14	I	KCOL1	KCOL1
	KCOL2	A14	I	KCOL2	KCOL2
	KCOL3	B15	I	KCOL3	KCOL3
	KCOL4	A15	I	KCOL4	KCOL4
	KROW0	C12	O	KROW0	KROW0
	KROW1	B12	O	KROW1	KROW1
	KROW2	A12	O	KROW2	KROW2
	KROW3	C13	O	KROW3	KROW3
	KROW4	B13	O	KROW4	KROW4
External Interrupt Interface	EINT0	D12	I	INT_HOOK	INT HOOK
	EINT1	B11	I		
	EINT2	C11	I		
	EINT3	D11	I		
External Memory Interface	ED0	T16	IO	ED0	ED0
	ED1	U17	IO	ED1	ED1
	ED2	T17	IO	ED2	ED2
	ED3	P14	IO	ED3	ED3
	ED4	R16	IO	ED4	ED4
	ED5	R17	IO	ED5	ED5
	ED6	P17	IO	ED6	ED6
	ED7	P16	IO	ED7	ED7
	ED8	P15	IO	ED8	ED8
	ED9	N17	IO	ED9	ED9
	ED10	N16	IO	ED10	ED10
	ED11	N15	IO	ED11	ED11
	ED12	M17	IO	ED12	ED12
	ED13	M16	IO	ED13	ED13
	ED14	M15	IO	ED14	ED14
	ED15	L17	IO	ED15	ED15

	/ERD_B	L16	O	/ERD	/ERD
	/EWR_B	L15	O	/EWR	/EWR
	/ECS0_B	L14	O	/ECS0_FLASH	ECS0 FLASH
	/ECS1_B	K17	O	/ECS1_SRAM	ECS1 SRAM
	/ECS2_B	K16	O		
	/ELB	K14	O	/ELB	ELB
	/EUB	J17	O	/EUB	EUB
	EA0	J16	O	EA0	EA0
	EA1	J15	O	EA1	EA1
	EA2	J14	O	EA2	EA2
	EA3	H17	O	EA3	EA3
	EA4	H16	O	EA4	EA4
	EA5	H15	O	EA5	EA5
	EA6	G17	O	EA6	EA6
	EA7	G16	O	EA7	EA7
	EA8	G15	O	EA8	EA8
	EA9	F17	O	EA9	EA9
	EA10	F16	O	EA10	EA10
	EA11	F15	O	EA11	EA11
	EA12	E17	O	EA12	EA12
	EA13	E16	O	EA13	EA13
	EA14	E15	O	EA14	EA14
	EA15	E14	O	EA15	EA15
	EA16	D17	O	EA16	EA16
	EA17	D16	O	EA17	EA17
	EA18	D15	O	EA18	EA18
	EA19	D14	O	EA19	EA19
	EA20	C17	O	EA20	EA20
	EA21	C16	O	EA21	EA21
	EA22	C14	O	EA22	EA22
	EA23	B17	O	EA23	EA23
	EA24	B16	O		
	EA25	P13	O		
	URXD1	C7	I	URXD1	URXD1
	UTXD1	C10	O	UTXD1	UTXD1
	/UCTS1	F10	I		
	/URTS1	E12	O		
	AU_VIN1_P	K2		MICP1	MICP1

Analog Interface	AU_VIN1_N	K1		MICN1	MICN1
	AU_VIN0_N	J2		MICN0	MICN0
	AU_VIN0_P	J1		MICP0	MICP0
	AU_VREF_PO	H4			
	AU_VREF_NI	H3			
	AU_MICBIAS_N	H2		MICBIASN	MICBIASN
	AU_MICBIAS_P	G3		MICBIASP	MICBIASP
	AU_OUT0_P	G2		SPKP0	RECEIVER
	AU_OUT0_N	G1		SPKN0	RECEIVER
	AU_MOUTR	F1		SPKN1	SPKR
	AU_MOUTL	F2		SPKP1	SPKR
	BDLAQP	L1		QP	QP
	BDLAQN	L2		QN	QN
	BDLAIN	L3		IN	IN
	BDLAIP	L4		IP	IP
Supply Voltages	VDDK	N4		VCORE	VCORE
	VDDK	P9		VCORE	VCORE
	VDDK	D9		VCORE	VCORE
	VDDK	H14		VCORE	VCORE
	VDD33	D13		VDD	VDD
	VDD33	P4		VDD	VDD
	VDD33	P5		VDD	VDD
	VDD33_EMI	P12		VMEM	VMEM
	VDD33_EMI	N14		VMEM	VMEM
	VDD33_EMI	M14		VMEM	VMEM
	VDD33_EMI	G14		VMEM	VMEM
	VDD33_EMI	F14		VMEM	VMEM
	VSS33	K7		GND	GND
	VSS33	L7		GND	GND
	VSS33	K8		GND	GND
	VSS33	J11		GND	GND
	VSS33	J7		GND	GND
	DGND	H9		GND	GND
	DGND	H7		GND	GND
	DGND	H11		GND	GND
	DGND	H10		GND	GND
	AVDD_MBUFL	F4		AVDD	AVDD
	AVDD_AFE	K4		AVDD	AVDD

	AVDD_GSMRFTX	J4		AVDD	AVDD
	AVDD_REF	E1		AVDD	AVDD
	AVDD_PLL	M4		AVDD	AVDD
	AVSS_MBUFL	G4		GND	GND
	AGND_AFE	H1		GND	GND
	AVSS_AFE	J3		GND	GND
	AGND_RFE	K3		GND	GND
	AVSS_GSMRFTX	M1		GND	GND
	AVSS_RFE	P1		GND	GND
	AVSS_PLL	T1		GND	GND
	AVDD_RTC	B10		VRTC	VRTC