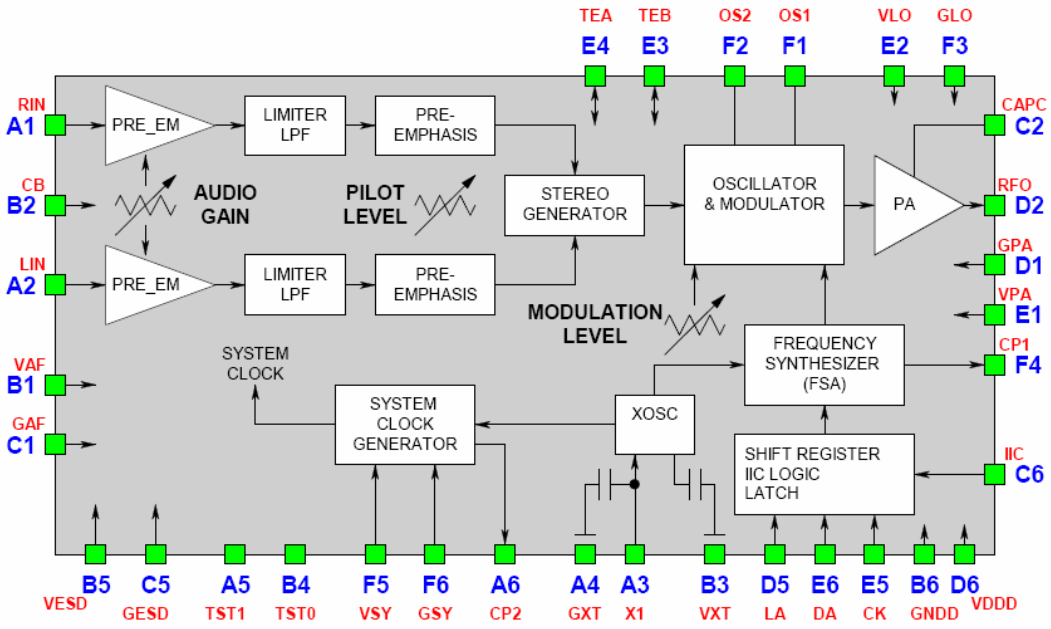
Operation Description

The NS73 is a FM stereo transmitter IC designed for FM transmitter embedded into battery operated portable devices.

Block Diagram of NS73

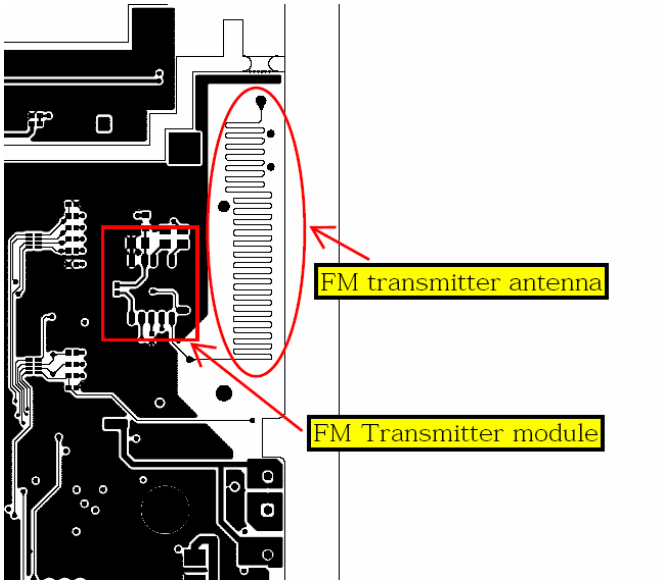


The EUT is composite device, main function is

PMP functions; MP3 play, Navigation,

FM transmitter

A pattern antenna is used on PCB board for transmitting.



NS73
User's Manual
(Ver3.15D)

The NS73 is a FM stereo transmitter IC designed for FM transmitter embedded into battery operated portable devices.
This document is programmer's manual to design software for host processor.

Subject to change without notice due to ongoing development.

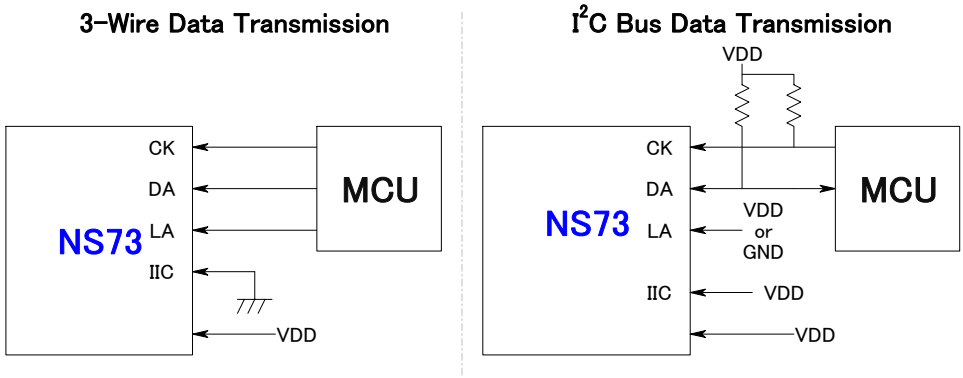
Version History

Version	Paragraph	Description	Revised by	Date
2.3	Register Map	A1]2:0]->A1[1:0] DEV deleted +/-94.5kHx	H. Miyagi	Feb.17,05
2.31	All	Correction of sentence	H. M	Feb. 19,05
2.4	Register Map	Addition Register CIA, CIB	M.Tsubokawa	Feb. 28, 05
2.5B2	All	Register Name Change	M.Tsubokawa	Mar. 11, 05
2.5B2	All	Correct Spell miss	M.Tsubokawa	Mar. 22, 05
2.51B2	All	Correct some miss	M.Tsubokawa	Apr. 01, 05
2.51B2	Data transmission format	Add wave form and those specification	M.Tsubokawa	Apr. 05, 05
2.52B2	Data transmission format	Modify some value	M.Tsubokawa	Apr. 11, 05
2.52B2	Controller basic operation routines	Correct figure	M.Tsubokawa	Apr. 11, 05
2.52B1	All	Make Change to B1	M.Tsubokawa	Apr. 18, 05
3.00C2	All	Make Change to C2	M.Tsubokawa	May. 11, 05
3.10D	Register Map Explanation of the registers operation routines	Make Change to D. Change explanation of register "MUTE". Change chart of operation routines.	M.Tsubokawa	Jul. 25, 05
3.11D	Register Map Explanation of the registers	Delete register "DEV". Change explanation of register "CEX". Change chart of operation routines.	M.Tsubokawa	Jul. 27, 05
3.12D	All	Delete "S32K", "FR" Change Description "PE", "PDX" Add figure "Frequency error" Change "PLT" bit length (3 -> 1) Change Description "CIA"(Current value was made fourth)	M.Tsubokawa	Aug. 10, 05
3.13D	Register Map Operation routines	Change Address8 data ("xx11 1000" -> "xx01 1000")	M.Tsubokawa	Aug. 11, 05
3.14D	Register Map	Change Address4 data ("xxxx xx01" -> "xxxx xx00") Delete figure "Frequency error"	M.Tsubokawa	Sep. 22, 05
3.15D	Explanation of the registers	Add Description "Relationship of PE and PDX" Change CEX explanation	M.Tsubokawa	Oct. 17, 05

1. Block diagram of connection to the MCU (Host Microprocessor)

fig.1

Communication to MCU



The NS73 has two types of serial data interface: 3-wire and I²C bus.
The interface type is selected by level setting of IIC pin.

IIC = 0 (connect to Ground) -→ 3-wire transmission
IIC = 1 (connect to VDD) -→ I²C bus transmission

The function of CK, DA, and LA pins vary according IIC pin setting;

In case of **IIC=0** 3-wire mode (see fig.1);
- CK = Serial clock input
- DA = Serial data input
- LA = Latch input

In case of **IIC=1** I²C mode (see fig.1);
- CK = Serial clock input
- DA = Serial data input and output
- LA = Address Selection.
  - Usually, LA is set to low level (connect to GND).
  - If I²C address conflicts with other I²C devices in same system, set LA to high level (connect to VDD)

Note) Follow below instructions otherwise it may be cause chip damage or improper operation of NS73.

a. The voltage at any pins of NS73 must not exceed VDD+0.3V or below -0.3V.
b. Take same ground potential between NS73 and other devices.
c. Keep low noise level on transmission lines while debugging.

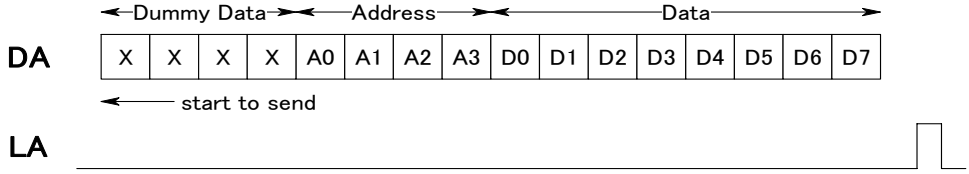
2. Data transmission format for MCU

2.1 3-Wire mode

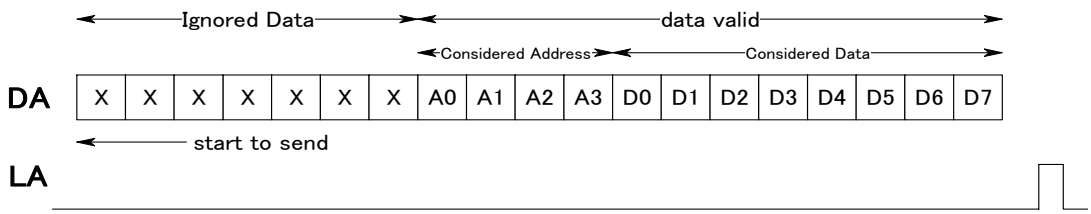
The MCU should send data to NS73 from LSB of Address first and LSB of Data to D7 continuously.
Total transmission data is 12 bits.
After sending all data (12 bit), send latch pulse of active high to LA port.
Then the data sent by MCU is stored into the register of NS73 whose address is assigned by A0 to A3.

In case of using serial interface of MCU with 8 bits data length (hardware data transmission), the data is sent twice continuously.
First 8 bits of transmission is address with dummy data (see fig-2) and next 8-bit is data. Dummy data should be sent at first.

fig−2a
The first 4 bits dummy data is needed when 2 bytes data transmission is used.

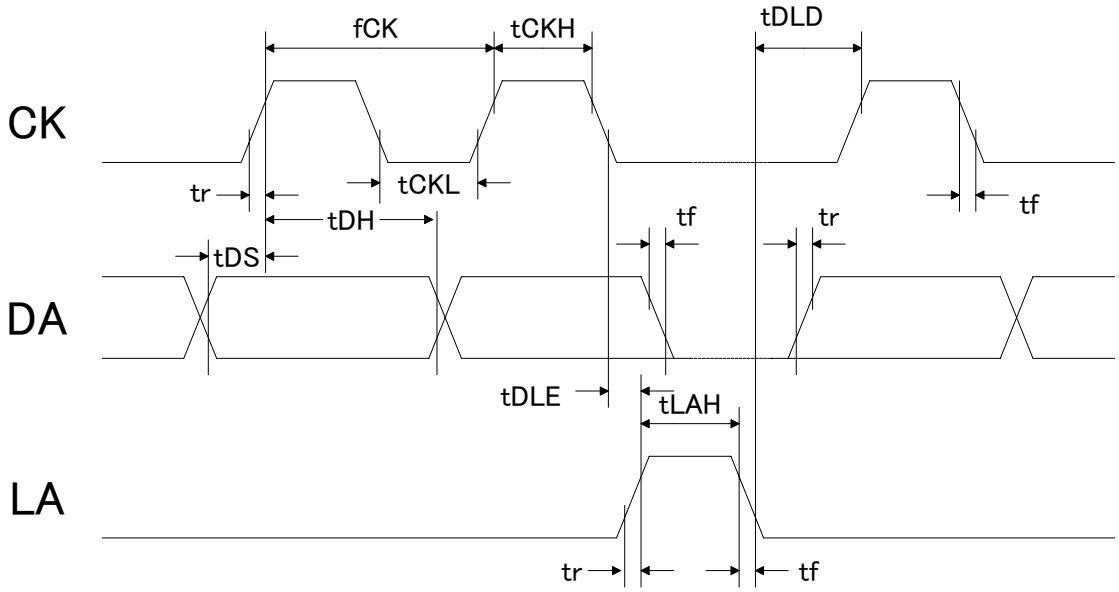


fig−2b
The last 12 bits data is valid if more than 12 bits data is sent



The last 12 bits (12 bits before latch pulse) are acceptable as valid data.

Wave form



AC characteristics

No.	Parameter	Symbol	Min.	Max.	Unit
1	CK frequency	fCK		1	MHz
2	Low period of the CK clock	tCKL	250		nS
3	High period of the CK clock	tCKH	250		nS
4	Rise time of CK, DA, LA	tr		125	nS
5	Fall time of CK, DA, LA	tf		125	nS
6	Data setup time	tDS	100		nS
7	Data hold time	tDH	100		nS
8	Latch enable time between CK clock	tDLE	0		nS
9	Latch disable time between CK clock	tDLD	0		nS
10	High period of LA pulse	tLAH	250		nS

DC characteristics

No.	Parameter	Symbol	Min.	Max.	Unit
1	Low level input voltage	VIL	-0.3	0.25VDD	V
2	High level input voltage	VIH	0.75VDD	VDD+0.3	V
3	Hysteresis of Schmitt trigger input	Vhys	0.05VDD		V
4	Input current (Input voltge 0.1~0.9VDDmax)	Ii		10	uA
5	Capacitance for each I/O pin	Ci		10	pF

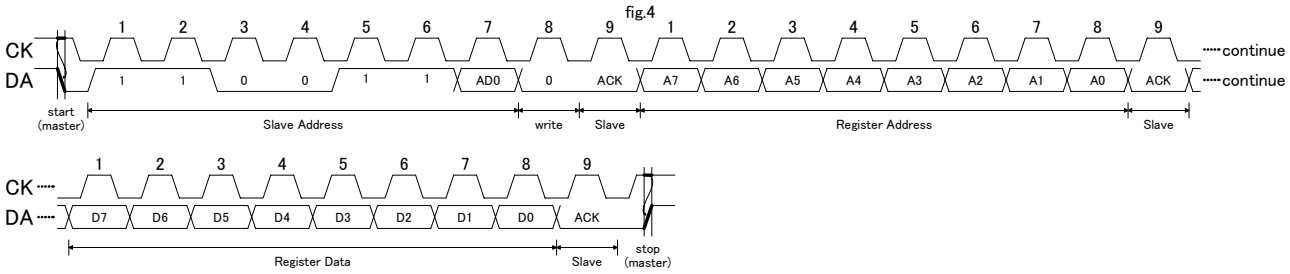
2.2 The I²C bus mode

Note that address and data are sent from MSB to LSB as contrasted with 3-wire method that sends serial data from LSB to MSB for address and data.

All CK(clock) should be generated by MCU.

Write mode (MCU to NS73)

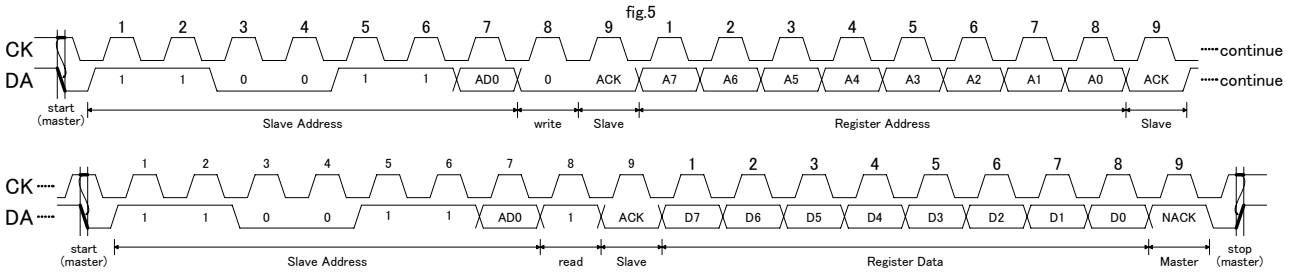
fig.4



Read Mode (to MCU from NS73):

MCU sends address to be set of NS73 to NS73, then MCU reads data of NS73.

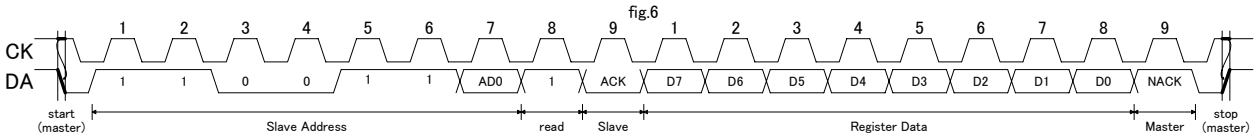
fig.5



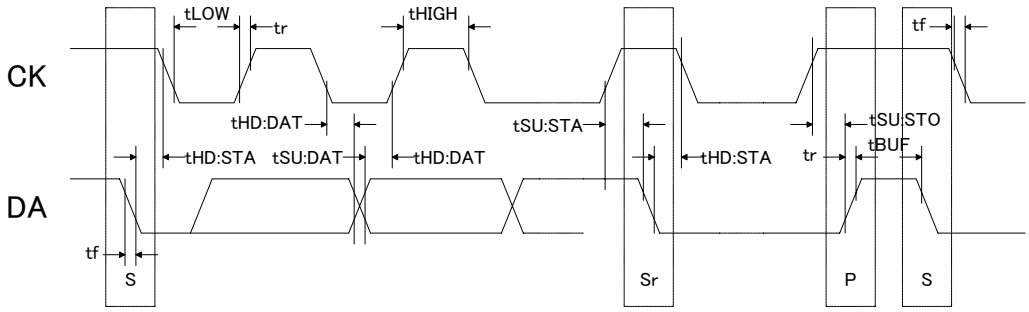
Dummy Read:

This is used as initialization.

fig.6



Wave form



AC characteristics

No.	Parameter	Symbol	Min.	Max.	Unit
1	CK frequency	fCK		400	kHz
2	Hold time START condition	tHD:STA	250		nS
3	HIGH period of the CK clock	tHIGH		0.6	uS
4	LOW period of CK clock	tLOW		1.3	uS
5	Set-up time for a repeat condition	tSU:STA		0.6	uS
6	Set-up time for a stop condition	tSU:STO	0.6		uS
7	Data hold time	tHD:DAT	0	0.9	uS
8	Data set-up time	tSU:DAT	100		nS
9	Rise time of both DA and CK	tr		300	nS
10	Fall time of both DA and CK	tf		300	nS
11	Bus free time between a STOP and START condition	tBUF	1.3		uS

DC characteristics

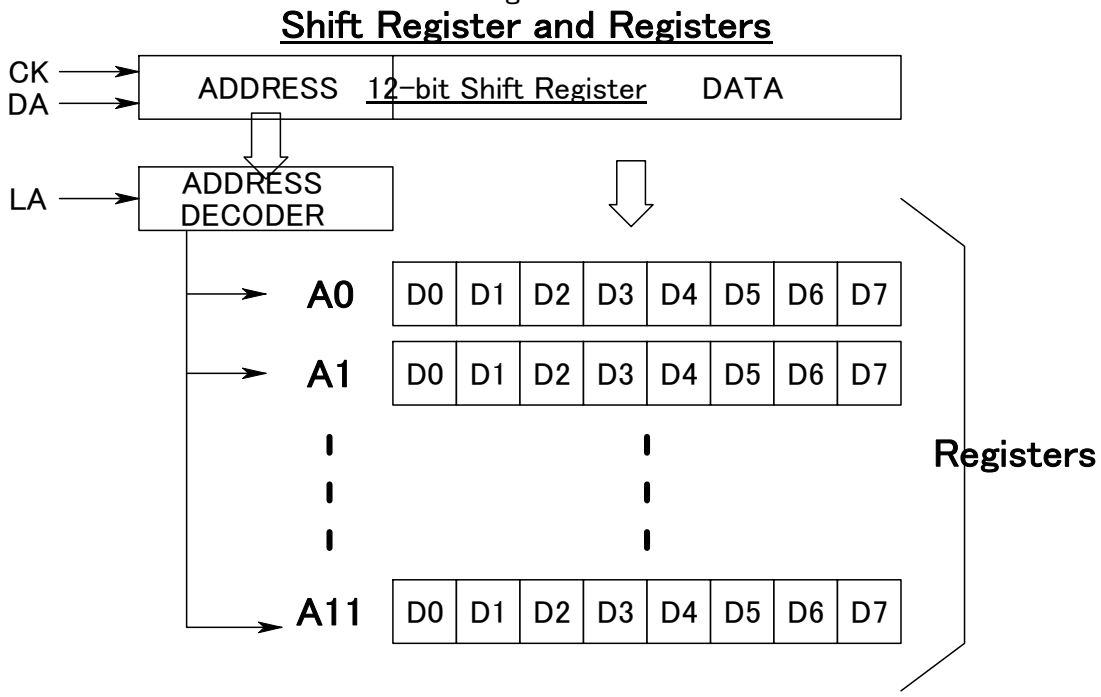
No.	Parameter	Symbol	Min.	Max.	Unit
1	Low level input voltage	VIL	-0.3	0.25VDD	V
2	High level input voltage	VIH	0.75VDD	VDD+0.3	V
3	Hysteresis of Schmitt trigger input	Vhys	0.05VDD		V
4	Low level output voltage at 3mA sink current	Vol		0.4	V
5	Input current (Input voltge 0.1~0.9VDDmax)	Ii		10	uA
6	Capacitance for each I/O pin	Ci		10	pF

3. Register configuration of NS73

3.1 Block diagram of register

The NS73 has registers to interface between MCU.
There are 8 bits latches in a register address and total 12 registers.
These registers are assigned by the address as A0 to A11.
Following is the case for 3-wire mode.

fig-8



Although the software-reset function is assigned to the address 14, no register for this function exists.

The data (DA) is sent from MCU synchronized with clock (CK).
The clock for 3-wire and I^2C are generated by MCU.
Then latch signal(LA) enables to transfer the data in the shift register to register which address is assigned by the first four bits of shift register (in case of 3-wire).
Therefore, the addresses of A12(0Ch), A13(0Dh) and A15(0Fh) are ignored even when they are sent.

3.2 Register map

Table-1 shows the register map of NS73.
The fixed data areas are used for chip test and setting conditions. Therefore, the fixed number should be kept as assigned.

Table-1 **Register Map**

Note.1) The letters written in blue show symbol name of items. Note.2) The fix numbers as "0" should be set "0" at anytime. Note.3) Default = all "0"
Note.4) X = don't care Note.5) Recommended value is meshed.

Address (A0 A1 A2 A3)	D0	D1	D2	D3	D4	D5	D6	D7
0 (0000)	**PE** Analog circuit Power enable 0 = Chip Off 1 = Chip On	**PDX** Xtal OSC enable 0 = Xtal On 1 = Xtal Off	**MUTE** Audio Mute 0 = Unmute 1 = Mute	0	**EM** Pre-emphasis switch 0 = pre-emphasis 1 = through	**EMS** Pre-emphasis Selection 0 = 50uS 1 = 75uS	**AG** Audio Input level to get 100% modulation 0 0 = 100mV 1 0 =140mV 0 1 = 200mV 1 1 = X	
1 (1000)	0	0	1	**PLT** Pilot tone enable 0 = Pilot on 1 = Pilot off	1	1	**SUBC** Forced Subcarrier OFF 0 = On 1 = Off	1
2 (0100)	**PL** TX Power Level 0 0 = X 1 0 = 0.5mW 0 1 = 1.0mW 1 1 = 2.0mW		**ULD** Unlock detect 0 = Disable 1 = Enable	0	0	0	0	0
3 (1100)	**P** LSB Program Data for Synthesizer (Lower Byte) P0 - P7 See explanation for detail							
4 (0010)	**P** Program Data for Synthesizer (upper Byte) P8 - P13 MSB See explanation of items						0	0
5 (1010)	0	0	0	0	0	0	0	0
6 (0110)	0	**CIA** Main Synthe. Charge Pump current 0 0 = 20uA 1 0 = 1.25uA 0 1 = 5uA 1 1 = 80uA		**CIB** Clock Gen. Charge Pump current 0 0 = 80uA 1 0 = 5uA 0 1 = 20uA 1 1 = 320uA		0	0	0
7 (1110)	0	0	0	0	0	0	0	0
8 (0001)	**CEX** L. Osc. freq. extension [0:1]		0	1	1	0	0	0
9 (1001)	0	0	0	0	0	0	0	0
A (0101)	0	0	0	0	0	0	0	0
B (0110)	0	0	0	0	0	0	0	0
E (0111)	**SRST** Software Reset 1 0 1 0				0	0	0	0

** Explanation of the registers

Terminology;

Ax[y] shows bit y of address Ax. If bit shows like[1:3], this means that bit 1, 2 and 3 are used.

The “b” is added for showing binary code and “h” is added for hexadecimal and no suffix shows for decimal. The suffixes are put at lowest digit side.

Example) 00111001b = 39h = 57 h93 shows hexadecimal starting from LSH

PE A0[0]: Analog circuit Power enable

This command can be used as the analog circuit power switch.

PE = 0; Analog circuit power off

PE = 1; Analog circuit power on

This command is used to set standby mode combined with "PDX" = "1". This mode costs only a few microampere currents.

PDX A0[1]: Crystal Oscillator enable

This command can be used as the digital circuit power switch and the oscillator power switch.

PDX = 0; Crystal Oscillator enable

PDX = 1; Crystal Oscillator disable

This command is used to set standby mode combined with "PE" = "0". This mode costs only a few microampere currents.

Relationship of PE and PDX

PE	PDX	
0	0	Don't use (only Analog circuit nonactive)
0	1	Standby Mode
1	0	Power ON
1	1	Don't use(only Crystal nonactive)

MUTE A0[2]: Muting

This command can be used to mute audio signal. It gets impossible to be recognized to be a stereo to grow without pilot signal when it transmitted a message as a stereo.

MUTE = 0; Un-muting

MUTE = 1; Muting

EM A0[4]: Pre-emphasis enable/disable

EM = 0; Pre-emphasis activating

EM = 1; Pre-emphasis Off (frequency response flatness until 15kHz)

EMS A0[5]: Pre-emphasis time constant selection

Set appropriate pre-emphasis level for each countries and area.

EMS = 0; set 50uS

EMS = 1; set 75uS

AG A0[6:7]: Audio input level selection to reach full level deviation

Select 100mV (0 0) for low level of signal source and select 200mV(0 1) for high-level signal source.

A0[6]	A0[7]	Audio input level
0	0	100mVrms
1	0	140mVrms
0	1	200mVrms
1	1	don't care (test mode)

For example, if A0[6:7] is set to [0:1], 100% modulation index can be achieved at 200mVrms input.

If you need to decrease gain, connect a resistor in series to each of Left and Right input.

If you want to operate NS73 with low input level signal, add the low noise amplifiers before Left and Right input.

PLT A1[3]: Pilot tone enable

PLT = 0; Pilot signal on

PLT = 1; Pilot signal off

SUBC A1[6]: Subcarrier enable/disable

SUBC = 0 (Subcarrier ON) + PLT = 0 ; Stereo mode

SUBC = 1 (Subcarrier OFF) + PLT = 1 ; Mono mode

PL A2[0:1]: TX Output power selection

A2[0]	A2[1]	Output Power
0	0	don't care (test mode)
1	0	0.5mW
0	1	1.0mW
1	1	2.0mW

Note): (1) above absolute values are not guaranteed.
It is just indication of output power level.
The output power depends on the number of RF LPF or power supply voltage. However, the power level will maintain a certain level.
(2) The radiated signal level should follow rules and regulations in each country.

ULD A2[2]: Synthesizer Unlock Detection activated
ULD = 0; Disable the unlock detection. The TX signal is radiated from antenna even when PLL of synthesizer is not locked.
ULD = 1; Unlock detection is activated. During unlocked condition of the loop of synthesizer, the TX power output is inhibited automatically (no signal at antenna appears).

P A3[0:7] + A4[0:5]: TX frequency generation program for the synthesizer
A3[0] is LSB of program data and A4[5] is MSB of program data.
Available program data range is from 256(00 0001 0000 0000b=100h) to 16383(11 1111 1111 1111b=3FFFh).
The program data should be -304kHz offset for desired frequency generation.
Refer to programming of frequency by the synthesizer.

CIA A6[1:2]: Main synthesizer Charge Pump current selection

A6[1]	A6[2]	Charge Pump current
0	0	20uA
1	0	1.25uA
0	1	5uA
1	1	80uA

CIB A6[3:4]: Clock generator Charge Pump current selection

A6[3]	A6[4]	Charge Pump current
0	0	80uA
1	0	5uA
0	1	20uA
1	1	320uA

CEX A8[0:1]; Local oscillation frequency extension
The typical value of oscillation frequency on Simulation;

A8[0]	A8[1]	Audio input level
0	0	101.1MHz - 108MHz
1	0	97.3MHz - 101MHz
0	1	90.1MHz - 97.2MHz
1	1	87.5MHz - 90MHz

Note that the VCO gain, which affects to PLL loop response, should vary in each selection.
The VCO gain of A8[0:1]=(0,0) is highest and (1,1) is lowest.

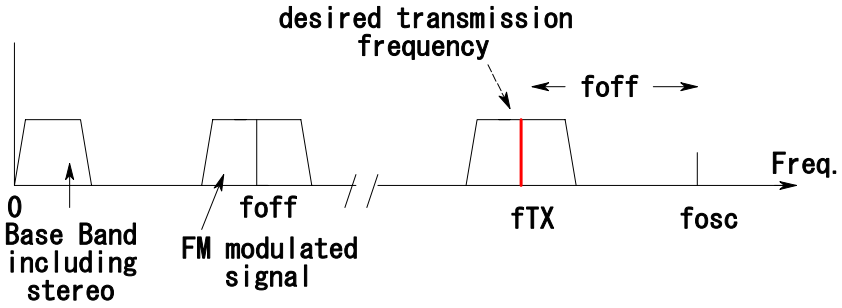
The loop response of the synthesizer is usually negative, i.e. if VCO frequency increases, the control voltage works to decrease until reaching stable condition of VCO frequency.
But in case of NS73, the PLL of synthesizer behaves as positive loop, i.e., if VCO frequency increases, the control voltage will also increase.

Programming of TX frequency for the synthesizer (MCU side programming)

Although the local oscillator is oscillating at 4 times of transmitted frequency, transmitted frequency can be used to calculate the number to program for the synthesizer because of the divided-by 4 pre-scaler between the local oscillator and the synthesizer.

It is also considered that the oscillation frequency(fosc) should be located below the transmission frequency(fTX).
Because the base band signal is modulated in FM with 304kHz offset(foff)
Following shows the frequency spectrum of NS73.

fig-9



Therefore, the fosc should be (fTX + foff).

This is applied to decide divided-by N of synthesizer.

The reference frequency of the synthesizer is taken as 8.192kHz or frequency of divided-by its integer-N.
However, the FM channel steps such as 50kHz, 100kHz and 200kHz are not divisible by 8.192kHz and its divided-by N.
Then, we have to accept some error frequencies from proper transmission frequency.
In order to satisfy the frequency, the divided-by ratio (N) is calculated as;

Choose the reference frequency of synthesizer to 8.192kHz, i.e.,

N = (fTX[MHz] + foff[MHz]) / 0.008192[MHz]

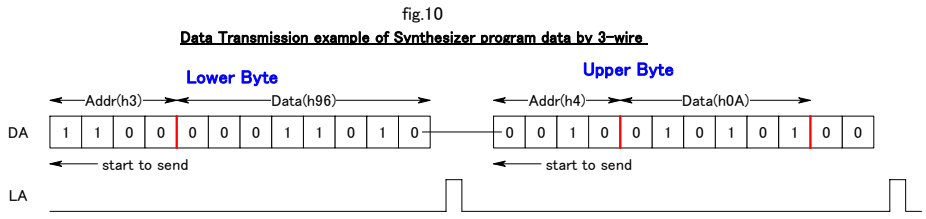
and round off the N to zero decimal places (integer).
Convert N to Nh and Nb.
Set Nb to shift register of transmission with LSB first for 3-wire serial mode or MSB first for I²C bus transmission.

For example) fTX=88.5MHz

N = (fTX + 0.304) / 0.008192 = (88.5 + 0.304) / (0.008192) = 10840.332...
N = round(N,0) = 10840
Nh = 2A58h Nb = 10 1010 0101 1000b
Data transmission for 3-wire is; start “0001 1010 0101 01” -end of bit
Data transmission for I²C is start “10 1010 0101 1000” -end of bit.

Total data transmission for above data to NS73 can be shown as below;

fig.10

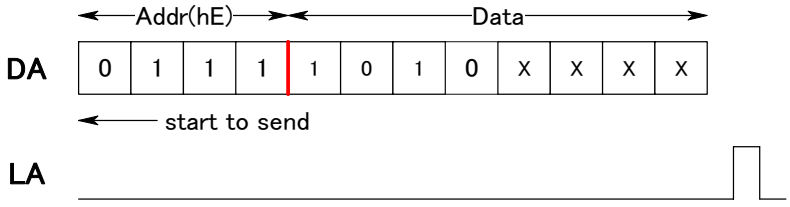


The figure below showed maximum frequency error with transmission frequency and the frequency that were really output of case using the crystal which satisfied tolerance of +/-20ppm.
In case using the crystal which does not satisfy tolerance of +/-20ppm, that error fits into a limit shown in follows is not guaranteed.

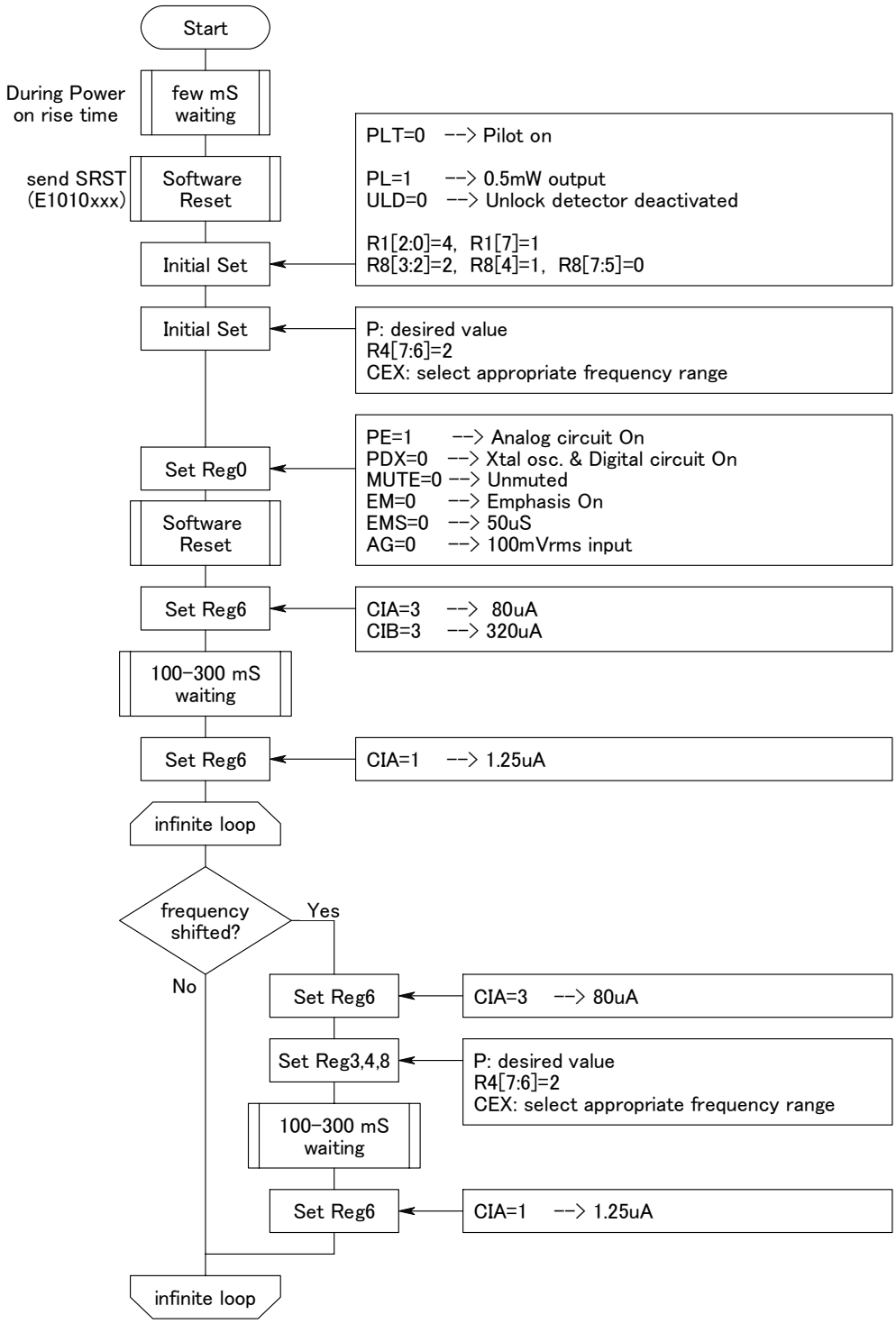
SRST AE[3:0]: Software reset

If Address “E” and bit : AE[0]=1, AE[1]=0, AE[2]=1, AE[3]=0, AE[4:7]=X (don’t care) are applied to NS73, DSP section and other counters are reset to zero. This function can be used as forced reset of the system logic.

fig-12



4. NS73 Controller basic operation routines



NS73 has power on reset circuit. Because this function works, has to wait for a few milli-seconds until VDD reaching specified value.

Next step, set appropriate data to all registers, refer to register map.
After having set all register, a software reset is done to make collection normal condition. Even if a software reset is done, data of register is held.