EZReader HF and Auto-Tune Antenna
Hardware Theory of Operation

By Ray Hillegass

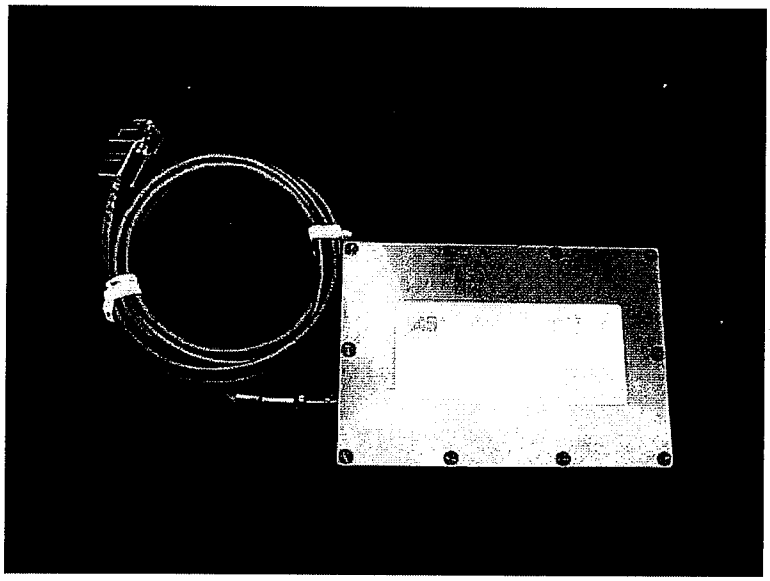

Table Of Contents:

1.0 Power Supply PCB 3
1.1 Input Filter section: 3
1.2 Switching Section: 3
1.3 Regulator Section: 4
1.4 I/O section: 5
2.0 Reader Board PCB 7
2.1 RF Transceiver: 7
2.2 RF Amplifier: 8
2.3 Transmit Filter: 10
2.4 Peak Detector: 10
2.5 Antenna and Setup Port Communication Module: 11
2.6 RS422/RS232 Host Communication Module: 12
2.7 Ethernet Module: 13
2.8 Micro Controller Module: 14
2.9 Memory Module: 15
3.0 Auto-Tune Antenna 16
3.1 Matching and Frequency Tuning Circuitry: 16
3.2 Envelope Detector: 16

1.0 Power Supply PCB

1.1 Input Filter section:

Referring to Figure 1 CN1 is the DC power input connection of the power supply. Pins 1 and 2 are the plus and minus DC input pins with pins 3, 4 and 5 providing connection to earth ground. Input voltage range is between 10 to 30 VDC. TVS 5 and 7 provide over voltage protection for both the plus and minus input individually to earth ground. CM1 is a 2 line common mode choke with an impedance of 700 ohms at 100 MHz with the current capability of 4 amps. L1 and L2 are EMI filters with a center capacitance of 2200PF and a cut off frequency of 3 MHz, their current capability is 5 amps. The combination of CM1, L1, L2 and all associated capacitors comprise the input filtering stage. Diode D2 provides reverse connection protection.

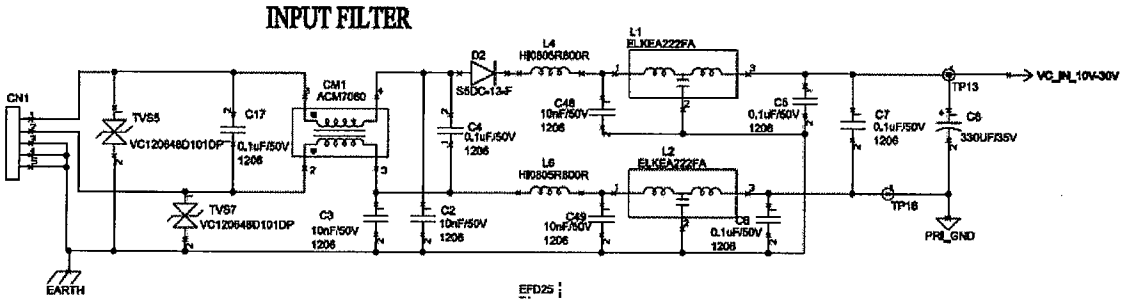

Figure 1

1.2 Switching Section:

Figure 2 shows the switching power supply section, the main components are U1, U2, U3, T1, and Q1. U1 is the LM3478 a Low-Side N-FET switching regulator controller. The switching frequency of U1 is controlled by R1 (91K) which is approximately 200 kHz. Q1 is a MOSFET and is used for switching the primary side of T1. Transformer T1 has a single primary winding and two secondary windings. The topology of the switching power supply provides isolation between input and output voltages. There are two voltages developed 18 and 7 VDC. The 18 VDC is truly regulated while the 7 VDC is quasi regulated based on 18 VDC developments. The 18VDC is set using U2 in combination with R8 and R9. U2 is a programmable shunt regulator with an internal reference of 2.5V. The output voltage is given by the following formula:

$$V_{out} = 2.5\ (1 + R9/R8)$$

Isolation between primary and secondary is kept in tact by the use of U3 an optocoupled phototransistor. The cathode of shunt regulator U2 is connected to the cathode U3, when the voltage at TP14 reaches 18 VDC the cathode of U2 shunts to signal SEC_GND which turns on opto U3's transistor. The collector of U3 is connected directly to U1's internal error amplifier's output (pin 2). This connection provides closed loop regulation while maintaining isolation. The 18 VDC output is capable of 1.5 amps of current while the 7 Volt output is good for 100 to 200ma of current.

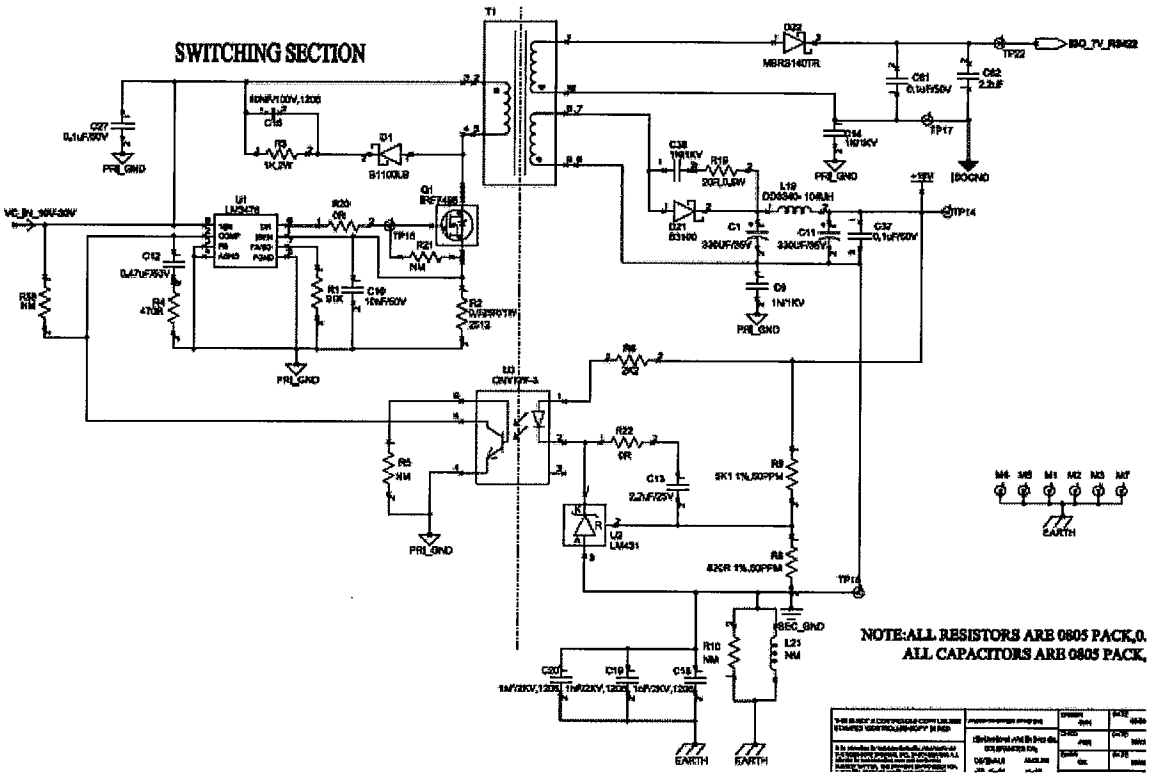

Figure 2

1.3 Regulator Section:

There are three regulators in this area, two linear U8, U9 and one switching U10. U8 and U9 are 12 and 5 volt outputs and provide power for the I/O section of the power supply board. U10 is a switching regulator with an 8 VDC output. This output is feed directly to the reader board where it is further regulated down to required levels. U10 was chosen to be a switching type regulator to provide a intermediate voltage to the reader's linear regulators which helps to significantly reduce their thermal dissipation.

Commom Mode Chokes CM2 and CM3 help to reduce switching noise generated by U10 and the switching power supply section before these voltages are feed to the reader board.

1.4 I/O section:

This section consists of two main parts Trigger Inputs and Relay Outputs. The Trigger Inputs circuitry conditions external signals that allow the reader to function autonomously when properly configured. Referring to Figure 3 external triggers signals can be ether Isolated or Non-Isolated. Isolated trigger require that both the positive and negative side of the signal be presented to the reader. These signals are feed to U24 and U25 which are Opto-Isolators thru CN4 pins 2,10,3 and 4. R38 and R39 are current limiting resistors and allow the outputs of U24 and U25 (pin 6) to turn on with an applied voltage between 5 and 24 VDC. The non-isolated inputs are normally used when the reader is supplying power to an external sensor such as a Photo-Eye. These inputs (CN4 pins 1 and 9) are active low and generally connected to the sinking output of a Photo-Eye. Both Isolated and Non-Isolated inputs eventually cause U19 pins 11 and 13 to go low when active. U19 is a Schmitt Trigger Hex Inverter. Using inverters with a Schmitt Trigger inputs allows for the inputs to be filtered using simple RC circuits which helps to reduce false triggers due to noise spikes while still maintaining clean on and off output transitions.

Power (12VDC) is available at CN4 pins 5,12 for +V and pins 6,13 for –V. This power is limited to a maximum current draw of 200 ma by FUSE1 which is a resettable PTC type.

Two Form-A solid state Relays contacts are also provided at CN4 pins 14, 15 and 7, 8 respectively. These contacts are controlled thru U18 and U21 and have optically isolated control lines. The relays outputs are configured so that either AC or DC voltages can be controlled.

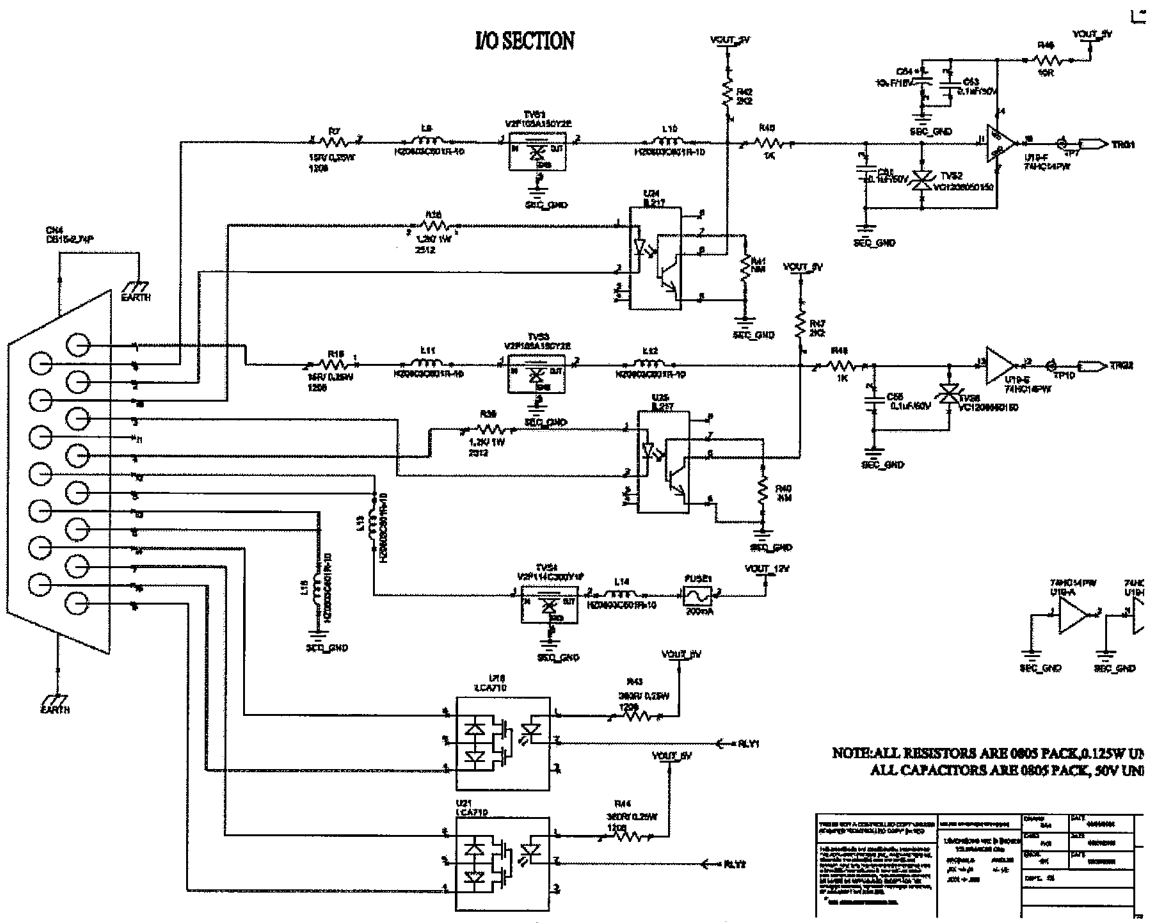
I/O SECTION
VOUT_5V
VOUT_12V
SEC_GND
EARTH
TRG1
TRG2
RLY1
RLY2
FUSE1
200mA
LCA710
NOTE:ALL RESISTORS ARE 0805 PACK,0.125W UN
ALL CAPACITORS ARE 0805 PACK, 50V UN

Figure 3

2.0 Reader Board PCB

2.1 RF Transceiver:

Referring to Figure 4 the transceiver (U14) provides the receive/transmit functions required to communicate with a variety of transponders that operate in the 13.56 MHz ISM band. U14 can be operated in one of two modes, one mode uses built in register configurations that automatically encodes the TX data and decodes the RX data that is present on the 3 wire digital interface. The second mode of operation is know as "direct mode" requires the controller to do all of the encoding and decoding of RF data in and out of the IC. This mode is used for communicating with transponders whose Air to Air protocol is not built into the on chip configurations.

The 3 wire digital interface that connects the transceiver (U14) to the microcontroller (1) consists of pins 11, 13, and 15. Note the pin 15 "SCLOCK" is bi-directional in nature. When communicating with U1 care must be taken to constantly monitor the FIFO buffer as it is 16 bits deep. U14 runs off a 13.560 MHz crystal (Y3) which provides internal clock signals along with RF signal present at pin after running thru an internal RF amplifier.

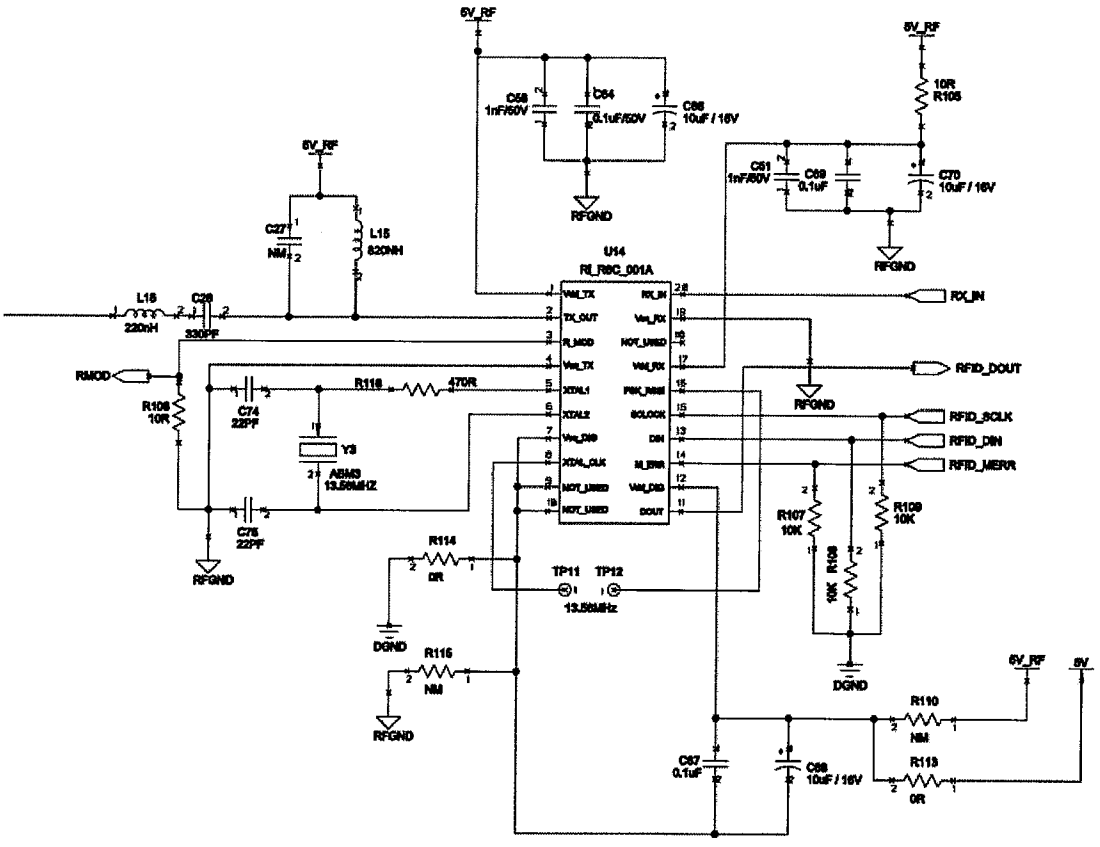

Figure 4

2.2 RF Amplifier:

Referring to Figure 5 the RF Amplifier section is comprised of F3, F2 and Q2. The RF transmit signal from U14-2 is fed to the gate of F3 via components C26, L18, and R22 which provide impedance matching. AM modulation of the carrier is accomplished by Q2 and F2. The signal "RMOD" which comes from U14-3 is capacitively coupled into the base of Q2 to eliminate any possible DC bias, as Q2 is turned on and off it in turn causes F2 to also turn on and off. F2 is connected directly across R72 shunting it out when turned on. R72 is the source resistor for F3 when it is not shunted by F2 the signal at the drain of F3 decreases when it is shunted out (F2 on) the level at F3 increases, this increase and decrease in signal produces an AM modulate signal. The modulation depth is controlled by the value of R72, a larger value increases the modulation depth and vice versa.

The amplifier is capable of delivering +31 dBm of RF level when directly measured at the RF_Out point of the TX Filter. The output level is adjusted by varying the DC supply voltage at L31. The output is normally set to 29.5 dBm. See Variable Supply For RF Amplifier section for details on power adjustment.

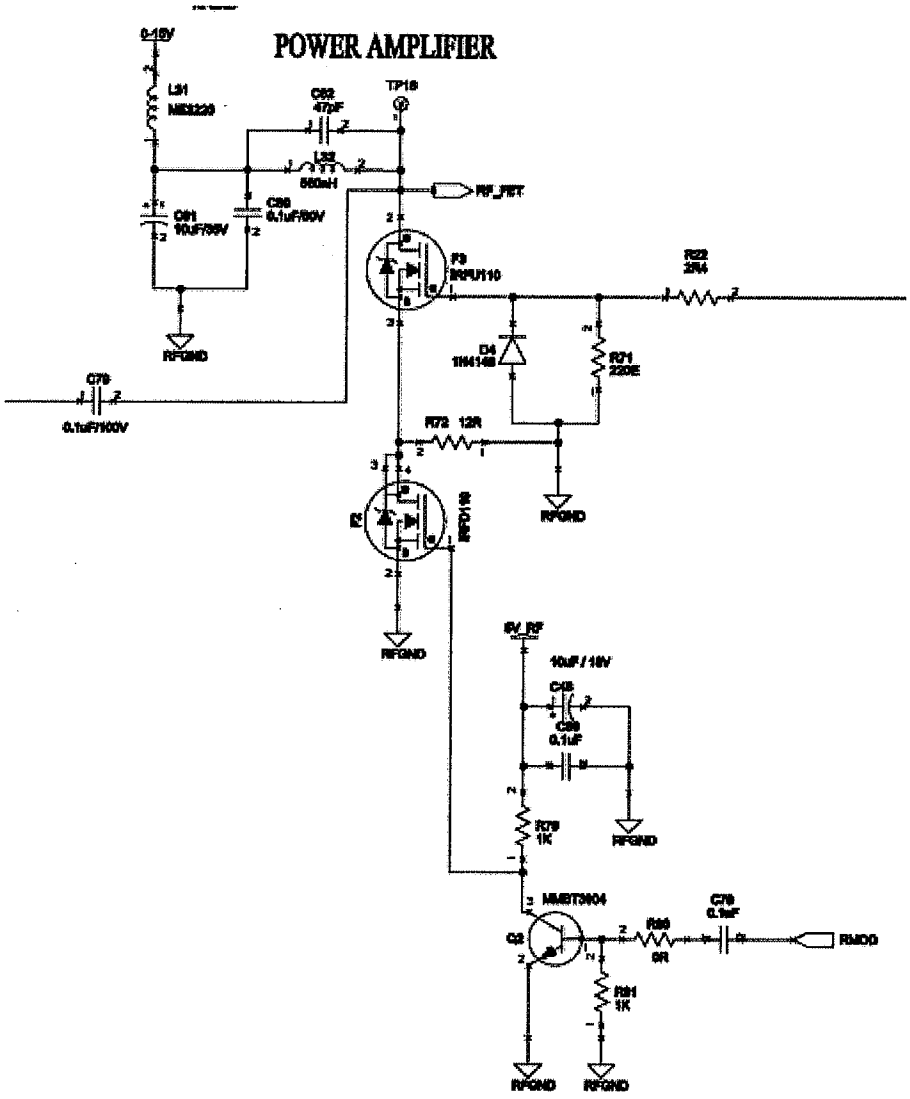
POWER AMPLIFIER
0-10V
L31
C62
47pF
TP19
L32
560nH
RF_FET
C61
10UF/50V
C60
0.1uF/50V
RFGND
F3
IRFU110
R22
2R4
D4
1N4148
R71
220E
C79
0.1uF/100V
R72 12R
RFGND
F2
IRFD110
RFGND
5V_RF
10uF / 10V
C45
C59
0.1uF
R79
1K
RFGND
MMBT3904
C78
0.1uF
Q2
R80
0R
RMOD
R81
1K
RFGND
RFGND

Figure 5

2.3 Transmit Filter:

Figure 6 shows the Transmit Filter, it is a low pass Chebyshev type. Parts C71, L20, L29 and C54 form a PIE network that is used to transform the higher impedance of the RF Amplifer's output down to 50 ohms. Components L14, L13, L16, C35, C34, C88, C37, C90, C45 form the 7th order Chebyshev filter, which has its corner frequency set slightly above 13.56 MHz with a theoretical attenuation curve of 42 dB per octave. This filter reduces harmonics generated by the RF Amplifier down to acceptable levels. The filter also helps to reduce any harmonics generated by the peak detector by placing the RF_IN point one section down from the RF_out point.

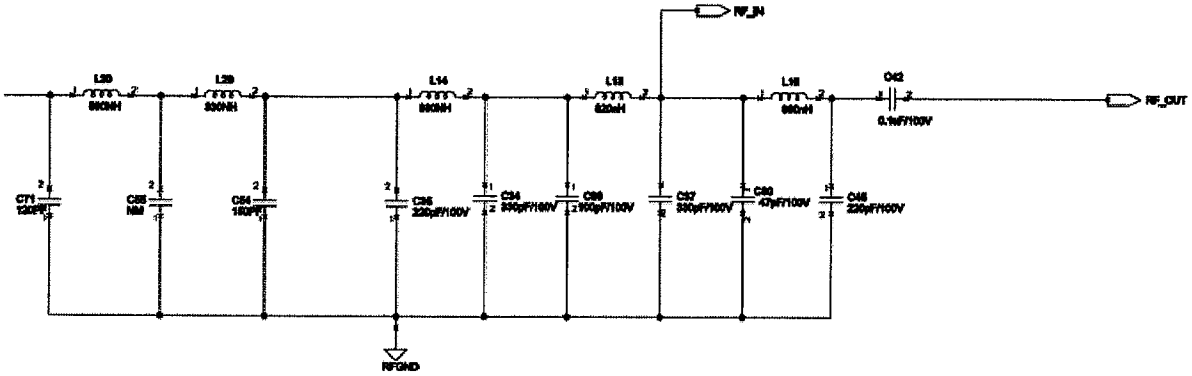

Figure 6

2.4 Peak Detector:

Figure 7 shows the Peak detector(aka Diode detector) circuitry it connects the RF output to the RF input. Signals received from the transponder are present at the same time the transmitter is present due to the fact that the transmitter signal is powering the transponder. The peak detectors purpose is to reduce the level of the carrier present at the receiver which prevents the receiver from being overloaded while not reducing the level of the already small receive signal. The transponder communicates using load modulation. For example the tag can use two subcarriers (423kHz and 484kHz) to modulate itself and thus change the load placed on the carrier. Using these two frequencies the tag will create a side bands (upper shown as example) that are 13.560MHz + (423kHz and 484 kHz) = 13.983 and 14.044 Mhz. These signals along with the carrier (13.560 Mhz) are fed to the peak detector, D3 blocks any negative voltage swings and since it is a non-linear device it also acts as an ideal mixer. Mixing these signals together results in the following frequencies:

13.560 MHz ---------- Carrier
13.983 MHz & 14.044 MHz --- Load Modulation Side Bands
27.543 MHz & 27.604 MHz --- Load Modulation + Carrier
423kHz & 484 kHz ---------- Load Modulation – Carrier (original transponder modulation frequencies)

Components C32 and R103 filter out the higher frequency components thus reducing their amplitude without effecting the intelligence frequencies of 423kHZ and 484kHz. Capacitor C33 blocks any DC component while R104 adds bias to the input of the RFID ASIC (U14-20). The ASIC will further filter and decode the frequencies based upon the selected Air to Air protocol.

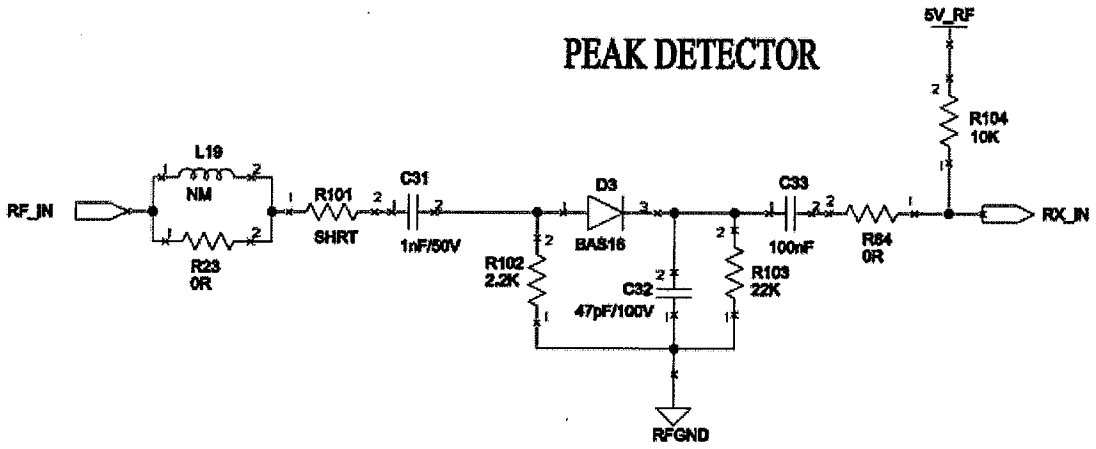

Figure 7

2.5 Antenna and Setup Port Communication Module:

Referring to Figure 8, signals ANT_SETUP_RX and ANT_SETUP_TX originate from UART 2 of microcontroller U1 pins 6 and 7. These two communication signals are shared between two external ports SETUP and Antenna. Depending on the state of signal MUX_A these signals will either be directed to one of the aforementioned ports by U8(Mux/Demux IC). When MUX_A is low communication will travel between the micro and the SETUP port. The SETUP port is an RS232 type connection which requires U10 to convert the TTL level signals from the MUX to an RS232 level. When signal MUX_A is high communication will be between the micro and the ANTENNA port. U9 is a RS485 transceiver that converts the TTL levels to 485 half duplex which is the ANTENNA ports communication format.

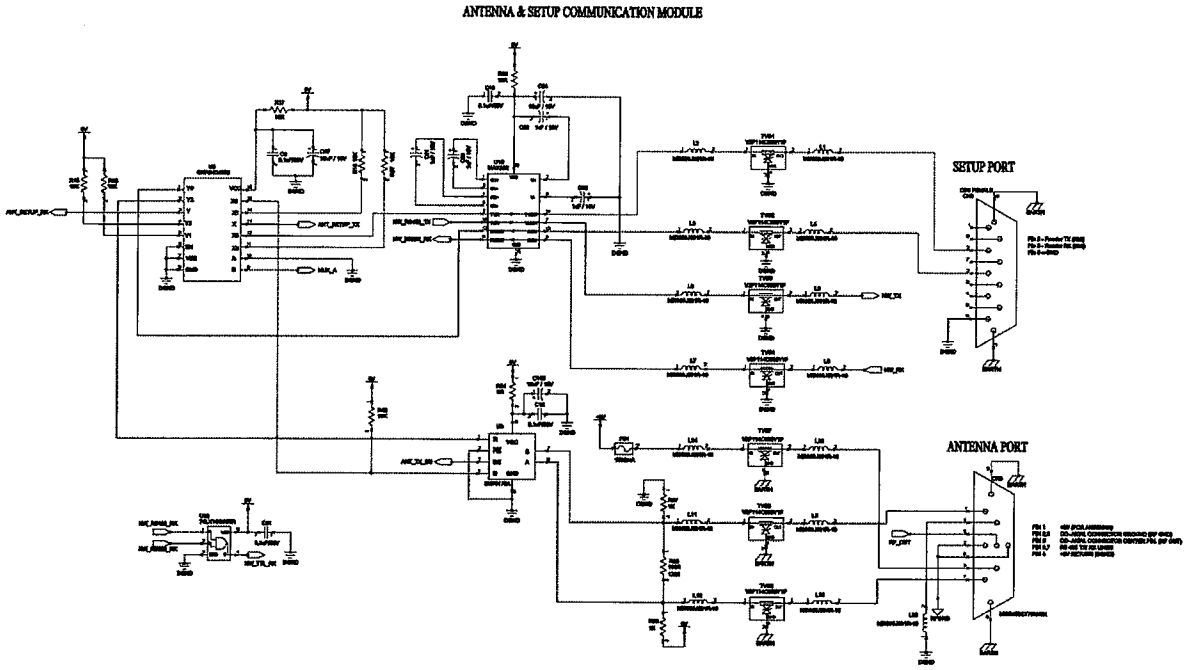

Figure 8

2.6 RS422/RS232 Host Communication Module:

The Host Serial Port in Figure 9 has both RS232 and RS422 communication capabilities. Signals NW_RS422_TX and NW_RS422_RX originate from internal UART 1 of micro controller U1 pins 37 and 38. Looking at the RS422 communication link these two signals first connect to Opto-Couplers U22 and U23 which aid in the galvanic isolation of RS422 communication link. The Opto's inputs and outputs are respectively connected to RS422 driver U19 and RS422 receiver U20. Notice that the power supply for both U19 and u20 is an isolated 5VDC which keeps the galvanic isolation integrity intact. Resistors R46, 47, 48, 52, 53, and 54 provide terminating and pulling resistors for the RS422 link.

Looking at the RS232 link, signals NW_RS422_TX and NW_RS422_RX are also connected to RS232 transceiver IC U10 pins 9 and 10 in Figure 7. U10 provides the RS232 level conversion for TTL signals. These level converter signals are NW_TX and NW_RX.

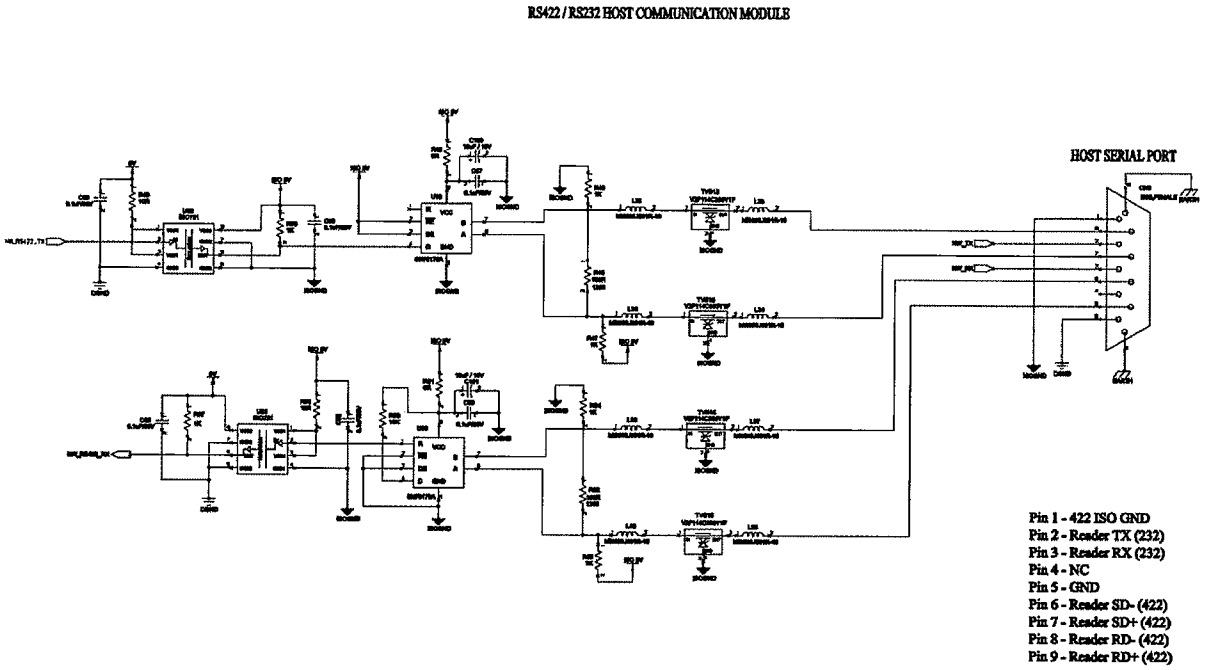

Figure 9

2.7 Ethernet Module:

Figure 10 shows that the Ethernet Module is mainly composed of three parts, U11, U6 and XTAL3. U11 is a stand alone Ethernet controller with SPI interface to communicate with microcontroller U1. Pins 27 and 28 of U11 control the LAN Tx/Rx and LINK LEDs. It has up to 10 Mb/s data rate with Full/Half Duplex support. Crystal XTAL3 provides the controller with a 25 MHz clock signal. U6 is a pulse transformer capable of supporting 10/100 Base connections.

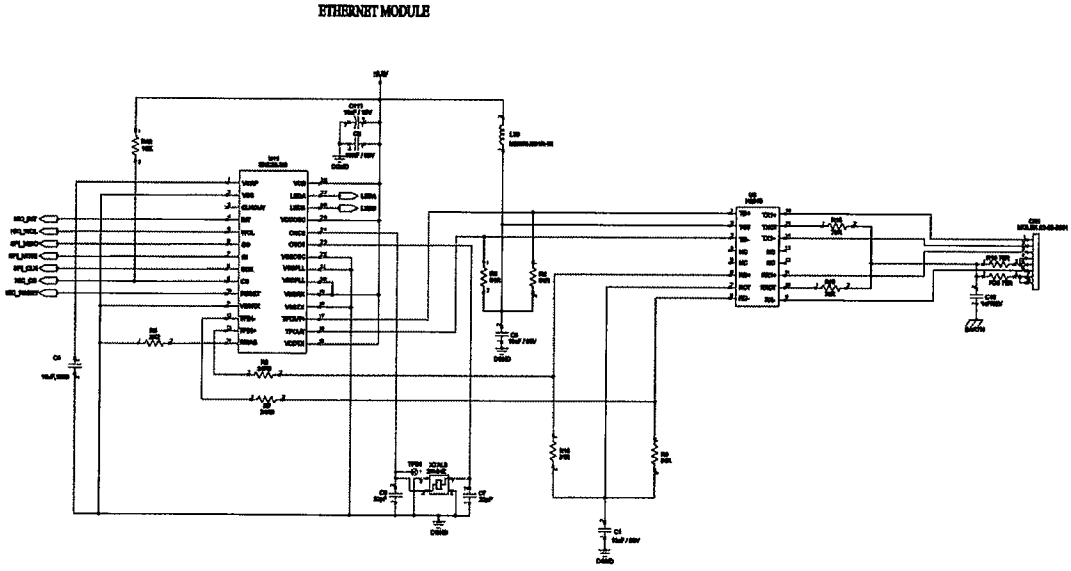

Figure 10

2.8 Micro Controller Module:

Referring to Figure 11 U1 is an 8 bit microcontroller with 128K of Flask and 1024 EEPROM memory. It uses a 40 MHz crystal (XTAL2) for development of internal clocks. Connector CN2 is used to program the microcontroller with its bootloader program and to configure internal registers. The Auto Tune Push Button Switch causes the microcontroller to send an Auto-Tune command the antenna out the thru the Antenna Port (CN3), the Auto-Tune process takes a little over 1 second to be completed, when finished the microcontroller will blink the Status LED(LED3) 3 times.

There are a total of six LEDS that provide visual diagnostics to the user. Two of them LED5 and LED 6 are under control of the Ethernet Controller IC (U11) and provide status related to the Ethernet connection. Led 4 is a power indicator. LED2 indicates data activity on the Host Serial Port (CN6). LED 1(Tag Read) flashes when there has been a valid message received from a transponder. LED3 (Status) is a bi-color type and is used to provide information on Reader's current status, for instance if the status LED is solid green the reader is functioning correctly or if the LED is Blinking Red two times every second there is no communication to the antenna.

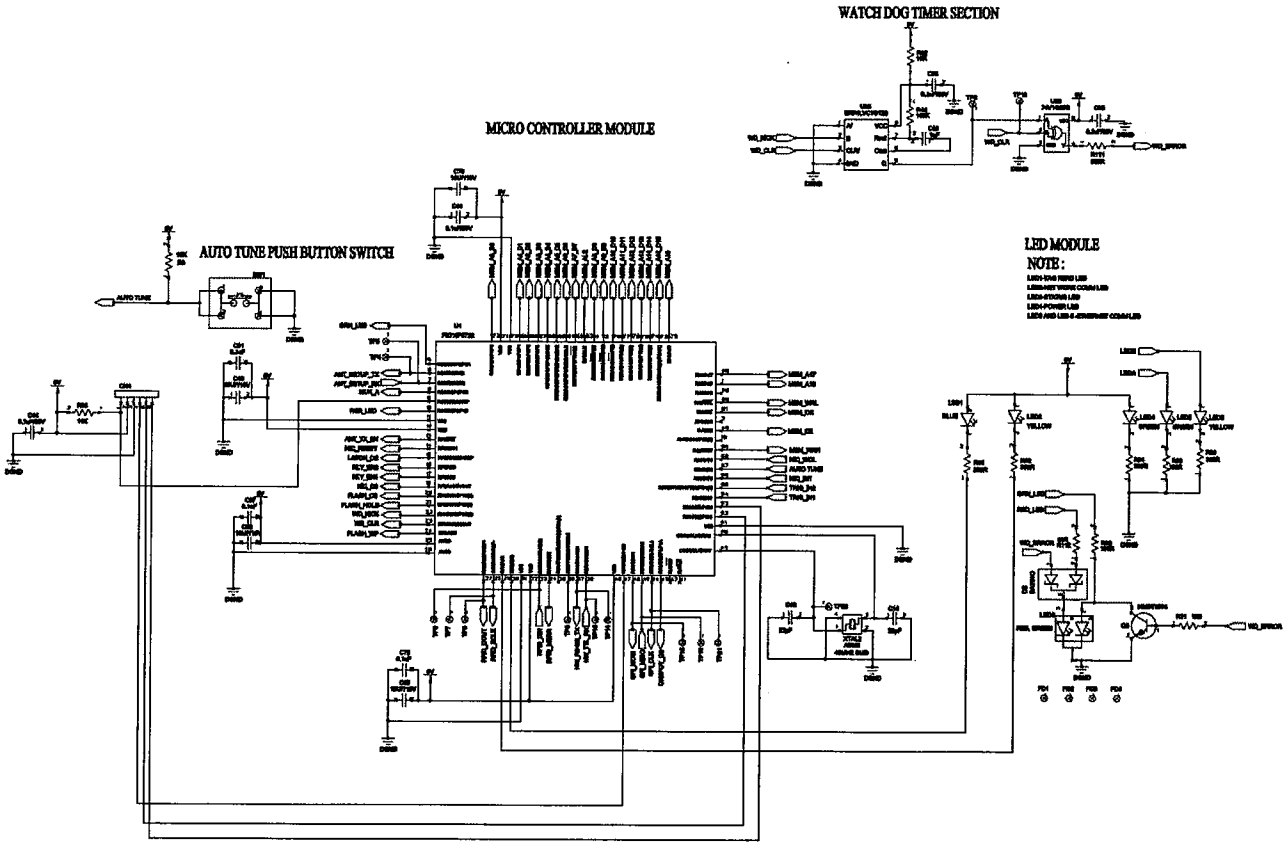

Figure 11

2.9 Memory Module:

Figure 12 shows the memory section of the reader. U2 and U24 are 512K x 8 CMOS SRAM ICs, yielding 1M x 8 of external RAM. This external RAM is necessary as the microcontroller internal RAM was not large enough to handle the application. U7 is a 2Meg x 8 Serial Flash IC and is used to hold the reader application as well as the Auto-Tune antenna application. During the boot sequence of the reader it checks the antenna firmware to ensure that it matches it internal version, if there is a mismatch the reader will automatically update the antenna firmware.

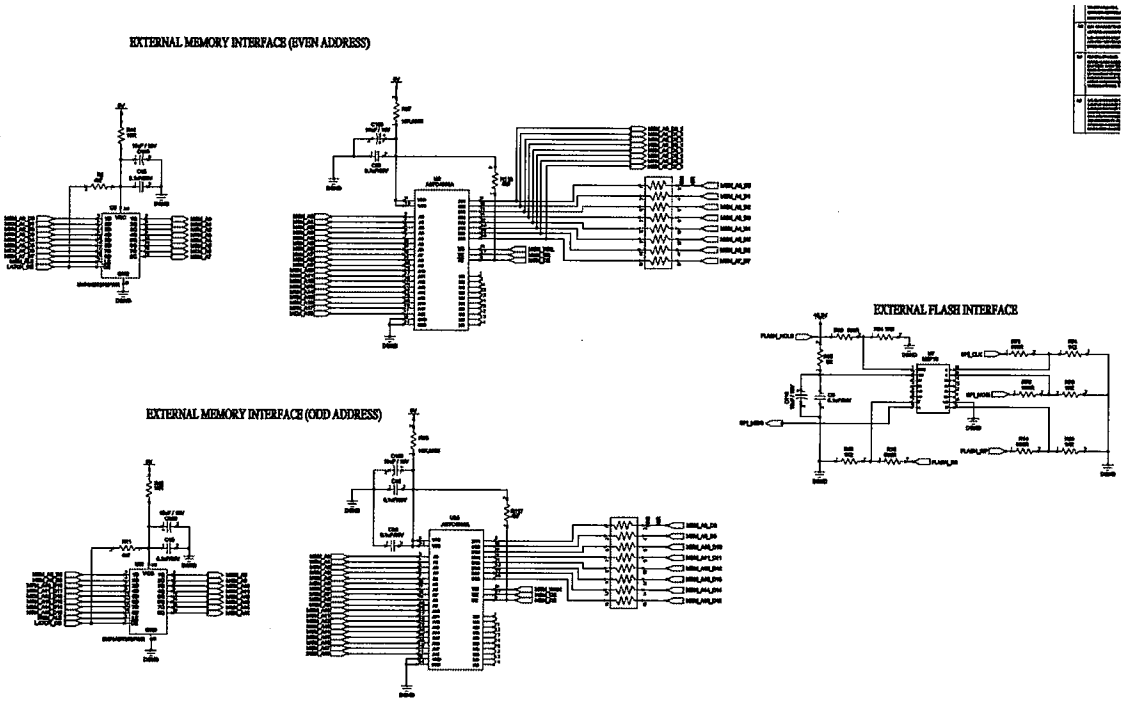

Figure 12

3.0 Auto-Tune Antenna

3.1 Matching and Frequency Tuning Circuitry:

Pictured below in Figure 13 is a detailed view of the match and frequency adjustment section of the auto tune antenna. The capacitors connected to K3 are used for frequency adjustment and the ones connected to K4 are used for match adjustment. Relays K3 and K4 internally have 8 relays each which are controlled serially by the microprocessor which is not shown. Capacitors C5 and C3 represent the fixed value of frequency capacitance and C1 and C6 do the same for the match capacitance. This configuration is known as a tapped "C" transformer. The tapped "C" transformer allows connection between the reader's 50 ohm RF port and the antenna without lowering the antenna's "Q". Without this impedance transformation the reader low output impedance would decrease the antenna's "Q" which in turn reduces the circulating current in the antenna's loop which will results in a lower read range. Adequate match can be obtained over the tuning range of the antenna with the use K4 this reduces cost and tuning time.

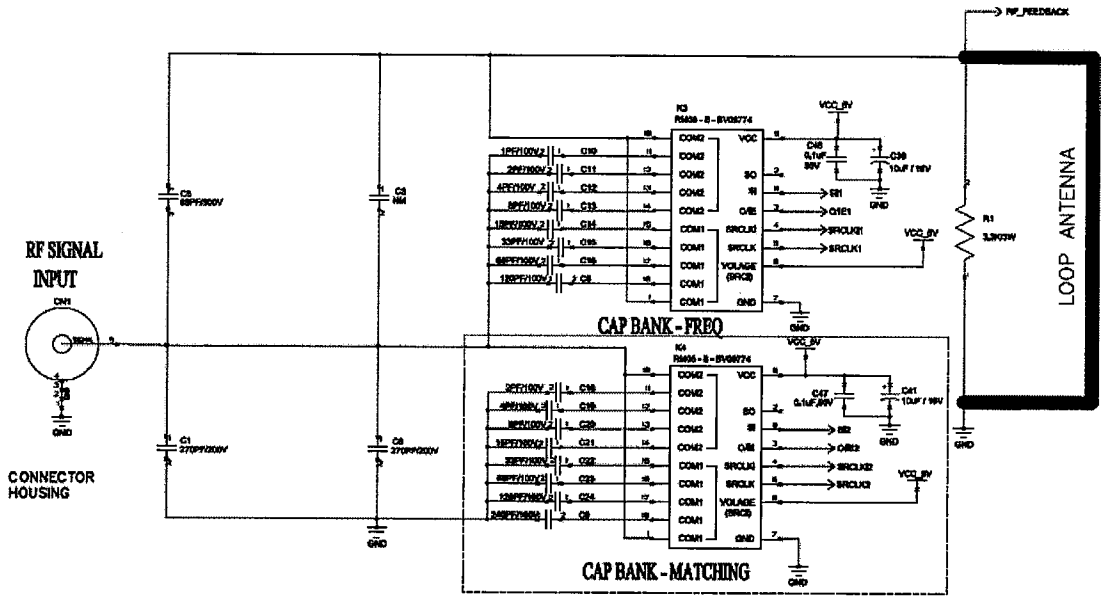

Figure 13

3.2 Envelope Detector:

To perform auto-tuning a sample of the antenna's RF energy needs to be taken and measured. Prior to measuring the energy it must be conditioned into a DC voltage that can be accurately measured. The envelope detector circuit shown in Figure 14 performs this task and is the preferred method as it yields the greatest dynamic range. A small capacitor (C27) is connected to the hot side of the antenna to sample the RF energy, this capacitor is very small typically less than 1 PF which prevents the peak detecting from loading antenna. Diode "D1" performs

a half wave rectification of the AC waveform. Capacitor C32 and R103 create an RC time constant that provides smoothing of the half wave rectified signal. Careful selection of RC time is required, making it too large will require too many cycles of the RF signal to fully charge C32 which increases the auto-tune time. Making it too short will lead to a choppy signal that will introduce measurement errors. Resistors R20 and R105 reduced the level of the signal present on R103 to magnitude that is within the range of the microcontroller's Analog to Digital Converter. Capacitor C26 provides additional filter. Note that there is a FET (not shown) connected to the point labeled ADC that discharges capacitor C26 before each new auto tune combination is tried.

ENVELOPE DETECTOR CIRCUIT.

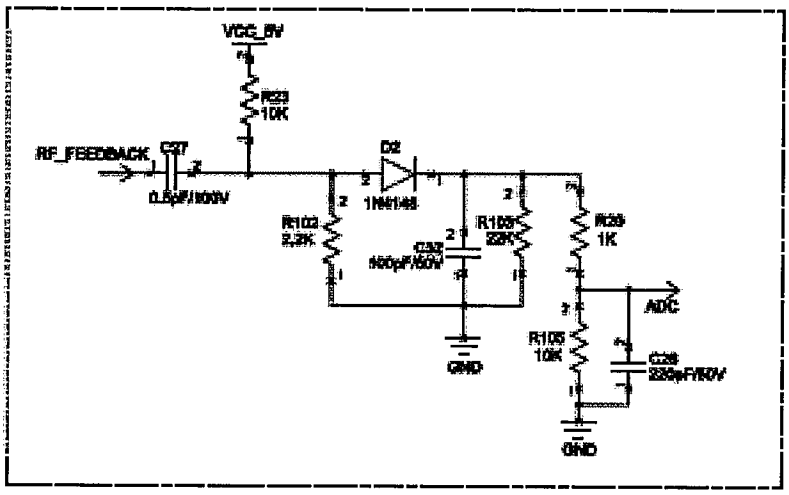

Figure 14

3.3 Microcontroller Section:

Referring to Figure 15 U1 is an 8 bit microcontroller with 16K of Flash memory and 256 bytes of EEPROM. It develops its timing from an internal oscillator. U1 has two main purposes the first is to implement auto-tuning when it receives a command from the reader. The second is to store reader parameters. In both cases the antenna always waits for a command from the reader before performing any function. In normal operation the microcontroller is in sleep mode with its internal oscillator shutdown. The turning off of the microcontroller's internal oscillator increases the read range of the antenna. The microcontroller wakes up when it senses activity on pin 18. This pin is connected to the signal "INT_SLEEP" which is also the receive data pin of U2 (RS485 transceiver IC). Whenever the reader sends data to the antenna it wakes up the microcontroller which then processes the command.

When the microcontroller receives an auto-tune command from the reader it will implement a unique auto-tuning algorithm enabling it to find the optimum setting

of K3, auto-tune time is approximately 1 second. After completing the auto-tune the antenna will send back to the reader the setting of K3 that resulted in the greatest voltage read by the internal ADC via the peak detector circuitry, and the corresponding ADC value for this voltage. The internal ADC is 10 bit and uses an internal 5 VDC reference this yields 4.88 millivolts per AD step.

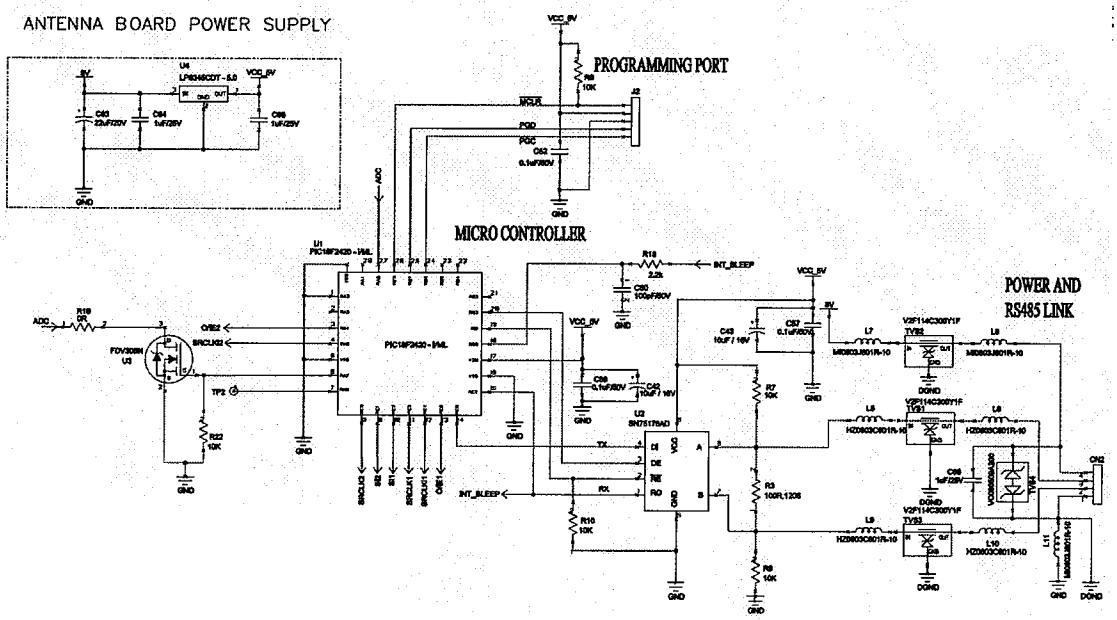

Figure 15

4.0 Revision History:

Revision	Date	Initials	Comments
1	2/20/08	RRH	Initial Release