INFORMAL REVISION HISTORY:

* 071102
  -01 PCB Fabbed

* 080116 -02 Version
  - Added capacitance on V3.3 to address card engine startup issue
  - Change CF connector back to "311"

* 080317 -03 Version
  - Change D5,D6,D10,D11 from RCLAMP0504S to RCLAMP0504P
    per ESP SZ request because "P" package has better availability there.

* 080512 -04 Version (5/5 Steve Mfgability Inputs + LPD pwr sequence inputs)
  - Add PXA270 SYS_EN controlled high side switch on (U11 on sht 10) V3.3
    per LogicPD inputs to prevent PXA270 ext peripherals from being powered
    before PXA270 I/O. Net remained V3.3 but is now switched
  - Create new V3.3_UNSW for output of POE module and V3.3_up_Batt
    of the PXA270 (per Marvell DS & LPD inputs)
  - Add TP's on PXA270 UARTA (IRDA) lines and pulldown and TP on IRDA
    shutdown so UARTA console can be used in prdctn w/IRDA xcvr installed
  - Change P2 chipcon pgming connector to same non-std 1x5 used on watch & hub
  - Remove USB host circuitry (wasn't populated before anyway)
  - Remove RFID module and associated power supply (per Chris 5/13 e-mail)

  - Remove accelerometer (was only included initially to allow test since this
    board was done before the Hub.
  - Change Y1 (32kHz Xtal) from FC-145 to FC-135 (Per Steve request)
  - Add testpoints on all LCD interface signals (per Steve request)

080520 -04 Version (Steve made chgs, chet added comments)
  - Add twelve testpoints to keypad (per steve 5/19 e-mail)
  - Add two testpoints to spare lines of RJ45 (per steve 5/19 e-mail)

080523 - 04 Changes (Mostly based on LogicPD schematic review)
  - Change PXA270 VCORE voltage from 1.5V to 1.27V
  - Remove C1, C13 VCORE caps - not necessary
  - Float card engine A67 (USB1_VBUS - old net was erroneously named overcrnt_f)
  - Strap CF A0 low since CE is driven for whole word only (Per LPD suggestion)
  - Drive CF reset w/inverted uP_RST_OUT instead of MSTR_RST_F (per LPD)
  - Add TP's on PXA270 JTAG lines (no-cost CYA for long term production needs)
  - Move LCD PS ctrl from PSOC to PXA270 LCD_VDDEN & add pull down
  - Change C8 (CF bulk cap) from 10uF to 22uF per LPD suggestion
  - Change VCORE DC/DC input from V3.3 (SYS_EN switched) to V3.3_UNSW
  - Remove PSOC drive of VCORE DC/DC enable - strapped always on
  - Moved PXA270_TO_2431_CYA_1 from MFP22 to MFP27 per LPD
    recommendation (MFP22 not PXA I/O)

0811XX - 05 Changes
  - Replace 300uF tant 3.3V bulk caps split between the inand out sides of the high
    side switch w/990uF alum electr. all on the input side. (see note sht 10 for details)
  - Change J16 RJ45 PN(s) and footprint so it can be populated with either a vertical
    (in SH) or right angle (in KBP) connector.
  - Add external LNA board power and TX/RX connector per Steve's inputs.

-05 TODO

TK0169-74-05 ESP SH/KPBP SCHEMATIC

(081114A)

Sht02_CardEng_DIMM_Socket
Sht02_CardEng_DIMM_Socket.Sch

Sht03_CardEng_AB_Hdrs
Sht03_CardEng_AB_Hdrs.Sch

Sht04_LCD_Interface
Sht04_LCD_Interface.Sch

Sht05_CF_Socket_Etc
Sht05_CF_Socket_Etc.Sch

Sht06_CC2431_ESPNET_Engine
Sht06_CC2431_ESPNET_Engine.Sch

Sht07_SysMgmt_uC_and_pwr
Sht07_SysMgmt_uC_and_pwr

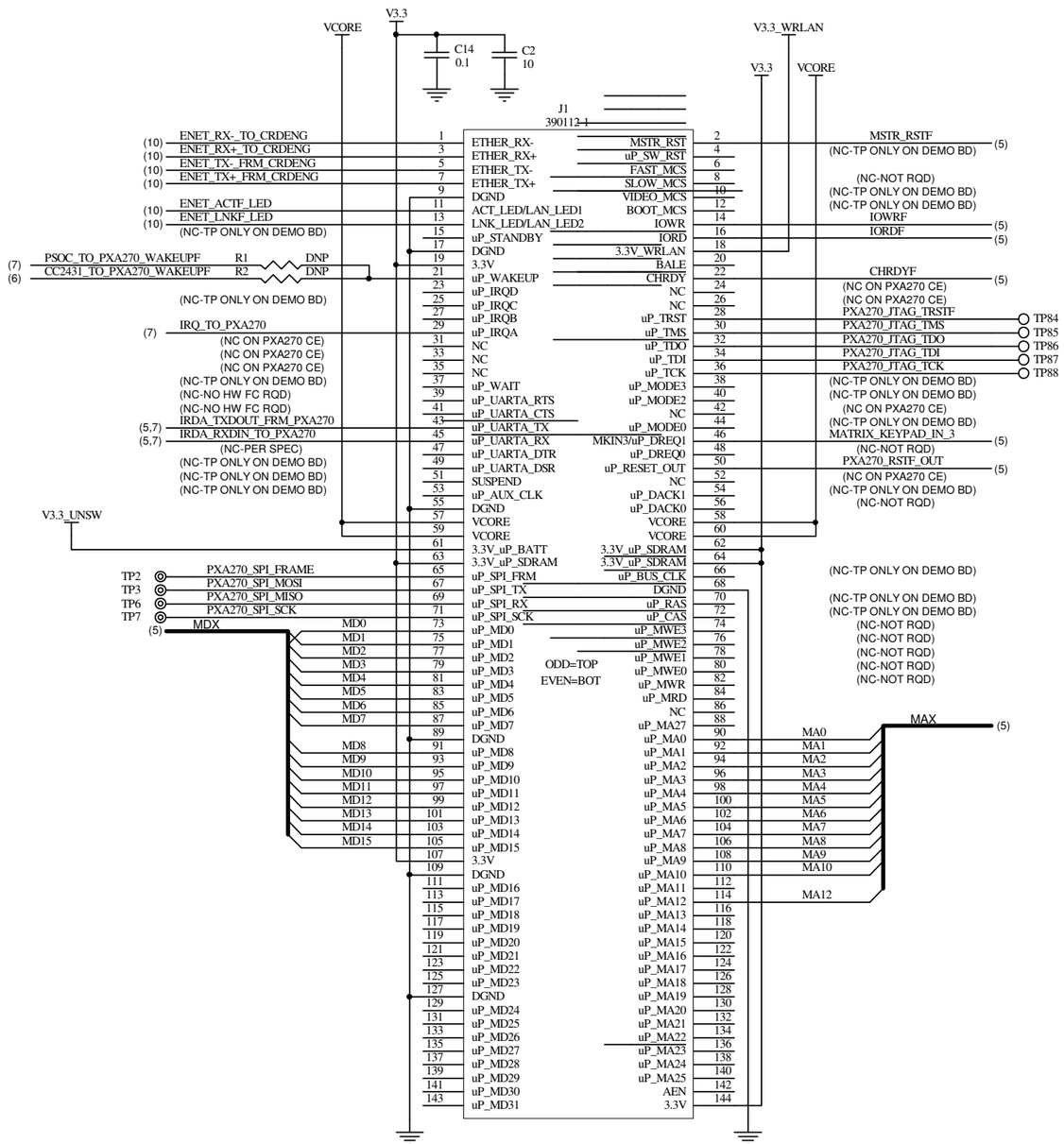
Sht08_USB_Etc
Sht08_USB_Etc

Sht09_RFID_Accelerometer
Sht09_RFID_Accelerometer

Sht10_POE
Sht10_POE

1

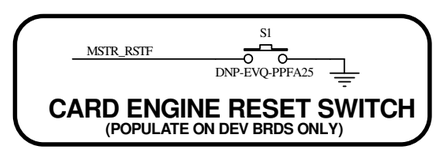
Title	ESP SUPERHUB		
Size: B	Number: TK0169-74-05		Revision: -
Date: 13-Nov-2008		Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0169_SuperHub\SCH_PCB\TK0169_-05_ESP_SuperHub.ddb			



NOTE: CARD ENGINE MASTER RESET DOES NOT NEED TO BE DRIVEN. IT IS A THE OUTPUT OF A SUPERVISOR ON THE CARD ENGINE.

NOTE: FAST_MCSF AND SLOW_MCSF CHIP SELECT SIGNALS ARE NOT USED BY ANYTHING ON THE CARD ENGINE. THEY ARE FOR PERIPHERALS EXTERNAL TO THE ENGINE ONLY.

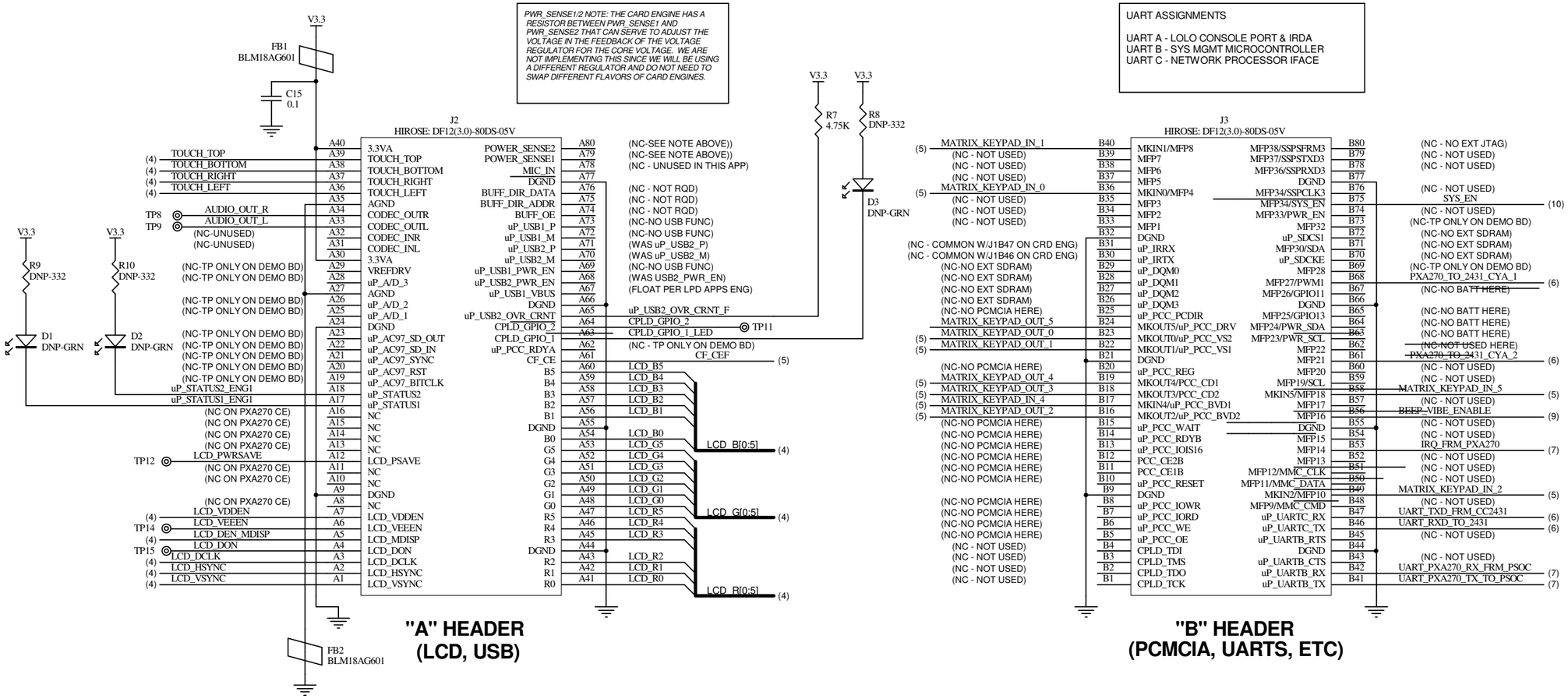
NOTE: uP_nTRST PXA270 JTAG RESET SIGNAL IS PULLED UP TO V3.3_UNSW ON THE CARD ENGINE AND IS ALSO DRIVEN ACTIVE TO RESET BY TWO DIFFERENT POWER MONITORS ON CARD ENGINE.



CARD ENGINE RESET SWITCH
(POPULATE ON DEV BRDS ONLY)

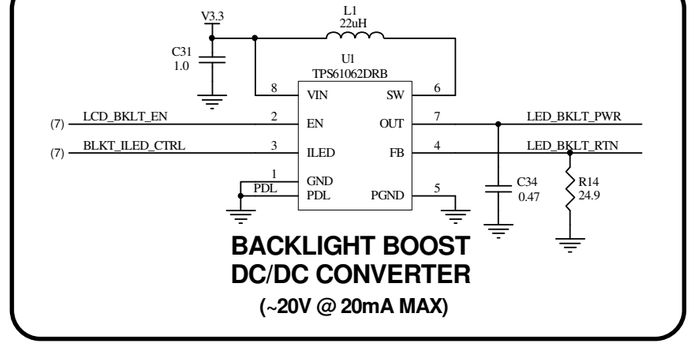
PXA270 CARD ENGINE "DIMM" CONNECTOR

Title: ESP SUPERHUB		
Size: B	Number: TK0169-74-05	Revision: -
Date: 13-Nov-2008	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0169_SuperHub\DSCH_PCB\TK0169_-05_ESP_SuperHub.ddb		



PXA270 CARD ENGINE "A" AND "B" HEADERS

Title	ESP SUPERHUB	
Size: B	Number: TK0169-74-05	Revision: -
Date: 13-Nov-2008	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0169_SuperHub\DSCH_PCB\TK0169_-05_ESP_SuperHub.ddb		



BACKLIGHT BOOST DC/DC CONVERTER

(~20V @ 20mA MAX)

LCD PWR RQMTS

VCC 3.3 @ @ 1.3 - 5mA
AVDD 5.0 @ 2-5mA
VGH 15.0 @ 100-300uA
VGL -10 @ 100-300uA
VLED ~20V @ 20mA
VCOM TBD AC @ ? current

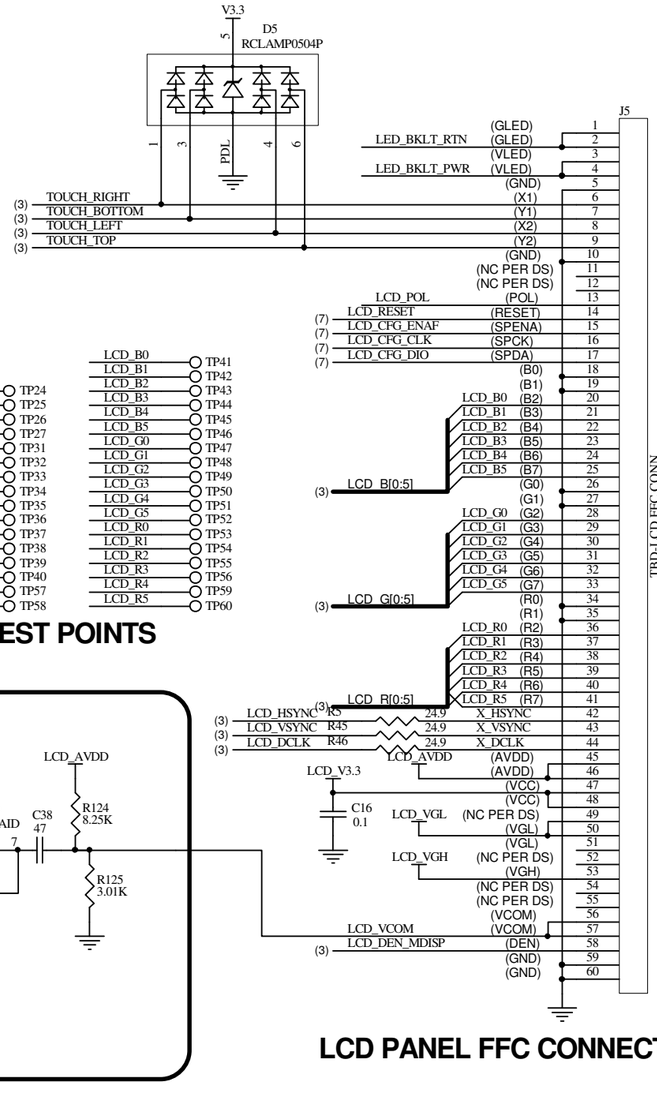
INNOLUX PT035 TOUCH INFO

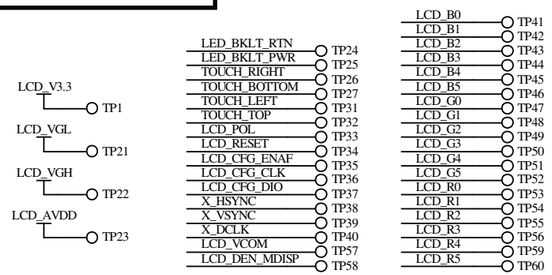
X1 - RIGHT - PIN 6
Y1 - BOTTOM - PIN 7
X2 - LEFT - PIN 8
Y2 - TOP - PIN 9

Display is set up for 6 O'Clock viewing. It is TBD whether it will need to be rotated 180 in the housing or not - depends on still fluid ID and use model.

TOUCH SCREEN INPUT ESD PROTECTION

(NOTE: .01uF CAPS ON THESE LINES ON CARD ENGINE TOO)

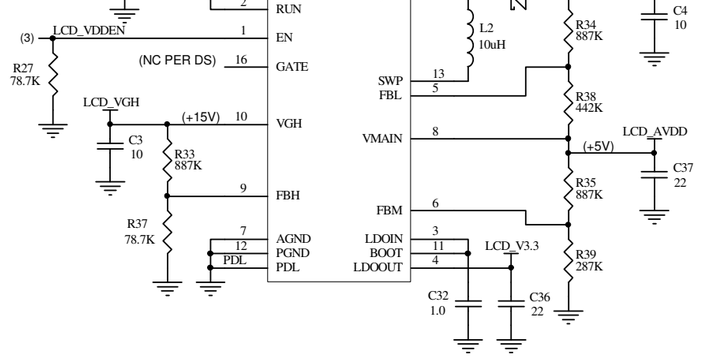




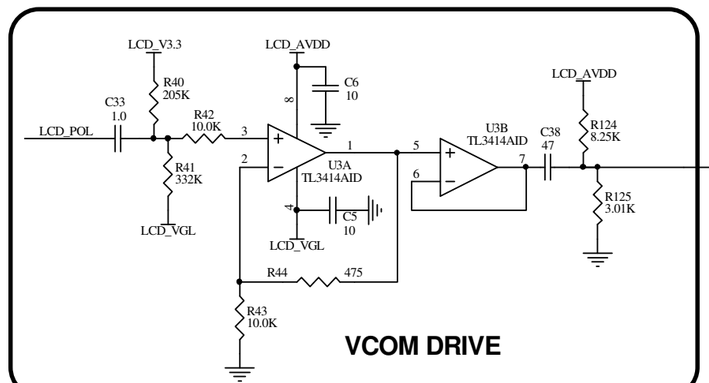
LCD INTERFACE TEST POINTS

TPS65120 VOLTAGE SETTINGS

VMAIN=AVDD=1.213*(887K+287K)/287K=5.0V
VGH=1.213*(887K+78.7K)/78.7K= 14.9V
VGL=-VMAIN*(RA/RB)=5*(887/442)=-10.0V
VLDO=3.3V (Fixed)



LCD +3.3, +5.0, +15.0 & -10.0V POWER SUPPLY



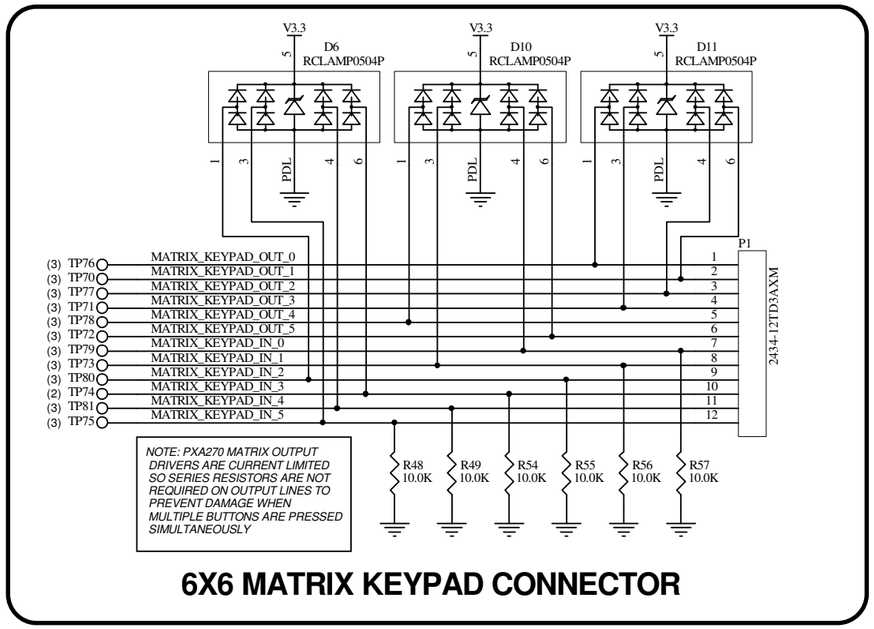
VCOM DRIVE

LCD PANEL FFC CONNECTOR

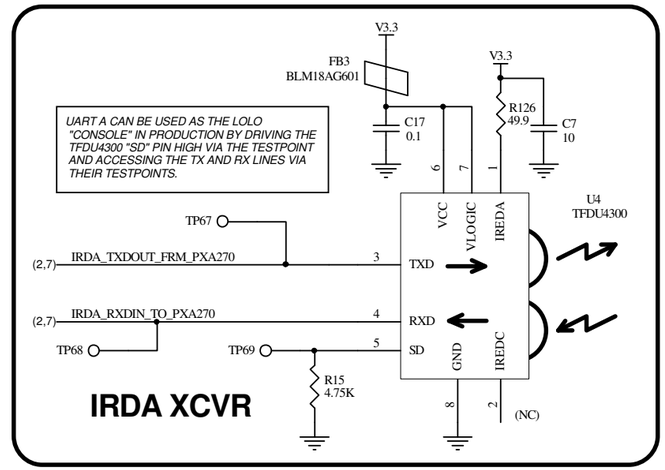
4

LCD POWER & INTERFACE

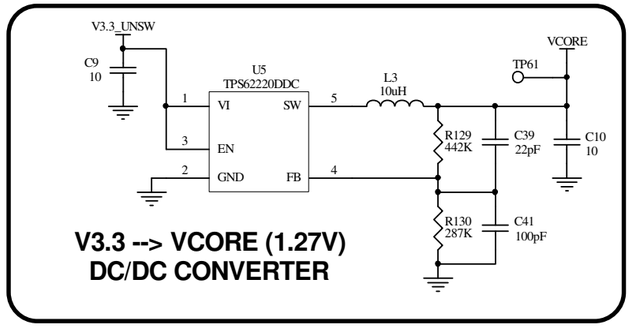
Title: ESP SUPERHUB		
Size: B	Number: TK0169-74-05	Revision: -
Date: 13-Nov-2008	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0169_SuperHub\SCH_PCB\TK0169_-05_ESP_SuperHub.ddb	DRAWN BY:	



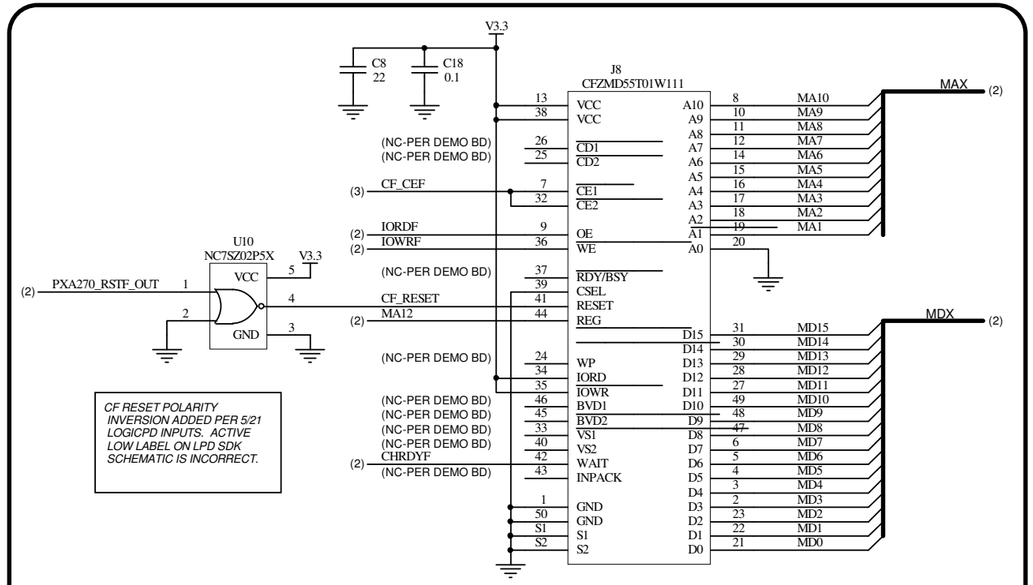
6X6 MATRIX KEYPAD CONNECTOR



IRDA XCVR



V3.3 --> VCORE (1.27V) DC/DC CONVERTER



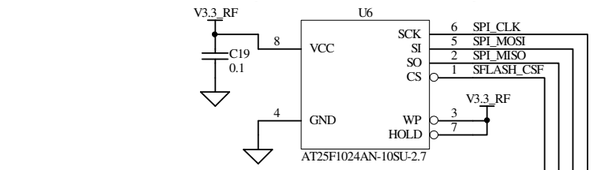
COMPACT FLASH SOCKET

5

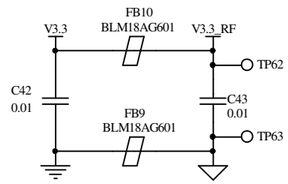
COMPACT FLASH, IRDA & KEYPAD INTERFACE

Title: ESP SUPERHUB		
Size: B	Number: TK0169-74-05	Revision: -
Date: 13-Nov-2008	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0169_SuperHub\PCB\TK0169_-05_ESP_SuperHub.ddb	Drawn By:	

128KB SERIAL EEPROM FOR OTA UPDATE (TBD IF RQD OR NOT)

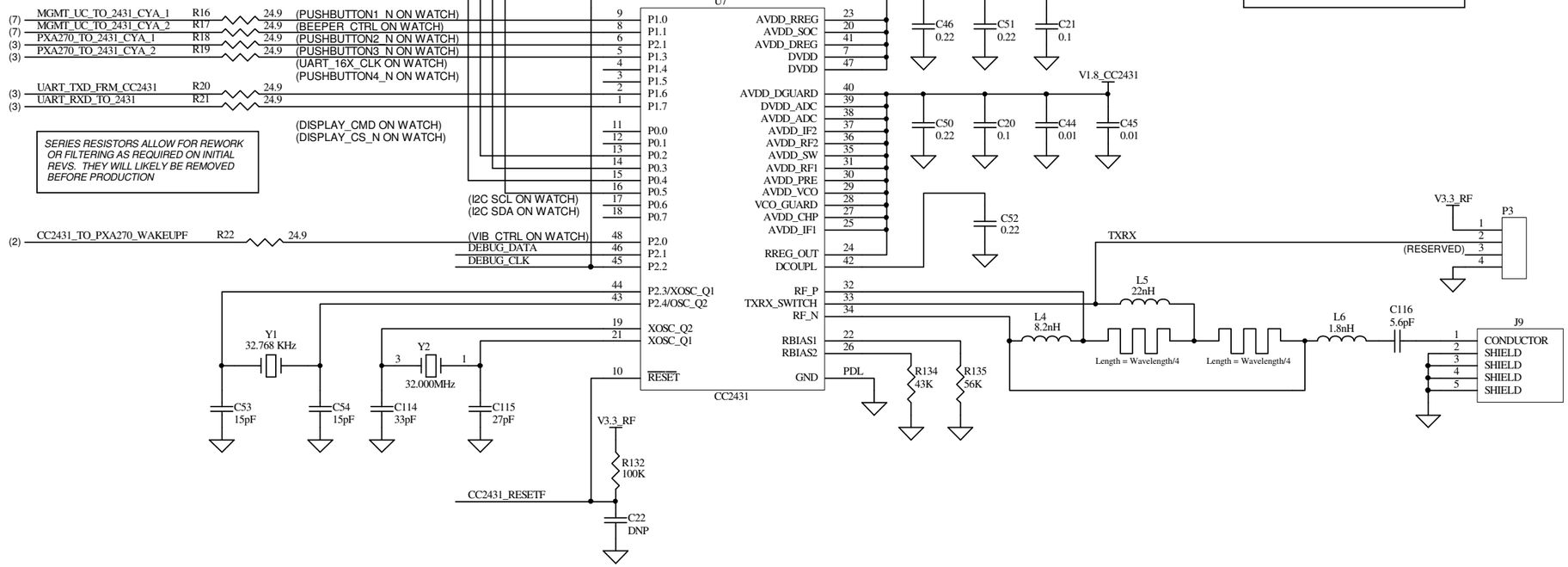


POWER FILTERING

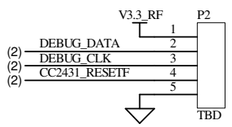


POWER FILTERING CAN BE REMOVED IF TESTING SHOWS IT IS NOT NECESSARY. FOOTPRINTS CAN ALSO BE USED FOR OTHER COMPONENTS IF FILTERING IS REQUIRED BUT THE CURRENT COMPONENTS ARE NOT OPTIMAL

SERIES RESISTORS ALLOW FOR REWORK OR FILTERING AS REQUIRED ON INITIAL REVS. THEY WILL LIKELY BE REMOVED BEFORE PRODUCTION



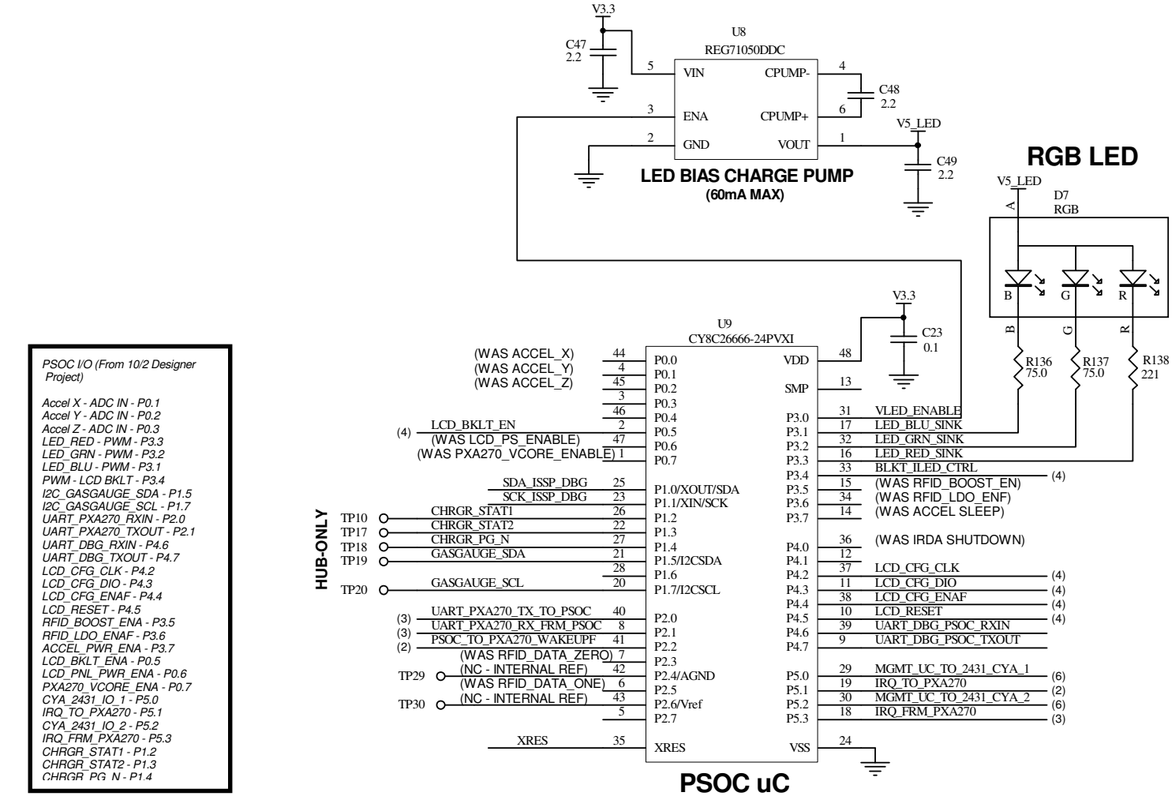
CC2431 PGM & DBG CONNECTOR (DNP IN PRODUCTION)



CC2431 NETWORK ENGINE

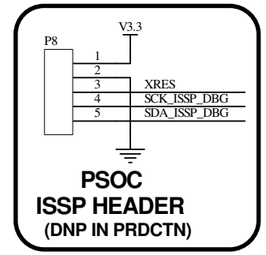
6

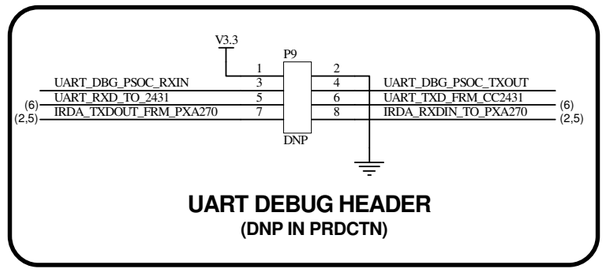
Title: ESP SUPERHUB		
Size: B	Number: TK0169-74-05	Revision: -
Date: 13-Nov-2008	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0169_SuperHub\DSCH\TK0169_-05_ESP_SuperHub.ddb	Drawn By: PCB\TK0169_-05_ESP_SuperHub.ddb	



PSOC I/O (From 10/2 Designer Project)

Accel X - ADC IN - P0.1
Accel Y - ADC IN - P0.2
Accel Z - ADC IN - P0.3
LED_RED - PWM - P3.3
LED_GRN - PWM - P3.2
LED_BLU - PWM - P3.1
PWM - LCD BKLT - P3.4
I2C_GASGAUGE_SDA - P1.5
I2C_GASGAUGE_SCL - P1.7
UART_PXA270_RXIN - P2.0
UART_PXA270_TXOUT - P2.1
UART_DBG_RXIN - P4.6
UART_DBG_TXOUT - P4.7
LCD_CFG_CLK - P4.2
LCD_CFG_DIO - P4.3
LCD_CFG_ENAF - P4.4
LCD_RESET - P4.5
RFID_BOOST_ENA - P3.5
RFID_LDO_ENAF - P3.6
ACCEL_PWR_ENA - P3.7
LCD_BKLT_ENA - P0.5
LCD_PNL_PWR_ENA - P0.6
PXA270_VCORE_ENA - P0.7
CYA_2431_IO_1 - P5.0
IRQ_TO_PXA270 - P5.1
CYA_2431_IO_2 - P5.2
IRQ_FRM_PXA270 - P5.3
CHRGR_STAT1 - P1.2
CHRGR_STAT2 - P1.3
CHRGR_PG_N - P1.4





CYPRESS PSOC NOTES

27443 - TSSOP28 - 16KB, 8 DIG, $2.88 DK 1K ($2.40 Avnet)
27543 - TQFQ44 - 16KB, 8 DIG, $3.43 DK 1K
27643LF - QFN48 - 16KB, 8 DIG, $3.57 DK 2K
27643PV - SSOP-48 - 16KB, 8 DIG, $3.10 DK 1K

29466 - TSSOP28 - 32KB, 16 DIG, DK $3.95 1K ($3.30 Avnet)
29566 - TQFP44 - 32KB, 16 DIG, DK $4.38 1K
29666LF - QFN48 - 32KB, 16 DIG, DK $4.63 1K
29666PV - SSOP-48 - 32KB, 16 DIG, DK $4.13 1K

"SYSTEM MANAGEMENT" MICROCONTROLLER (PSOC)

Title: ESP SUPERHUB		
Size: B	Number: TK0169-74-05	Revision: -
Date: 13-Nov-2008	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0169_SuperHub\SCH_PCB\TK0169_-05_ESP_SuperHub.ddb	Drawn By:	

USB HOST WAS NEVER POPULATED AND WAS REMOVED 5/13/08

FORMERLY USB HOST INTERFACE

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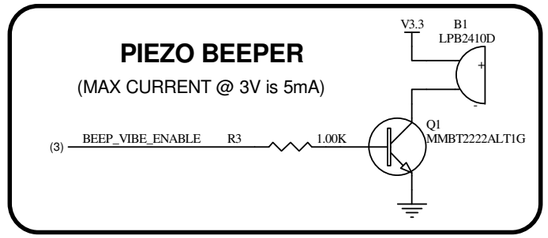
Title: ESP SUPERHUB		
Size: B	Number: TK0169-74-05	Revision: -
Date: 13-Nov-2008	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0169_SuperHub\PCB\TK0169_-05_ESP_SuperHub.ddb	DRAWN BY:	

RFID REMOVED PER 5/13/08 CHRIS E-MAIL



ACCELEROMETER REMOVED 5/13
(ONLY INCLUDED FOR PRE-HUB TEST INITIALLY)

9

RFID MODULE, ACCELEROMETER, ETC.

Title	ESP SUPERHUB	
Size: B	Number: TK0169-74-05	Revision: -
Date: 13-Nov-2008	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0169_SuperHub\PCB\TK0169_-05_ESP_SuperHub.ddb	DRAWN BY:	

SIGNIFICANT PTB48540 POE MODULE SPECS:

* IEEE 802.3af Compliant
* 36-57V IN
* 1500V Input to Output Isolation
* 3.3V OUT
* 10W Output
* ~75% EFF (3-10W OUT)
* Short circuit & overtemp protection

CLASS RESISTOR DETAILS:

MODULE HAS INTERNAL 4.42K CLASSIFICATION RESISTOR WHICH MAKES IT A CLASS 0 DEVICE WITH NO EXTERNAL RESISTOR POPULATED

CLASS / VALUE / POWER RANGE
CLASS 0 / DNP / 0.4W to 13W
CLASS 1 / 1.21K / 0.4 to 3.8W
CLASS 2 / 619 / 3.8 to 6.5W
CLASS 3 / 392 / 6.5 to 13W

3.3V SWITCH NOTE

3.3V HIGH SIDE SWITCH ADDED 5/12/08 PER LOGICPD AND MARVELL DATASHEET GUIDANCE TO KEEP PXA270 EXTERNAL PERIPHERALS FROM BEING POWERED PRIOR TO THE PXA270 CORE AND I/O BEING UP AND "SANE" AND TO PREVENT THE PERIPHERALS FROM BACK POWERING THE PXA270 3.3V I/O AT STARTUP

V3.3
TP64
V3.3_UNSW
TP65
TP66

U28
PTB48540BAH

10 DATA LINE A
9 DATA LINE B
7 SPARE LINE B
8 SPARE LINE A
(NC - INT 24.9K) 5 DETECT A
(NC - INT 24.9K) 6 DETECT B
R148 619
12 CLASS A
11 CLASS B
(NC - INT PU) 13 OUTPUT INHIBIT
(NC) 4 INPUT REF
VOUT+ 3
VOUT ADJ 2
VOUT- 1

V3.3_UNSW
R4 DNP
R6 DNP
C1 330
C11 330
C12 330

U11
FPF1008
2 VIN
3 VIN
VOUT 4
VOUT 5
(3) SYS_EN 1
ON/OFF
GND 6
V3.3

3.3V POWER SWITCH

3.3V BULK CAPACITANCE NOTE

PER THE LOGIC PXA270 CARD ENGINE HARDWARE MANUAL A MINIMUM OF 300uF OF BULK CAPACITANCE IS REQUIRED ON THE 3.3V RAIL FOR THE CARD ENGINE. THIS IS DUE TO A LARGE CURRENT SPIKE THAT THE CARD ENGINE REQUIRES SHORTLY AFTER POWER IS APPLIED. WITHOUT THIS CAPACITANCE, THE 3.3V SUPPLY WILL DROOP WHICH CAUSES THE PROCESSOR TO RESET AND THEN OSCILLATE THROUGH THE SAME CYCLE FOREVER. THE -04 VERSION HAD THE BULK CAPACITANCE ON THE OUTPUT SIDE OF THE SYS_EN CONTROLLED HIGH SIDE SWITCH. THAT ACTUALLY MADE THE OSCILLATION WORSE SO ALL BULK CAPACITANCE WAS MOVED TO THE INPUT SIDE OF THE SWITCH. THE MAXIMUM RECOMMENDED OUTPUT CAPACITANCE FOR THE PTB48540 POE MODULE IS 1000uF.

V3.3
TP16
R13 DNP-332
D18 DNP-GRN
TP28
TP5

3.3V PWR LED

POE PD CTRLR MODULE W/ ISOL DC/DC CNVRTR

V3.3_WRLAN
C30 0.1
R32 0R0
R127 49.9
R128 49.9
R23 24.9
R24 24.9

TP82
TP83

T1
PULSE_H2019

16	TX+	TD+	1	ENET_TX+_FRM_CRDENG	(2)
15	TXCT	TCT	2		
14	TX-	TD-	3	ENET_TX-_FRM_CRDENG	(2)
11	RX+	RD+	6 (R25 24.9)	ENET_RX+_TO_CRDENG	(2)
10	RXCT	RCT	7 (NC)		
9	RX-	RD-	8 (R26 24.9)	ENET_RX-_TO_CRDENG	(2)

J16
A00-108-2X2-450

1 ENET_TX+
2 ENET_TX-
3 ENET_RX+
4 ENET_SPARE_PAIR_1
5 ENET_RX-
6
7 ENET_SPARE_PAIR_2
8

C120 .022
C121 .022
C122 .022
C123 .022
R149 75.0
R150 75.0
R151 75.0
R152 75.0
C124 1000pF (2000V)

BST

POE COMPATIBLE ENET ISOLATION XFMR

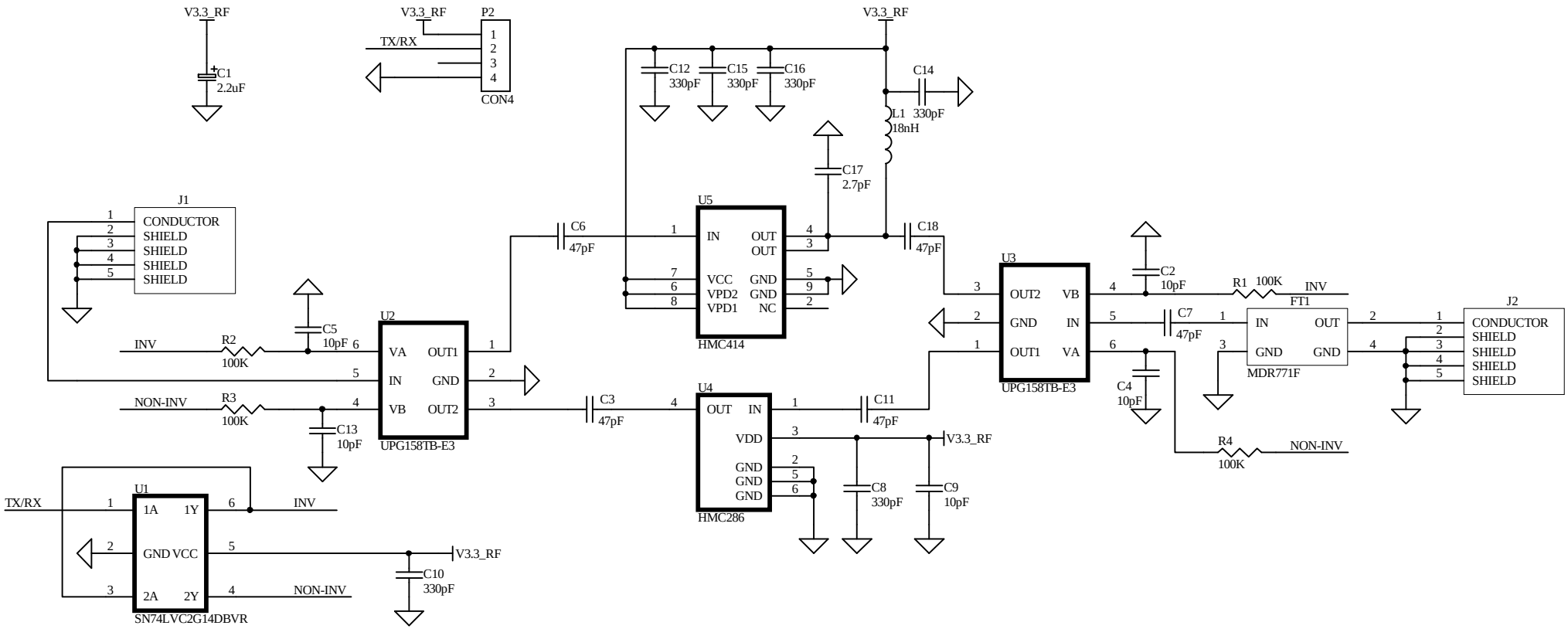
V3.3
V3.3
R11 DNP-332
R12 DNP-332
D9 DNP-GRN
D17 DNP-GRN
(2) ENET_LNKF_LED
(2) ENET_ACTF_LED

ENET STATUS LEDS (DNP IN PRDCTN?)

10

10/100BT & PWR OVER ENET MODULE

Title	ESP SUPERHUB		
Size: B	Number: TK0169-74-04		Revision: -
Date: 13-Nov-2008	Sheet X of Y		
File: C:\wcn\Turnkey\jobs\ESP_TK0169_SuperHub\SCH_PCB\TK0169_-05_ESP_SuperHub.ddb			


V3.3_RF
C1
2.2uF
V3.3_RF
P2
TX/RX
1
2
3
4
CON4
V3.3_RF
C12
330pF
C15
330pF
C16
330pF
C14
L1
18nH
330pF
C17
2.7pF
J1
CONDUCTOR
SHIELD
SHIELD
SHIELD
SHIELD
U5
IN
OUT
OUT
VCC
GND
VPD2
GND
VPD1
NC
HMC414
C6
47pF
C18
47pF
U3
OUT2
VB
GND
IN
OUT1
VA
UPG158TB-E3
C2
10pF
R1
100K
INV
FT1
C7
47pF
IN
OUT
GND
GND
MDR771F
J2
CONDUCTOR
SHIELD
SHIELD
SHIELD
SHIELD
C5
10pF
U2
INV
R2
100K
VA
OUT1
IN
GND
VB
OUT2
NON-INV
R3
100K
C13
10pF
UPG158TB-E3
C3
47pF
U4
OUT
IN
VDD
GND
GND
GND
HMC286
C11
47pF
V3.3_RF
C8
330pF
C9
10pF
C4
10pF
R4
100K
NON-INV
U1
TX/RX
1A
1Y
INV
GND
VCC
2A
2Y
NON-INV
SN74LVC2G14DBVR
V3.3_RF
C10
330pF