INFORMAL REVISION HISTORY:

* 071210 - STARTED -01 USING TK0169 SUPERHUB AS BASIS

* 080228 - Made -02 Version changes
- Added manual reset circuit (two buttons pressed while on charger)
- Change R68 from 619R to 330R to up power mux current limit
- Change C22 to DNP (cap on chipcon reset line)
- Ground U9 (PSOC) pin 43 so it can tell whether it is on a SHKPBP or a HUB
- Move C18 out from under CF Socket (layout change only)

* 080304
- Change C71 from 0.15uF to 0.22uF to make battery charge safety timer ~9 hrs nominal instead of ~6.5 hrs nominal to allow a dead battery to charge fully before the safety timer shuts the charger off.

* 080305
- Finish -02 PCB layout mods

* 080310 (-03 Version)
- -03 is PCB changes only to change board to 1.6mm thick instead of 1.0mm thick. In addition to changing the notes on the fab drawing, the controlled impedance trace geometries in the RF section also change per the John Holt inputs.

* 080519 -04 Changes
- Change Y1 footprint from FC-145 to FC-135 (Per Steve request)
- Add TP's on PXA270 UARTA (IRDA) lines (per Steve request)
- Add TP's on all LCD interface signals (per Stever request)
- Add SYS_EN control of V3.3 (per logicpd recommendation)
- Add 3.3V LDO for PXA270 3.3V_uP_batt (per logicpd recommendation)
- Change L9 to Sumida CDRH5D28RHPNP-4R7NC (per steve request)
- Remove unnecessary zero ohm R's on touch interface lines

* 080530 -04 Changes
- Change VPWRC OR'ing diodes from Schottky to standard
- Change PXA270 VCORE voltage from 1.5V to 1.27V (312 vs. 520 MHz)
- Remove C13 VCORE caps - not necessary per LPD
- Remove R7 to float card engine A67 (USB1_VBUS - old net was erroneously named overcrnt_f)
- Strap CF A0 low since CE is driven for whole word only (Per LPD suggestion)
- Drive CF reset w/inverted uP_RST_OUT instead of MSTR_RST_F (per LPD)
- Add TP's on PXA270 JTAG lines (no-cost CYA for long term production needs)
- Move LCD PS ctrl from PSOC to PXA270 LCD_VDDEN & add pull down
- Add 0.1uF and 22uF caps at CF connector (esp since on diff 3.3V rail now)
- Moved PXA270_TO_2431_CYA_1 from MFP22 to MFP27 per LPD recommendation (MFP22 not PXA I/O)
- Change audio amp feedback network values so they meet 5K min effective impedance requirement (also upped gain from 4.2 to 6.0 v/v)
- Add QTBD to SHUTDOWN line drive on audio amp so can guarantee high threhold met in shutdown (3.3V not enough to guarantee shutdown)
- Add caps at VTSB and SNS pins on UX charger IC per DS recommendation
- Segregate PXA270 and CF power from PSOC and Chipcon power to allow complete power off of PXA270 card engine. This involved moving PSOC and Chipcon to 3.3V LDO and adding a high side switch on the output of the 3.3V buck/boost switcher (see notes on sht 11 for explanation of each pwr rail)
- Added U23 SYS_EN controlled tristate buffer to all three PXA270 UART inputs and the wakeup_f input to prevent PXA from getting backpowered by input sigs when pwrd off

* 090111 -05 Changes
- Following changed reflect rework mods over Q4 '08 and early '09 that haven't been rolled into a schematic yet.
- Change card engine power from SYS_EN controlled V3.3_PXA_SW to V3.3_PXA_BATT leaving the CF card and the keypad pullups as the only thing powered by the SYS_EN controlled V3.3_PXA_SW. This was done because it was discovered that the card engine 3.3V is gated onboard with SYS_EN and gating it externally also was causing startup problems.
- Change KEY_LEFT_1 and KEY_RIGHT_2 inputs so they can be used to cause a manual reset when the PXA270 is powered down without backfeeding power into it. This involved changing the pullups on those lines from the SYS_EN switched 3.3V to non SYS_EN gated 3.3V and running the inputs to the processor through unused channels on the existing UTBD tristate buffer. It also involved adding an inverter to the tristate control on the previously unused buffer bank because the lower bank enable has the opposite sense as the one that was already in use.
- Add transistor on coma mode output between PSOC and coma mode latch to prevent leakage current from VPWRC back into PSOC input when in coma mode. Also provide population path for direct connection since that was not fully tested with PSOC software. Small leakage through the direct path does not result in an invalid level on the latch input when in coma mode - only in slightly higher power consumption.
- Change coma mode latch PRE-F input from being driven by CHRGR_PG_N to being driven by an inverted version of V4.5_CHRGR. This was done to eliminate leakage on CHRGR_PG_N back into PSOC while in coma mode that was causing the latch to believe the charger was connected. Making this change required the addition of '02 NOR gate used as an inverter to make the polarity of the input correct.
- BOM Changes
R80, R85 - New - 4.75K; U24, U28 - New - NC7SZ02P5X
R29, R87 - New - DNP; R31 - New - 1.00K; Q6 - New - MMBT2222
D13 - New - 1N4148; R84 - Delete; R86 - New - Zero Ohm

TODO:

TK0168-74-05 ESP HUB SCHEMATIC

(090112A)

Sht02_CardEng_DIMM_Socket
Sht02_CardEng_DIMM_Socket.Sch

Sht03_CardEng_AB_Hdrs
Sht03_CardEng_AB_Hdrs.Sch

Sht04_LCD_Interface
Sht04_LCD_Interface.Sch

Sht05_CF_Socket_Etc
Sht05_CF_Socket_Etc.Sch

Sht06_CC2431_ESPNET_Engine
Sht06_CC2431_ESPNET_Engine.Sch

Sht07_SysMgmt_uC_and_pwr
Sht07_SysMgmt_uC_and_pwr

Sht08_USB_Etc
Sht08_USB_Etc

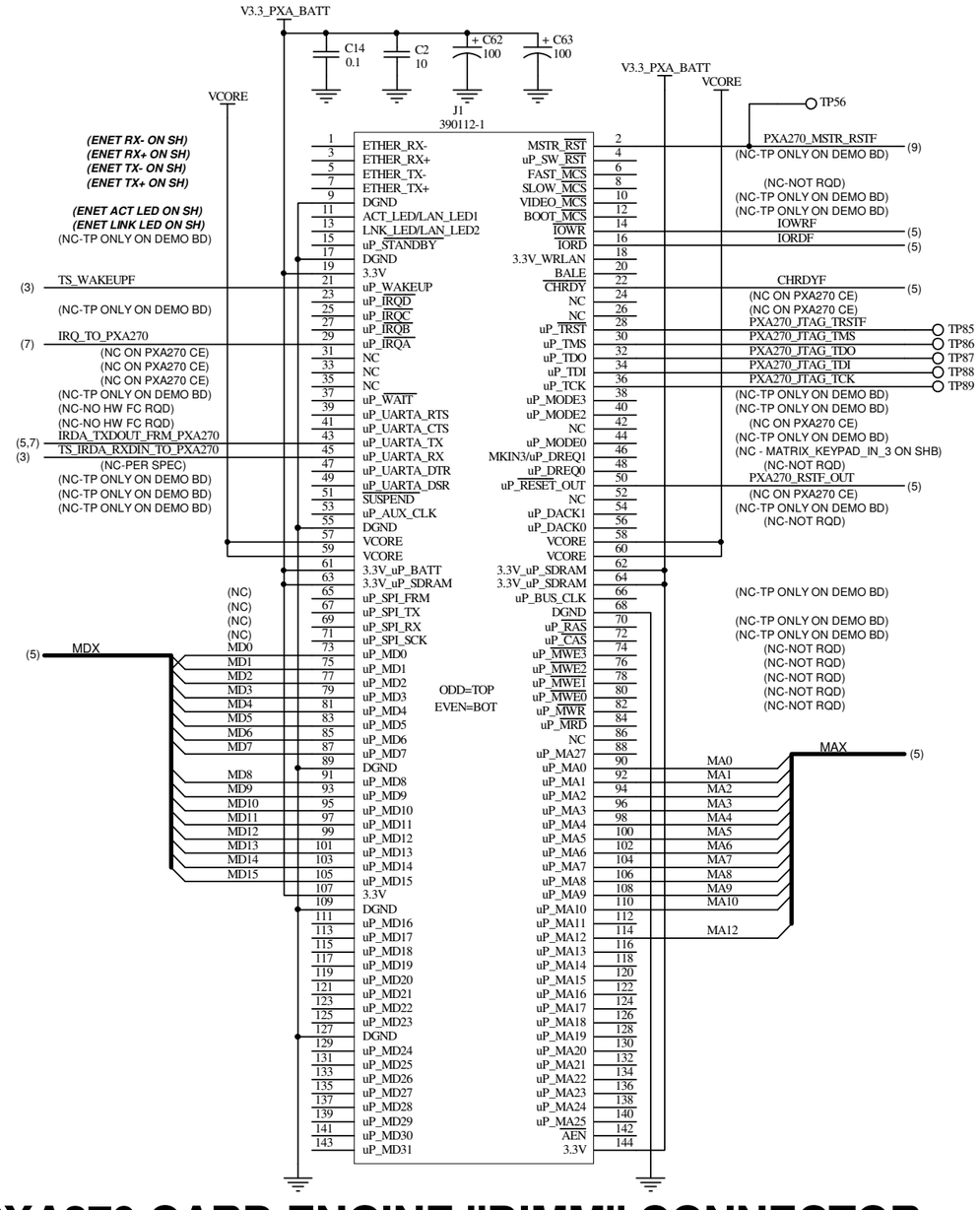
Sht09_RFID_Accelerometer
Sht09_RFID_Accelerometer

Sht10_Battery_Subsystem
Sht10_Battery_Subsystem

Sht11_Notes
Sht11_Notes

1

Title	ESP HUB		
Size: B	Number: TK0168-74-05		Revision: -
Date:	12-Jan-2009	Sheet X of Y	
File:	C:\wcn\Turnkey\jobs\ESP_TK0168_Hub\SCH_DBG\TK0168-05_ESP_Hub.ddb		



PXA270 CARD ENGINE "DIMM" CONNECTOR

Title	ESP HUB	
Size: B	Number: TK0168-74-05	Revision: -
Date: 12-Jan-2009	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0168_Hub\SCH_DSN\TK0168-05_ESP_Hub.ddb		

2

THE PURPOSE OF U23 IS TO TRISTATE INPUTS TO THE PXA270 CARD ENGINE WHEN THE PXA270 3.3V I/O SUPPLY IS NOT UP. THIS HAPPENS BRIEFLY AT POWER UP AND FOR AN EXTENDED PERIOD WHEN THE PXA270 IS POWERED DOWN WHEN THE HUB IS IN THE POWER MODE WHERE THE PXA270 CARD ENGINE IS

U24
NC7SZ02P5X
SYS_EN
INVERTED_SYS_EN
V3.3

U23
SN74HC241PWR
V3.3
KEY_LEFT_1
KEY_RIGHT_2
TS_KEY_LEFT_1
TS_KEY_RIGHT_2
(NC)
UART_TXD_FRM_CC2431
UART_PXA270_RX_FRM_PSOC
IRDA_RXDIN_TO_PXA270
WAKEUPF
TS_UART_TXD_FRM_CC2431
TS_UART_PXA270_RX_FRM_PSOC
TS_IRDA_RXDIN_TO_PXA270
TS_WAKEUPF
PSOC_TO_PXA270_WAKEUPF
CC2431_TO_PXA270_WAKEUPF
R1 DNP
R2 1.00K
R27 78.7K

V3.3_PXA_BATT
FB1 BLM18AG601
C15 0.1

V3.3_PXA_SW
R77 4.75K
R8 DNP-332
D3 DNP-GRN

J2
HIROSE: DF12(3.0)-80DS-05V

		A40	3.3VA	POWER_SENSE2	A80	(NC-SEE NOTE ABOVE))
(4)	TOUCH_TOP	A39	TOUCH_TOP	POWER_SENSE1	A79	(NC-SEE NOTE ABOVE))
(4)	TOUCH_BOTTOM	A38	TOUCH_BOTTOM	MIC_IN	A78	(NC - UNUSED IN THIS APP)
(4)	TOUCH_RIGHT	A37	TOUCH_RIGHT	DGND	A77	
(4)	TOUCH_LEFT	A36	TOUCH_LEFT	BUFF_DIR_DATA	A76	(NC - NOT RQD)
		A35	AGND	BUFF_DIR_ADDR	A75	(NC - NOT RQD)
TP8	AUDIO_OUT_R	A34	CODEC_OUTR	BUFF_OE	A74	(NC - NOT RQD)
	AUDIO_OUT_L	A33	CODEC_OUTL	uP_USB1_P	A73	(NC-NO USB FUNC)
	(NC-UNUSED)	A32	CODEC_INR	uP_USB1_M	A72	(NC-NO USB FUNC)
	(NC-UNUSED)	A31	CODEC_INL	uP_USB2_P	A71	(NC-NO USB HOST)
		A30	3.3VA	uP_USB2_M	A70	(NC-NO USB HOST)
	(NC-TP ONLY ON DEMO BD)	A29	VREFDRV	uP_USB1_PWR_EN	A69	(NC-NO USB FUNC)
	(NC-TP ONLY ON DEMO BD)	A28	uP_A/D_3	uP_USB2_PWR_EN	A68	(NC-NO USB HOST)
		A27	AGND	uP_USB1_VBUS	A67	
	(NC-TP ONLY ON DEMO BD)	A26	uP_A/D_2	DGND	A66	
	(NC-TP ONLY ON DEMO BD)	A25	uP_A/D_1	uP_USB2_OVR_CRNT	A65	uP_USB2_OVR_CRNT_F
		A24	DGND	CPLD_GPIO_2	A64	CPLD_GPIO_2 — TP11
	(NC-TP ONLY ON DEMO BD)	A23	uP_AC97_SD_OUT	CPLD_GPIO_1	A63	CPLD_GPIO_1_LED
	(NC-TP ONLY ON DEMO BD)	A22	uP_AC97_SD_IN	uP_PCC_RDYA	A62	(NC - TP ONLY ON DEMO BD)
	(NC-TP ONLY ON DEMO BD)	A21	uP_AC97_SYNC	CF_CE	A61	CF_CEF (5)
	(NC-TP ONLY ON DEMO BD)	A20	uP_AC97_RST	B5	A60	LCD_B5
	(NC-TP ONLY ON DEMO BD)	A19	uP_AC97_BITCLK	B4	A59	LCD_B4
uP_STATUS2_ENG1		A18	uP_STATUS2	B3	A58	LCD_B3
uP_STATUS1_ENG1		A17	uP_STATUS1	B2	A57	LCD_B2
	(NC ON PXA270 CE)	A16	NC	B1	A56	LCD_B1
	(NC ON PXA270 CE)	A15	NC	DGND	A55	
	(NC ON PXA270 CE)	A14	NC	B0	A54	LCD_B0
	(NC ON PXA270 CE)	A13	NC	G5	A53	LCD_G5 — ENG1_B[0:5] (4)
	(NC)	A12	LCD_PSAVE	G4	A52	LCD_G4
	(NC ON PXA270 CE)	A11	NC	G3	A51	LCD_G3
	(NC ON PXA270 CE)	A10	NC	G2	A50	LCD_G2
	(NC)	A9	DGND	G1	A49	LCD_G1
	(NC ON PXA270 CE)	A8	NC	G0	A48	LCD_G0 — ENG1_G[0:5] (4)
(4)	LCD_VDDEN	A7	LCD_VDDEN	R5	A47	LCD_R5
	(NC)	A6	LCD_VEEEN	R4	A46	LCD_R4
(4)	LCD_DEN_MDISP	A5	LCD_MDISP	R3	A45	LCD_R3
		A4	LCD_DON	DGND	A44	
(4)	LCD_DCLK	A3	LCD_DCLK	R2	A43	LCD_R2
(4)	LCD_HSYNC	A2	LCD_HSYNC	R1	A42	LCD_R1
(4)	LCD_VSYNC	A1	LCD_VSYNC	R0	A41	LCD_R0 — ENG1_R[0:5] (4)

V3.3_PXA_SW
R9 DNP-332
R10 DNP-332
D1 DNP-GRN
D2 DNP-GRN
FB2 BLM18AG601

"A" HEADER
(LCD, USB)

J3
HIROSE: DF12(3.0)-80DS-05V

(5)	KEY_LEFT_2	B40	MKIN1/MFP8	MFP38/SSPSFRM3	B80	(NC - NO EXT JTAG)
	(NC - NOT USED)	B39	MFP7	MFP37/SSPSTXD3	B79	(NC - NOT USED)
	(NC - NOT USED)	B38	MFP6	MFP36/SSPRXD3	B78	(NC - NOT USED)
	(NC - NOT USED)	B37	MFP5	DGND	B77	
	TS_KEY_LEFT_1	B36	MKIN0/MFP4	MFP34/SSPCLK3	B76	(NC - NOT USED)
	(NC - NOT USED)	B35	MFP3	MFP34/SYS_EN	B75	SYS_EN (8)
	(NC - NOT USED)	B34	MFP2	MFP33/PWR_EN	B74	(NC - NOT USED)
	(NC - NOT USED)	B33	MFP1	MFP32	B73	(NC-TP ONLY ON DEMO BD)
		B32	DGND	uP_SDCST	B72	(NC-NO EXT SDRAM)
	(NC - COMMON W/J1B47 ON CRD ENG)	B31	uP_IRRX	MFP30/SDA	B71	(NC-NO EXT SDRAM)
	(NC - COMMON W/J1B46 ON CRD ENG)	B30	uP_IRTX	uP_SDCKE	B70	(NC-NO EXT SDRAM)
	(NC-NO EXT SDRAM)	B29	uP_DQM0	MFP28	B69	(NC-TP ONLY ON DEMO BD)
	(NC-NO EXT SDRAM)	B28	uP_DQM1	MFP27/PWM1	B68	PXA270_TO_2431_CYA_1 (6)
	(NC-NO EXT SDRAM)	B27	uP_DQM2	MFP26/GPIO11	B67	(NC-NO BATT HERE)
	(NC-NO EXT SDRAM)	B26	uP_DQM3	DGND	B66	
	(NC-NO PCMCIA HERE)	B25	uP_PCC_PCDIR	MFP25/GPIO13	B65	(NC-NO BATT HERE)
	(NC-MATRIX_KEY_OUT_5 ON SH)	B24	MKOUT5/uP_PCC_DRV	MFP24/PWR_SDA	B64	(NC-NO BATT HERE)
	(NC-MATRIX_KEY_OUT_0 ON SH)	B23	MKOUT0/uP_PCC_VS2	MFP23/PWR_SCL	B63	(NC-NO BATT HERE)
	KEY_ESP	B22	MKOUT1/uP_PCC_VS1	MFP22	B62	(NC - NOT USED)
(5)		B21	DGND	MFP21	B61	PXA270_TO_2431_CYA_2 (6)
	(NC-NO PCMCIA HERE)	B20	uP_PCC_REG	MFP20	B60	(NC - NOT USED)
	(NC-MATRIX_KEY_OUT_4 ON SH)	B19	MKOUT4/PCC_CD1	MFP19/SCL	B59	(NC - NOT USED)
	(NC-MATRIX_KEY_OUT_3 ON SH)	B18	MKOUT3/PCC_CD2	MKIN5/MFP18	B58	TS_KEY_RIGHT_2
	KEY_RIGHT_1	B17	MKIN4/uP_PCC_BVD1	MFP17	B57	AUDIO_AMP_EN (10)
(5)	KEY_RIGHT_3	B16	MKOUT2/uP_PCC_BVD2	MFP16	B56	BEEP_VIBE_ENABLE (9)
(5)		B15	uP_PCC_WAIT	DGND	B55	(NC - NOT USED)
	(NC-NO PCMCIA HERE)	B14	uP_PCC_RDYB	MFP15	B54	(NC - NOT USED)
	(NC-NO PCMCIA HERE)	B13	uP_PCC_IOIS16	MFP14	B53	IRQ_FRM_PXA270 (7)
	(NC-NO PCMCIA HERE)	B12	PCC_CE2B	MFP13	B52	(NC - NOT USED)
	(NC-NO PCMCIA HERE)	B11	PCC_CE1B	MFP12/MMC_CLK	B51	(NC - NOT USED)
	(NC-NO PCMCIA HERE)	B10	uP_PCC_RESET	MFP11/MMC_DATA	B50	(NC - NOT USED)
		B9	DGND	MKIN2/MFP10	B49	KEY_LEFT_3 (5)
	(NC-NO PCMCIA HERE)	B8	uP_PCC_IOWR	MFP9/MMC_CMD	B48	(NC - NOT USED)
	(NC-NO PCMCIA HERE)	B7	uP_PCC_IORD	uP_UARTC_RX	B47	TS_UART_TXD_FRM_CC2431
	(NC-NO PCMCIA HERE)	B6	uP_PCC_WE	uP_UARTC_TX	B46	UART_RXD_TO_2431 (6)
	(NC-NO PCMCIA HERE)	B5	uP_PCC_OE	uP_UARTB_RTS	B45	(NC - NOT USED)
	(NC - NOT USED)	B4	CPLD_TDI	DGND	B44	
	(NC - NOT USED)	B3	CPLD_TMS	uP_UARTB_CTS	B43	(NC - NOT USED)
	(NC - NOT USED)	B2	CPLD_TDO	uP_UARTB_RX	B42	TS_UART_PXA270_RX_FRM_PSOC
	(NC - NOT USED)	B1	CPLD_TCK	uP_UARTB_TX	B41	UART_PXA270_TX_TO_PSOC (7)

"B" HEADER
(PCMCIA, UARTS, ETC)

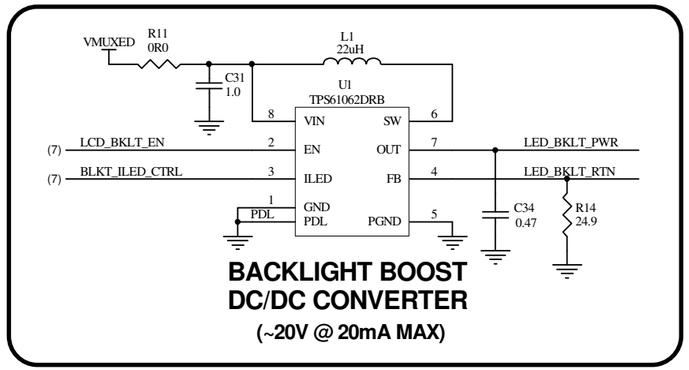
UART ASSIGNMENTS

UART A - LOLO CONSOLE PORT & IRDA
UART B - SYS MGMT MICROCONTROLLER
UART C - NETWORK PROCESSOR IFACE

3

PXA270 CARD ENGINE "A" AND "B" HEADERS

Title: ESP HUB		
Size: B	Number: TK0168-74-05	Revision: -
Date: 12-Jan-2009	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0168_Hub\SCH_PCB\TK0168-05_ESP_Hub.ddb		



BACKLIGHT BOOST DC/DC CONVERTER

(~20V @ 20mA MAX)

LCD PWR RQMTS

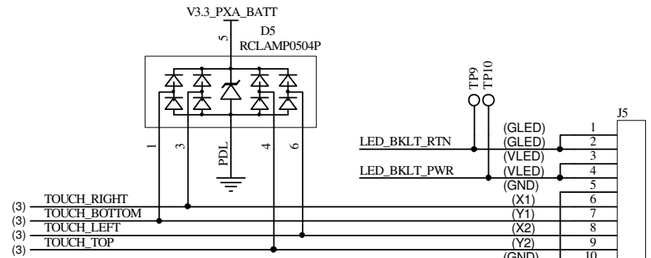
VCC 3.3 @ @ 1.3 - 5mA
AVDD 5.0 @ 2-5mA
VGH 15.0 @ 100-300uA
VGL -10 @ 100-300uA
VLED ~20V @ 20mA
VCOM TBD AC @ ? current

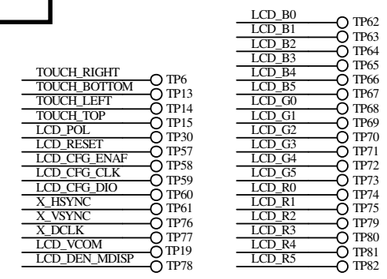
INNOLUX PT035 TOUCH INFO

X1 - RIGHT - PIN 6
Y1 - BOTTOM - PIN 7
X2 - LEFT - PIN 8
Y2 - TOP - PIN 9

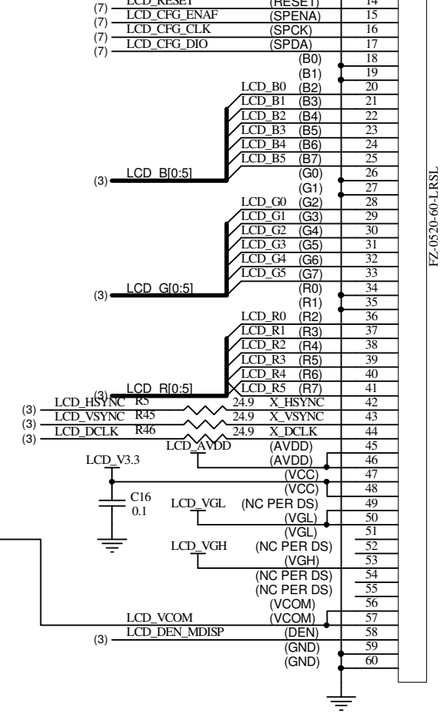
TOUCH SCREEN INPUT ESD PROTECTION

(NOTE: .01uF CAPS ON THESE LINES ON CARD ENGINE TOO)





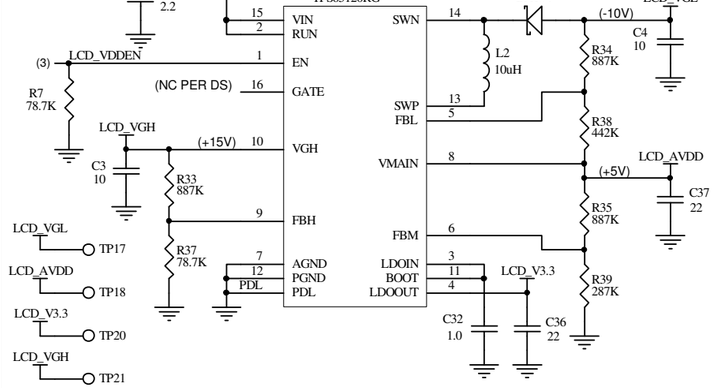
LCD INTERFACE TEST POINTS



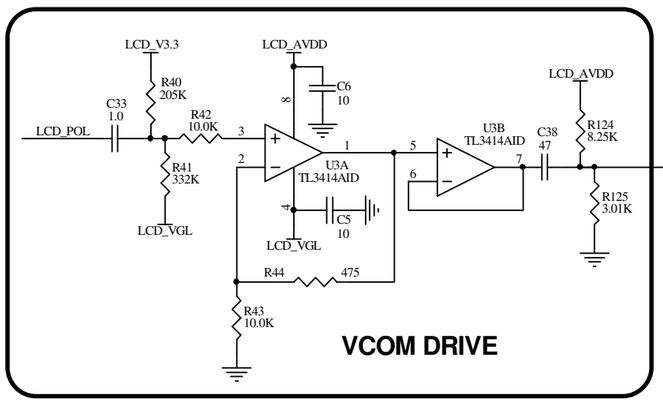
LCD PANEL FFC CONNECTOR

TPS65120 VOLTAGE SETTINGS

VMAIN=AVDD=1.213*(887K+287K)/287K=5.0V
VGH=1.213*(887K+78.7K)/78.7K= 14.9V
VGL=-VMAIN*(RA/RB)=5*(887/442)=-10.0V
VLDO=3.3V (Fixed)



LCD +3.3, +5.0, +15.0 & -10.0V POWER SUPPLY

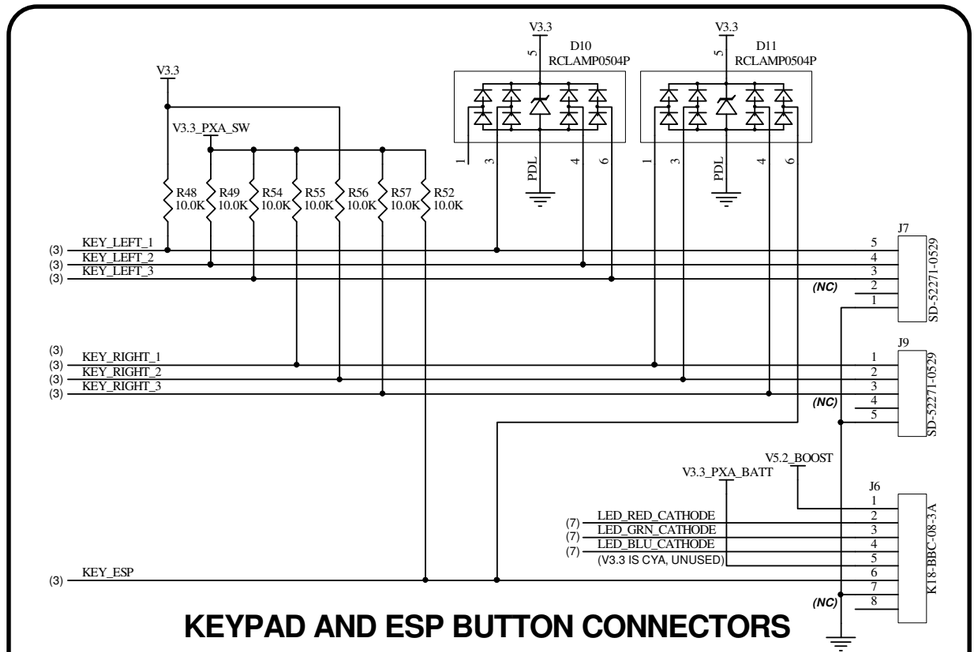


VCOM DRIVE

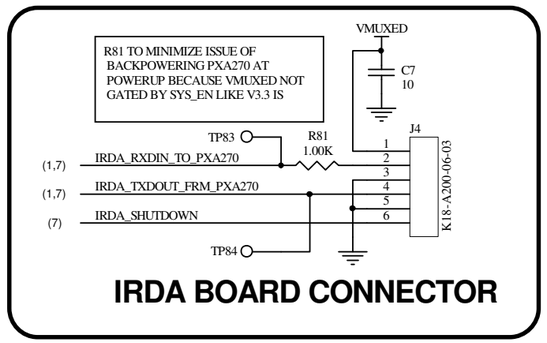
LCD POWER & INTERFACE

Title: ESP HUB		
Size: B	Number: TK0168-74-05	Revision: -
Date: 12-Jan-2009	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0168_Hub\SCH_DBK\TK0168-05_ESP_Hub.ddb	Drawn By:	

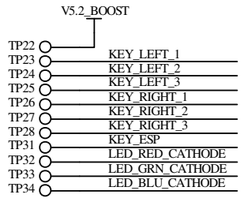
4



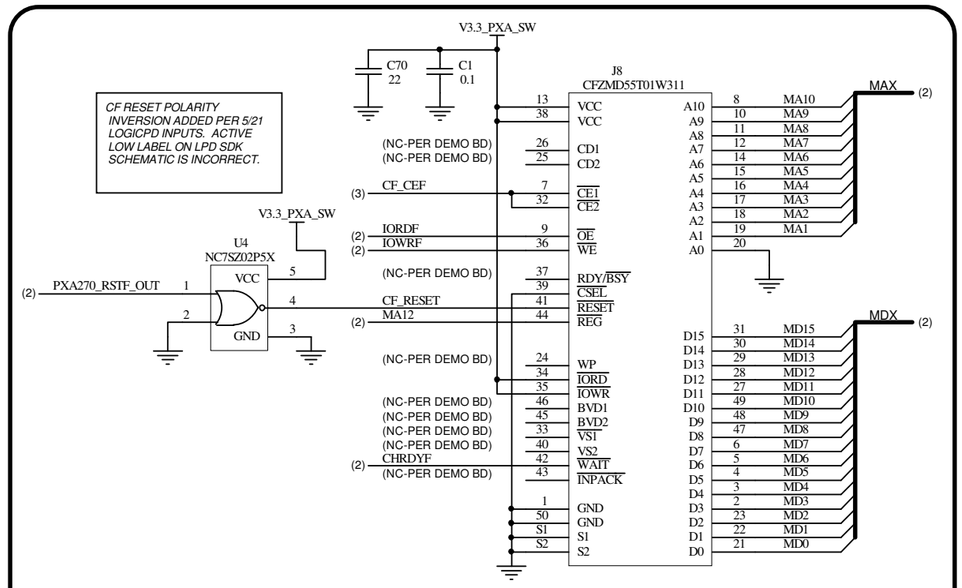
KEYPAD AND ESP BUTTON CONNECTORS



IRDA BOARD CONNECTOR



KEYPAD & LED TESTPOINTS



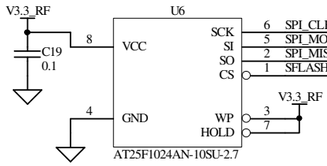
COMPACT FLASH SOCKET

5

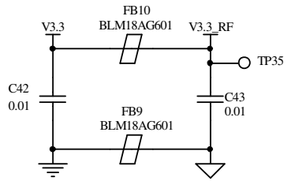
COMPACT FLASH, IRDA & KEYPAD INTERFACE

Title: ESP HUB		
Size: B	Number: TK0168-74-05	Revision: -
Date: 12-Jan-2009	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0168_Hub\SCHEMATICS\TK0168-05_ESP_Hub.ddb	Drawn By:	

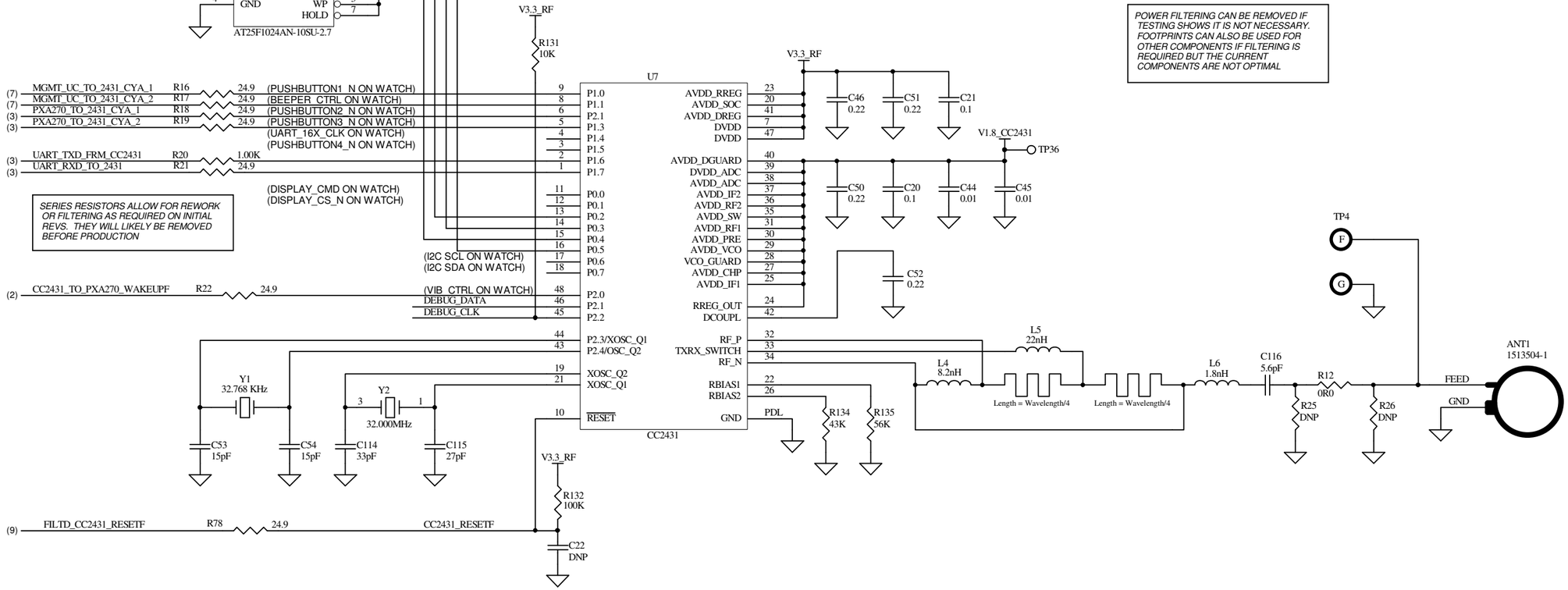
128KB SERIAL EEPROM FOR OTA UPDATE (TBD IF RQD OR NOT)



POWER FILTERING

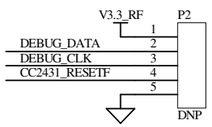


POWER FILTERING CAN BE REMOVED IF TESTING SHOWS IT IS NOT NECESSARY. FOOTPRINTS CAN ALSO BE USED FOR OTHER COMPONENTS IF FILTERING IS REQUIRED BUT THE CURRENT COMPONENTS ARE NOT OPTIMAL



SERIES RESISTORS ALLOW FOR REWORK OR FILTERING AS REQUIRED ON INITIAL REVS. THEY WILL LIKELY BE REMOVED BEFORE PRODUCTION

CC2431 PGM & DBG (DNP IN PRODUCTION)



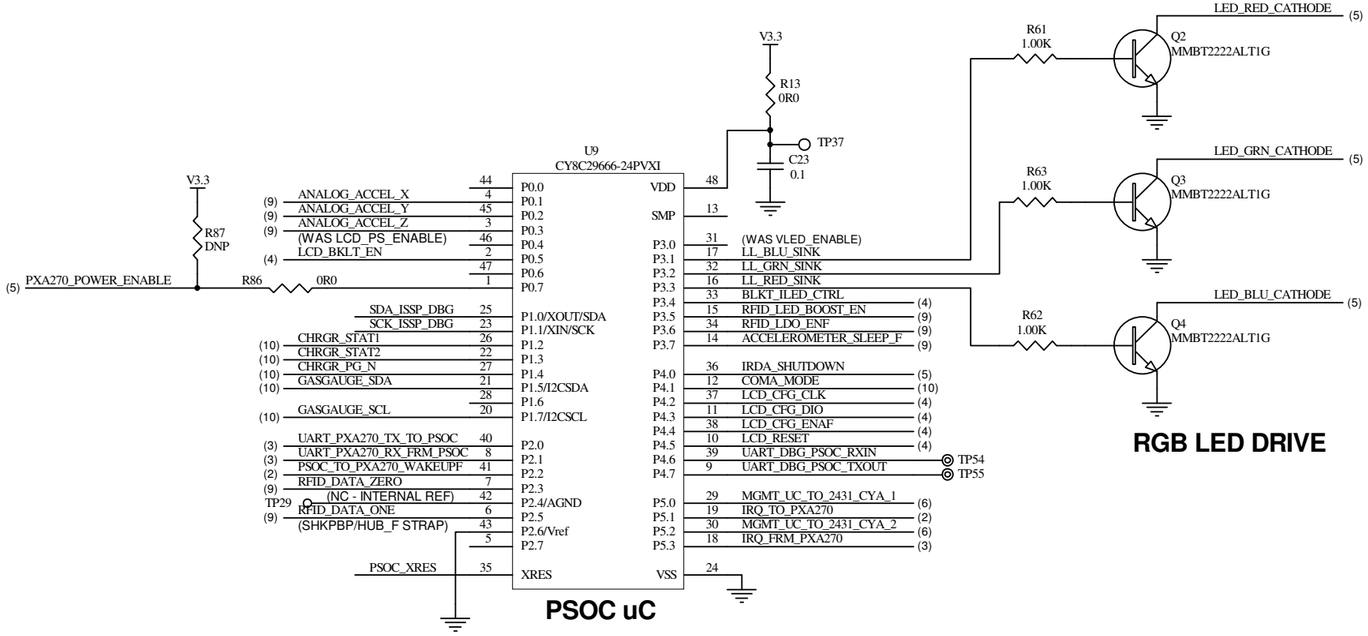
CC2431 NETWORK ENGINE

6

Title: ESP HUB		
Size: B	Number: TK0168-74-05	Revision: -
Date: 12-Jan-2009	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0168_Hub\SCH\TK0168-05_ESP_Hub.ddb		

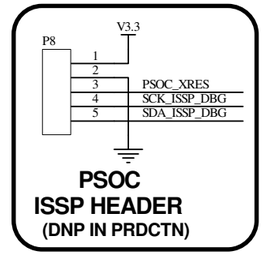
PSOC I/O (From 10/2 Designer Project)

Accel X - ADC IN - P0.1
Accel Y - ADC IN - P0.2
Accel Z - ADC IN - P0.3
LED_RED - PWM - P3.3
LED_GRN - PWM - P3.2
LED_BLU - PWM - P3.1
PWM - LCD BKLT - P3.4
I2C_GASGAUGE_SDA - P1.5
I2C_GASGAUGE_SCL - P1.7
UART_PXA270_RXIN - P2.0
UART_PXA270_TXOUT - P2.1
UART_DBG_RXIN - P4.6
UART_DBG_TXOUT - P4.7
LCD_CFG_CLK - P4.2
LCD_CFG_DIO - P4.3
LCD_CFG_ENAF - P4.4
LCD_RESET - P4.5
RFID_BOOST_ENA - P3.5
RFID_LDO_ENAF - P3.6
ACCEL_PWR_ENA - P3.7
LCD_BKLT_ENA - P0.5
LCD_PNL_PWR_ENA - P0.6
PXA270_VCORE_ENA - P0.7
CYA_2431_IO_1 - P5.0
IRQ_TO_PXA270 - P5.1
CYA_2431_IO_2 - P5.2
IRQ_FRM_PXA270 - P5.3
CHRGR_STAT1 - P1.2
CHRGR_STAT2 - P1.3
CHRGR_PG_N - P1.4



PSOC uC

RGB LED DRIVE



PSOC ISSP HEADER (DNP IN PRDCTN)

CYPRESS PSOC NOTES

27443 - TSSOP28 - 16KB, 8 DIG, $2.88 DK 1K ($2.40 Avnet)
27543 - TQFQ44 - 16KB, 8 DIG, $3.43 DK 1K
27643LF - QFN48 - 16KB, 8 DIG, $3.57 DK 2K
27643PV - SSOP-48 - 16KB, 8 DIG, $3.10 DK 1K

29466 - TSSOP28 - 32KB, 16 DIG, DK $3.95 1K ($3.30 Avnet)
29566 - TQFP44 - 32KB, 16 DIG, DK $4.38 1K
29666LF - QFN48 - 32KB, 16 DIG, DK $4.63 1K
29666PV - SSOP-48 - 32KB, 16 DIG, DK $4.13 1K

"SYSTEM MANAGEMENT" MICROCONTROLLER (PSOC)

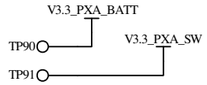
Title: ESP HUB		
Size: B	Number: TK0168-74-05	Revision: -
Date: 12-Jan-2009	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0168_Hub\SCH_DBK\TK0168-05_ESP_Hub.ddb		

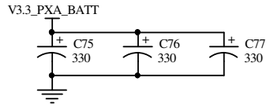
3.3V POWER NOTES:

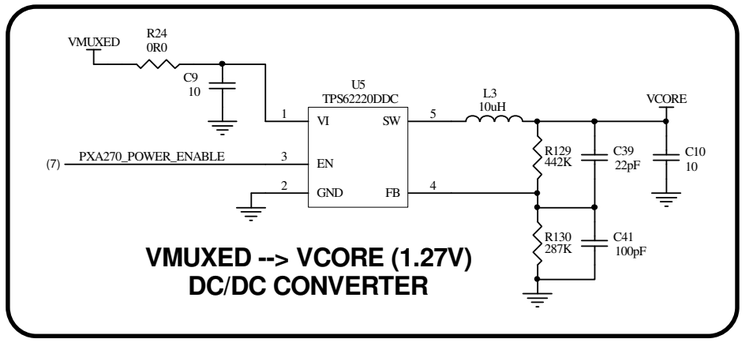
100mA - Card Engine - MAX) w/b 250mA with ethernet
30mA - Estimate from typical 512MB max write current
35mA - CC2431 subsystem - max
30mA - PSOC - high estimate - may be single digit
20mA - Status LEDs - estimate - can be depop'd in prdctn

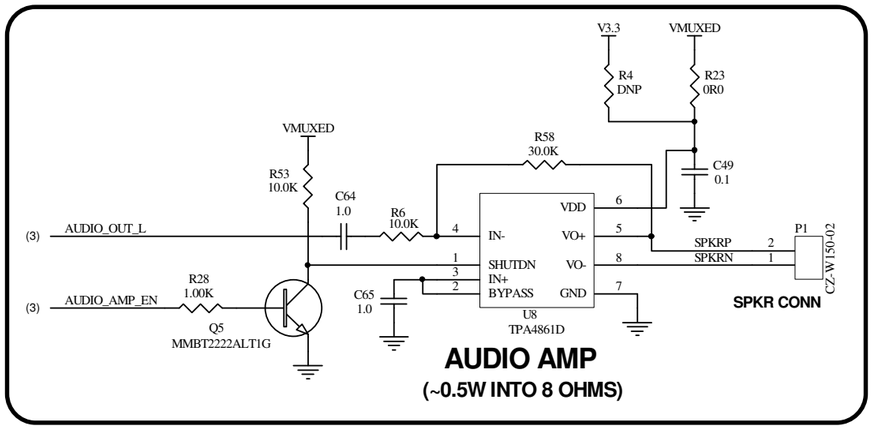
215mA max

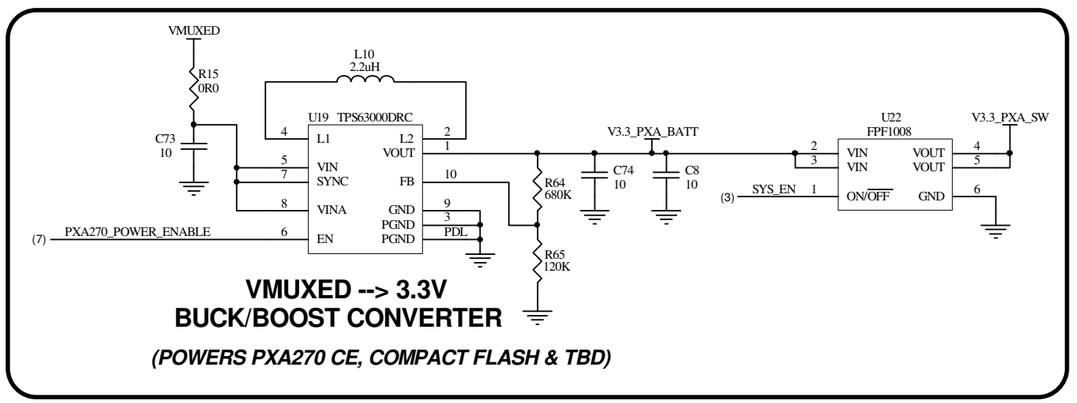
Typical w/active card engine is likely to be ~90mA

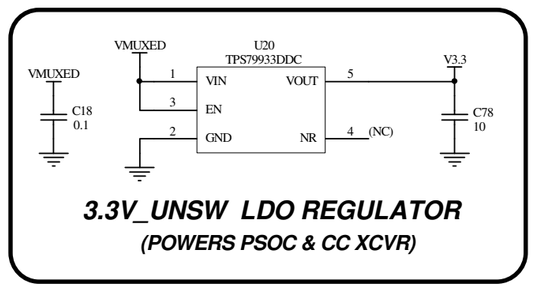


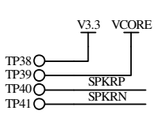












3.3V AND VCORE POWER SUPPLIES & AUDIO AMP

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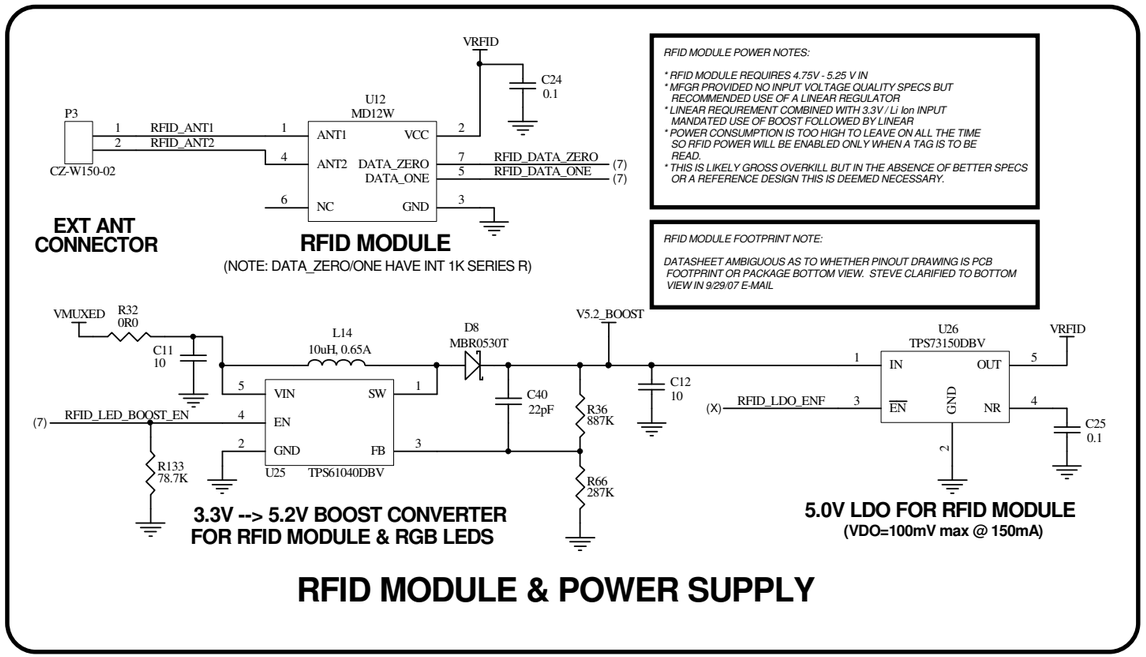
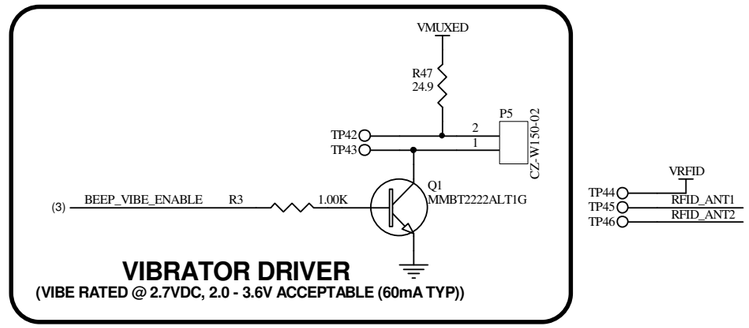
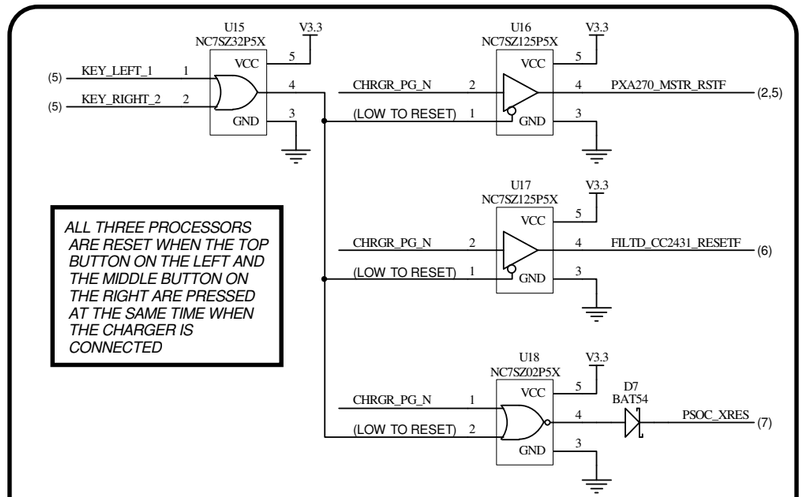
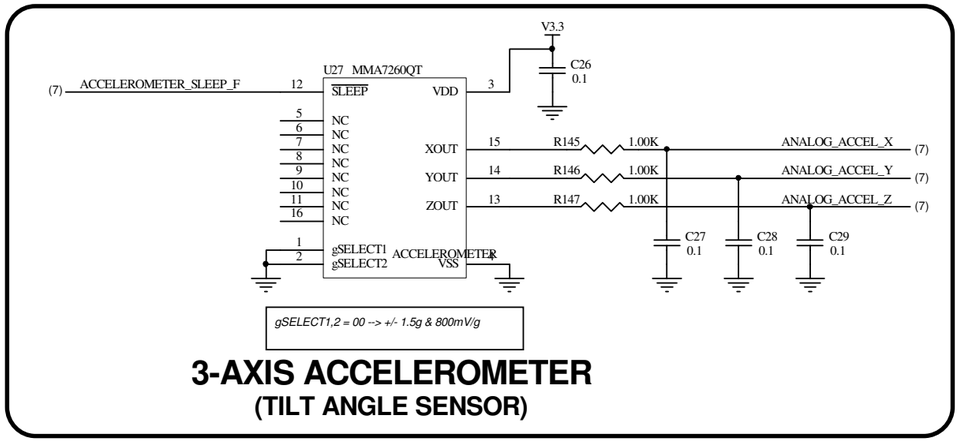
Title: ESP HUB		
Size: B	Number: TK0168-74-05	Revision: -
Date: 12-Jan-2009	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0168_Hub\SCH_PCB\TK0168-05_ESP_Hub.ddb	Drawn By:	









RFID MODULE, ACCELEROMETER, ETC.

Title: ESP HUB		
Size: B	Number: TK0168-74-05	Revision: -
Date: 12-Jan-2009	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0168_Hub\SCHEMATIC\TK0168-05_ESP_Hub.ddb	Drawn By:	

POWER MUX IS REQUIRED BECAUSE WITHOUT A PATH AROUND THE CHARGER FOR INPUT CURRENT, A LOW CHARGE STATE LI-ION CELL WOULD NEVER CHARGE BECAUSE THE SYSTEM WOULD CONSUME ALL OF THE PRECHARGE CURRENT (AND MORE IF ALLOWED) ALLOWING NO CURRENT TO FLOW INTO THE CELL. SCHOTTKY ORING WAS CONSIDERED BUT DISQUALIFIED BECAUSE IT WOULD RESULT IN A 0.35V MINIMUM DROP ON THE BATTERY VOLTAGE WHICH WOULD HAVE THE ELECTONICS DROPPING OUT WHILE THERE WAS STILL ENERGY IN THE CELL. AN ACTIVE MUX SWITCH WAS LESS EXPENSIVE ($ AND REAL ESTATE-WISE) THAN SCHOTTKYS PLUS A BUCK BOOST SUPPLY.

COMA MODE IMPLEMENTATION NOTES:
TPS2114 D0=1, D1=0 --> OUT connected to higher input
TPS2114 D0=1, D1=1 --> OUT is hi-z
74LVC2G74 QN OUT WHEN CLRn=0,PRE=0 is HIGH

STAT OUTPUT NOT REQUIRED BECAUSE SAME INFO AVAILABLE FROM CHARGER PG_N IN THIS DESIGN

VIH MIN FOR TPS2114/5 IS 2.0V. EVEN W/VBAT @ 3.4V --> VPWRC @ 2.7V, SNXXX GUARANTEES VOH MIN OF 2.6V W/THIS LOAD

VMUXED V3.3
TP2 TP3
TP7 TP12

TP47 TP48

U10 TPS62110RSA
C17 10
C66 1.0
L8 6.8
R50 442K
C69 10pF
C67 22
C55 0.1
R67 154K
R80 4.75K
D13 1N4148W
V4.5_CHRGR

DC/DC BUCK CONVERTER
(17V IN MAX; 1.5A OUT MAX)

U28 NC7SZ02P5X
VPWRC
CHARGER_PRESENT_F

U11 TPS2115APW
C56 0.1
R68 330
PM_RILIM (INT PU)
VBAT
C30 10
(NC)

POWER MUX

COMA_CTRL_COMA_NORMAL_F
D9 1N4148W
D12 1N4148W
U21 SN74LVC2G74
R83 78.7K
R82 DNP
COMA_MODE_F
R29 DNP
(7) COMA_MODE
R31 1.00K
R85 4.75K
Q6 MMBT2222ALT1G

"COMA MODE" CONTROL LATCH

CHARGER CONNECTOR

P4 K108-B000-02-2
V15_CHARGER
R60 10.0K
C59 0.1

U13 BQ24120RLH
C47 10
R79 DNP
L9 4.7uH
D6 18V
C48 10
C72 10
R70 0.10
TP50
P6 K108-B000-02-3
TP51
RTN_BAT
R69 9.31K
C13 0.1
C68 0.1
PACK_TEMPSENSE
TP49
R59 10.0K
TP1
C71 0.22
R75 5.90K
R76 5.90K
(7) CHRGR_STAT1
(7) CHRGR_STAT2
(7) CHRGR_PG_N

LI-ION CHARGER

BATTERY CONNECTOR

U14 BQ27210DRK
R72 1K
R71 .02
R73 1K
R74 1K
C61 0.1
C60 0.1
C57 0.1
C58 0.1
TP5
GASGAUGE_SCL (7)
GASGAUGE_SDA (7)
PDL

SEE PP4, 10 OF TI BQ27X10EVM MANUAL (TI DOC SLUU259) FOR CONFIRMATION THAT THE GAS GAUGE, CHARGER AND SYSTEM CONNECTIONS HERE ARE CORRECT.

"GAS GAUGE" IC

I2C ADR = AA/AB
SCL, SDA RESISTORS FOR DEBUG BREAKOUT ONLY

R(ISET1)=5.90K --> FAST CHARGE @ 1.7A
R(ISET2)=5.90K --> PRE CHARGE @ 0.17A
C(TTC)=0.22uF --> 9.5HR NOM SAFETY TIMER
9.31K,442K TS DIVIDER => 0 - 45 DEG C
DETAILED CALCS IN CHET NOTEBOOK FOR 9/18/07

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LI-ION CHARGER, GAS GAUGE, POWER MUX, ETC

Title: ESP HUB		
Size: B	Number: TK0168-74-05	Revision: -
Date: 12-Jan-2009	Sheet X of Y	
File: C:\wcn\Turnkey\jobs\ESP_TK0168_Hub\SCH\ESP_TK0168-05_ESP_Hub.ddb		

POWER NET DESCRIPTIONS:

V15_CHARGER is the raw 15V DC charger input. It feeds the switchmode battery charger directly. It also gets bucked down to V4.5_CHRGR to provide power all the non-charger electronics when connected to the charger

V4.5_CHRGR is the bucked down version of V15_CHRGR. V4.5_CHRGR goes into the power mux and powers the system when it is connected to the charger.

VBAT is the battery input. When the battery is charging current flows into the battery via this net. When off charger, all the power to run the system comes in on this net.

VMUXED is an intelligently "OR'd" combination of V4.5 Charger and VBAT. It is sourced by the charger when the charger is connected and by the battery when the charger is not connected. It is also gated by the "COMA Mode" control.

VPWRC is a diode OR'd combination of V4.5_CHRGR and VBAT. It is used to power the "COMA Mode" circuitry that can not be powered by the power mux because it is used to control the power mux (chicken and egg problem)

V3.3 powers the PSOC system management microcontroller, and the CC2431 RF transceiver. It also powers some 3.3V peripherals that are not directly connected to the PXA270. V3.3 is present at all times that VMUXED is present which is anytime there is a charger connected or a battery installed and the system is not in Coma Mode.

V3.3_RF powers the Chipcon CC243X transceiver subsystem. It is directly powered by V3.3 and is really just V3.3 passed through a simple filter.

V3.3_PXA_BATT is the source to the PXA270 card engine 3.3V_uP_BATT and general 3.3V input input. It can be turned off by the PSOC system management microcontroller but is not gated by teh PXA270 SYS_EN signal as the V3.3_PXA_SW rail that powers the remainder of the PXA270 and tightly coupled peripherals is. The _BATT in the net name is a bit of a misnomer since it is not powered directly by the battery and is switched by another microcontroller.

V3.3_PXA_SW powers the compact flash Card. V3.3_PXA_SW is sourced by the same converter as V3.3_PXA_BATT but passes through a high side switch controlled by the PXA270 SYS_EN signal. It is gated by SYS_EN to prevent the CF interface from back powering the PXA before the PXA 3.3V I/O is powered up.

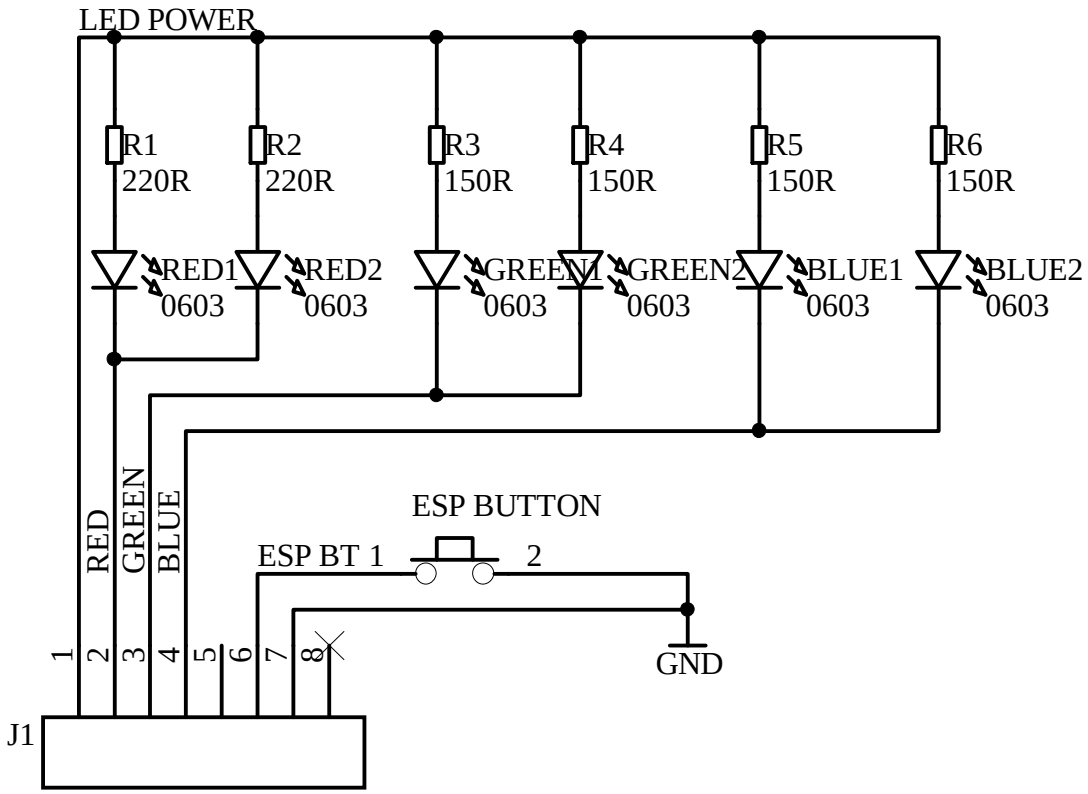
VCORE is the 1.27V supply to the PXA270 core. It is switched by the PSOC in order to be able to completely turn the PXA270 off. Its' voltage is a function of the operating frequency of the card engine. For a 312MHz card engine it can be as low as 1.18V. Logic suggested 1.25V. 1.27V was chosen here because it could be achieved with existing resistor values.

LCD_XXX are four power rails that are specific to the LCD display (exclusive of the backlight). They are generated by a single application specific DC/DC converter. All the LCD_XXX rails are controlled by the LCD_VDDEN signal from the PXA270 card engine (by the PSOC sys mgmt uC before 6/3/08).

LCD_BKLT_PWR is the power for the LED backlight for the LED display. It is an ~20V boost converter with variable current output. The supply is enabled and current controlled by the PSOC sys mgmt uC but is ultimately controlled by the application running in the PXA270.

NOTES

Title	ESP HUB		
Size: B	Number: TK0168-74-05		Revision: -
Date:	12-Jan-2009	Sheet X of Y	
File:	C:\wcn\Turnkey\jobs\ESP_TK0168_Hub\SCHEMS\TK0168-05_ESP_Hub.ddb		


LED POWER
R1
220R
R2
220R
R3
150R
R4
150R
R5
150R
R6
150R
RED1
0603
RED2
0603
GREEN1
0603
GREEN2
0603
BLUE1
0603
BLUE2
0603
RED
GREEN
BLUE
ESP BUTTON
ESP BT 1
2
GND
1
2
3
4
5
6
7
8
J1

INFORMAL REVISION HISTORY:

* STARTED 1/8/08

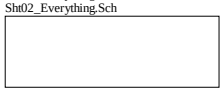
TODO:

1 - COVER
2 - TBD

TK0177-74-01 ESP HUB IRDA BOARD

(0801080A)

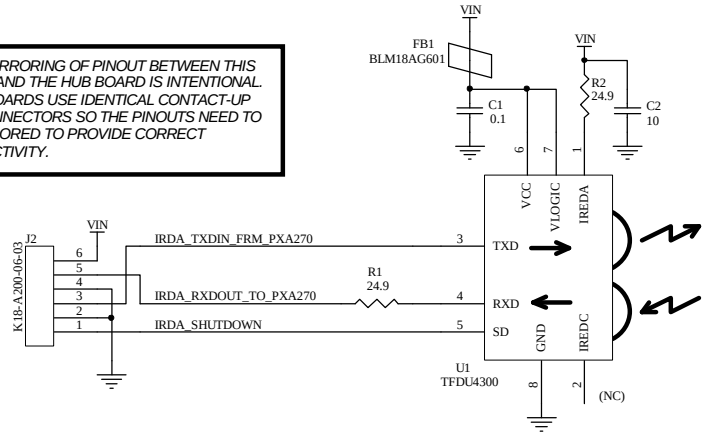
Sht02_Everything
Sht02_Everything.Sch



1

Title: ESP HUB		
Size: B	Number: TK0168-74-01	Revision: -
Date: 13-Feb-2009	Sheet X of Y	
File: D:\Workshop\ESP\3rd Research\Design\HUB IRDA\TK0177_-01_ESP_Hub_IRDA_Board		

NOTE: MIRRORING OF PINOUT BETWEEN THIS BOARD AND THE HUB BOARD IS INTENTIONAL. BOTH BOARDS USE IDENTICAL CONTACT-UP FFC CONNECTORS SO THE PINOUTS NEED TO BE MIRRORED TO PROVIDE CORRECT CONNECTIVITY.



Title			
Size: B	Number		Revision
Date: 13-Feb-2009		Sheet of	
File: D:\Workshop\ESP\3rd Research\Design\HUB\IRDA\TK0177_-01_ESP_Hub_IRDA_Board			