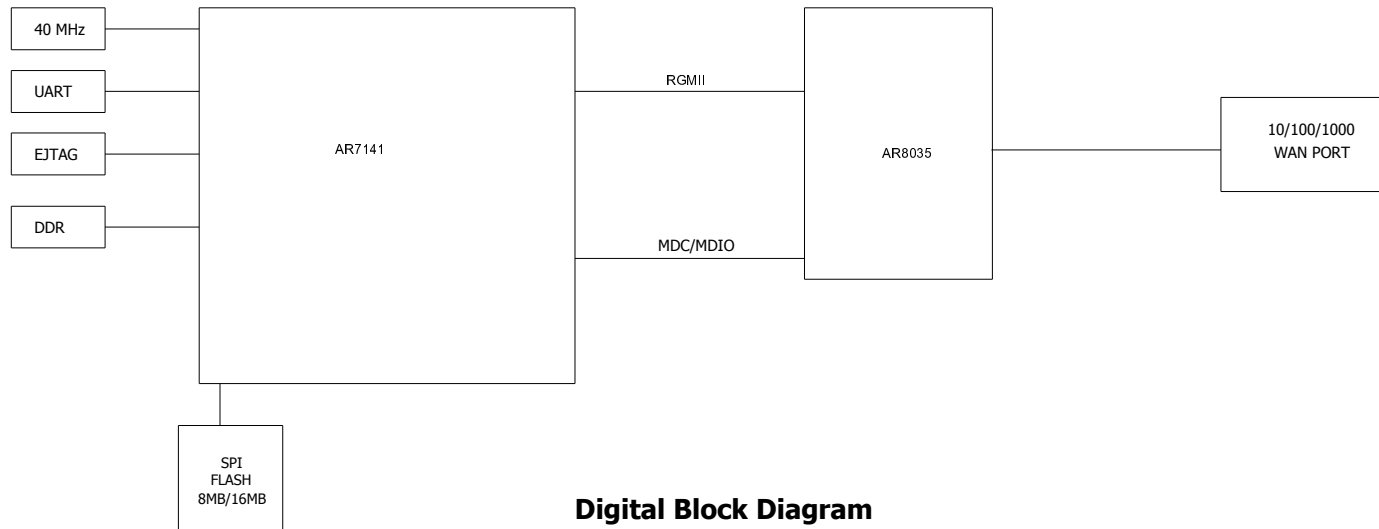


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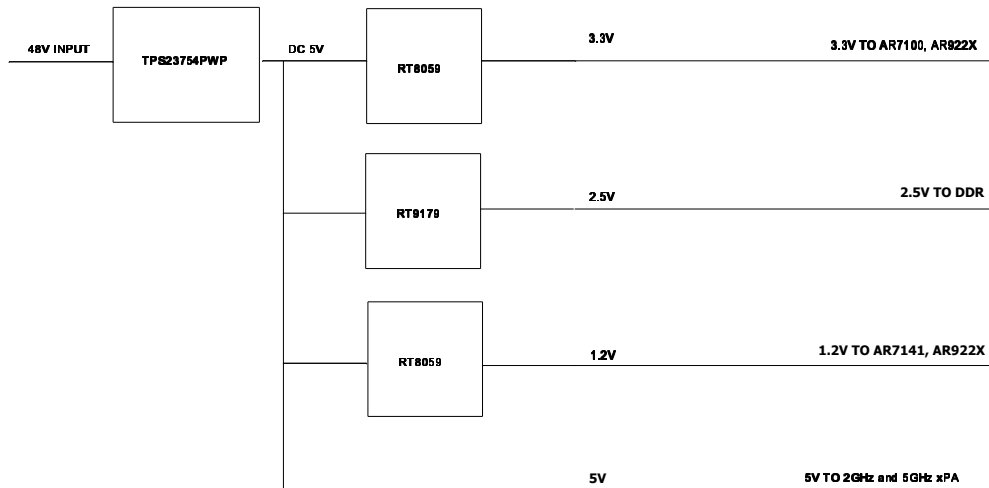
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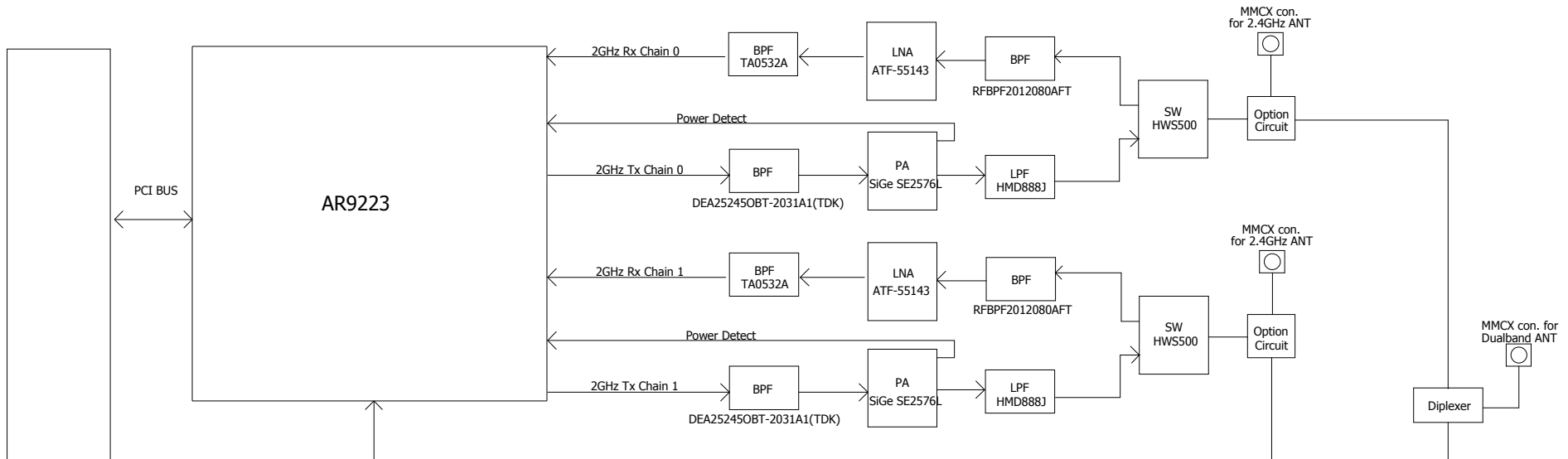
802.11 a/b/g/n 2.4/5GHz

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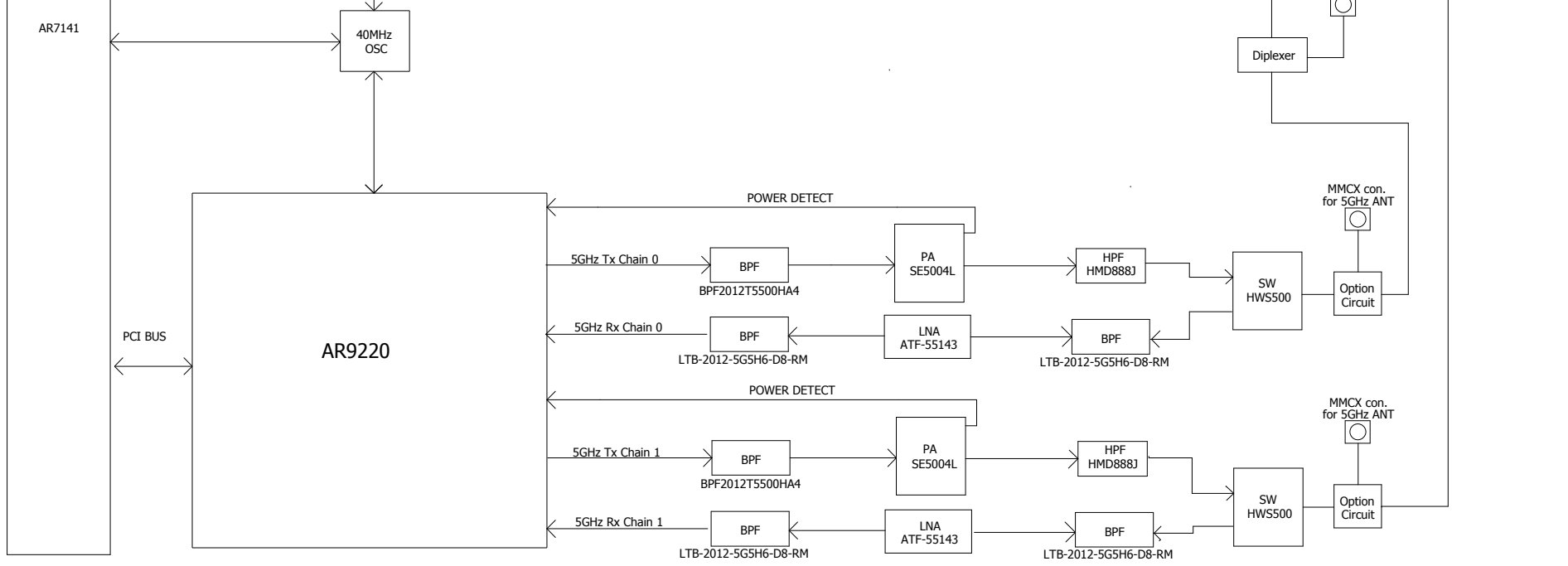


Digital Block Diagram

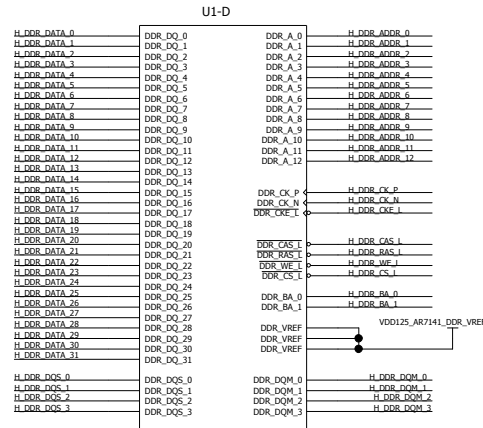
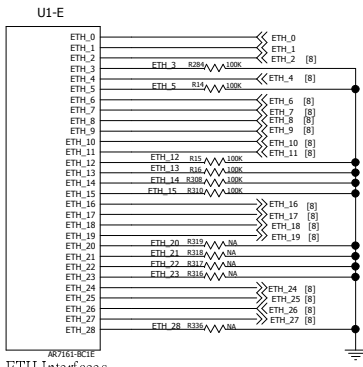
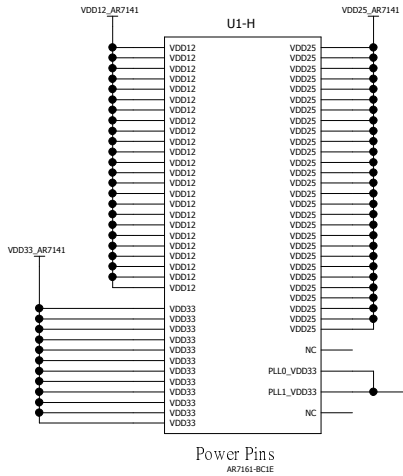
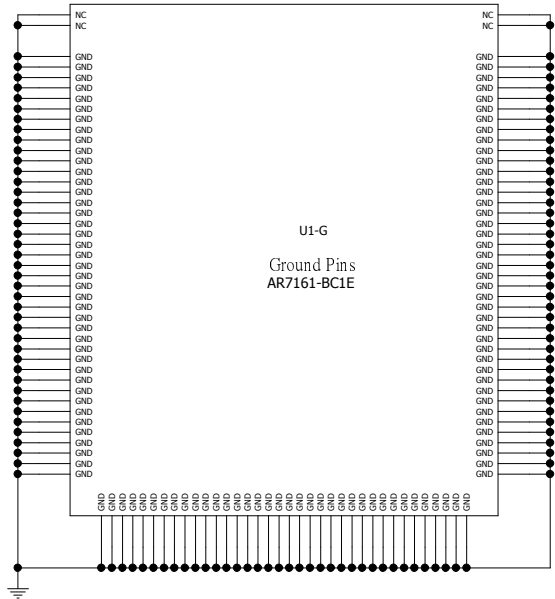




2.4GHz Radio Block Diagram

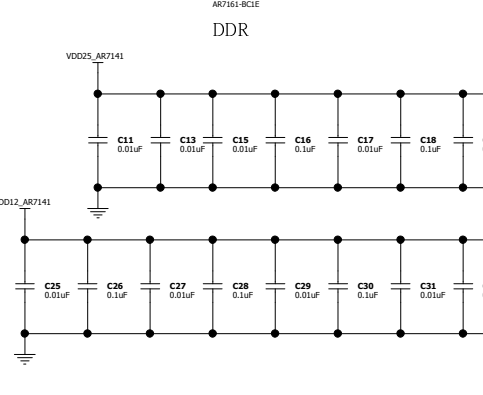
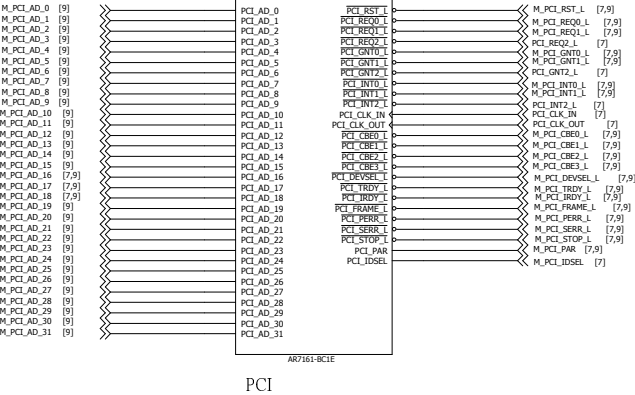


5GHz Radio Block Diagram

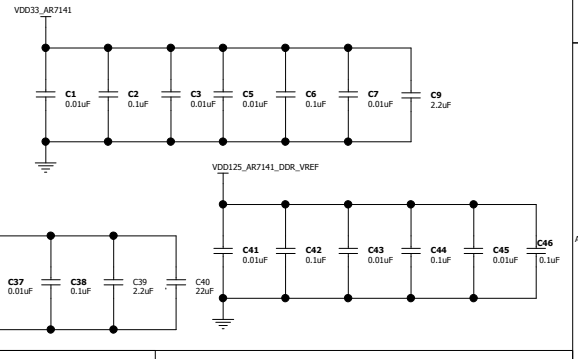
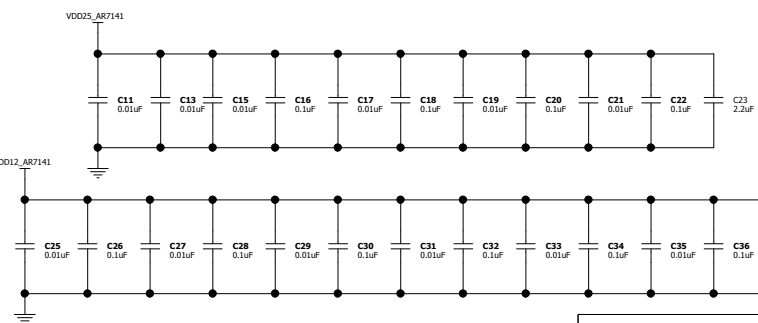


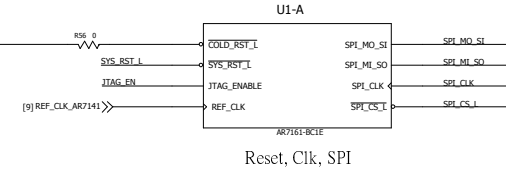
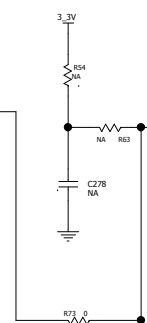
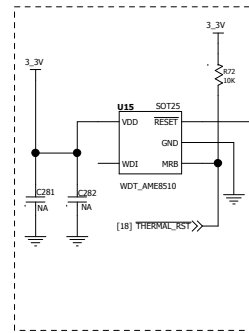
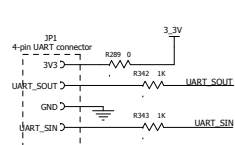
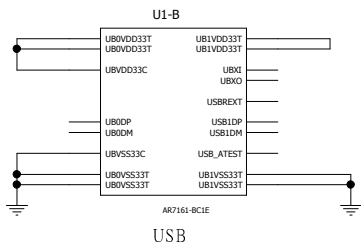
ETH Interfaces

MII interfaces

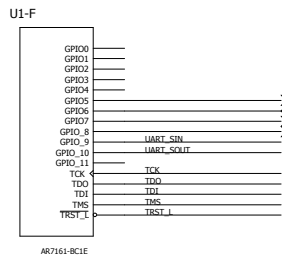
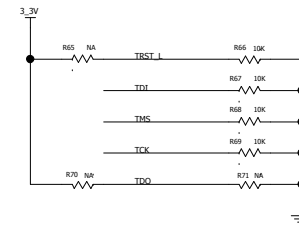
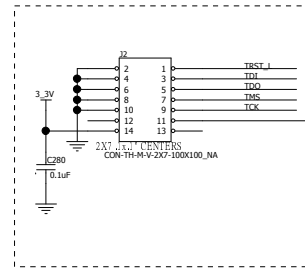
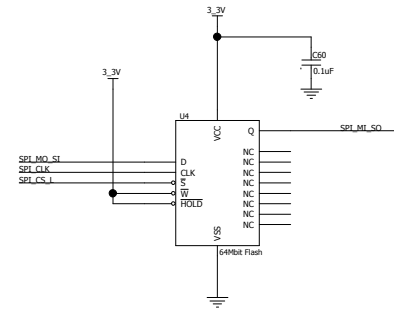
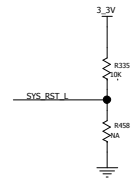


DDR

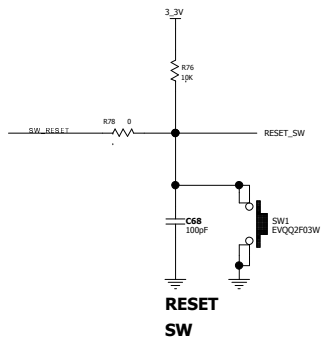
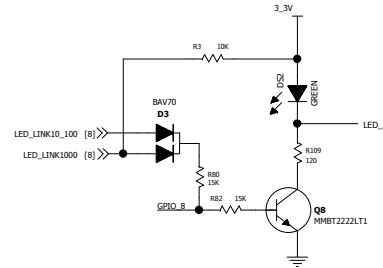
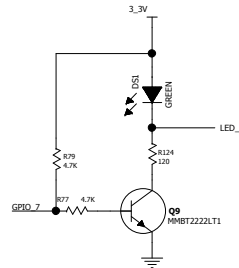




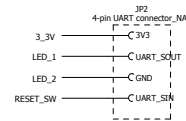
Reset, Clk, SPI

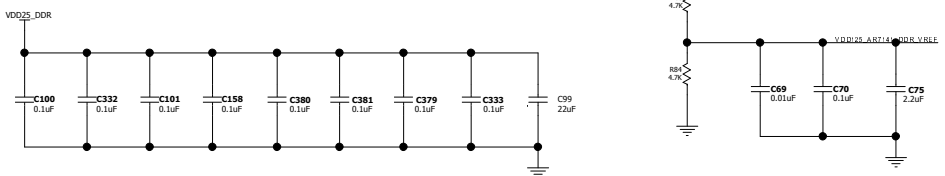
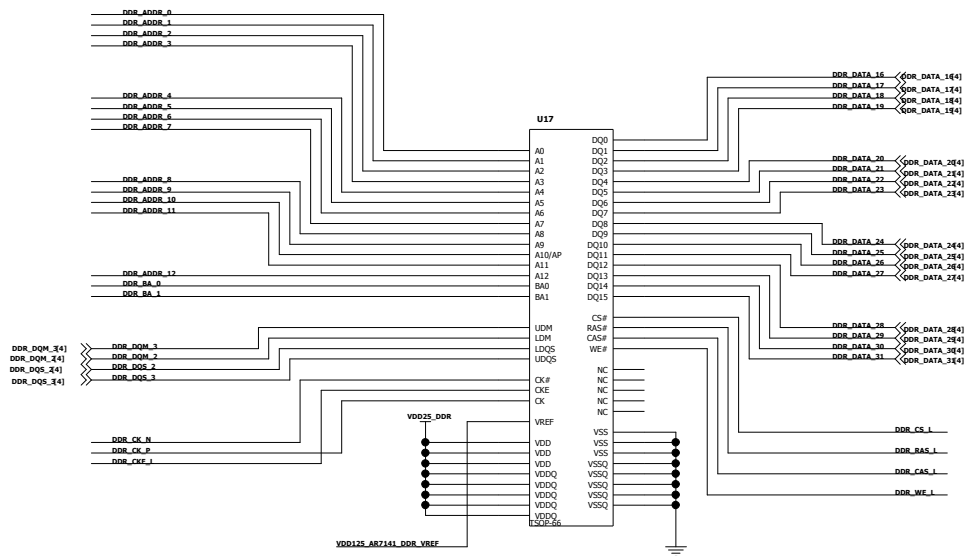
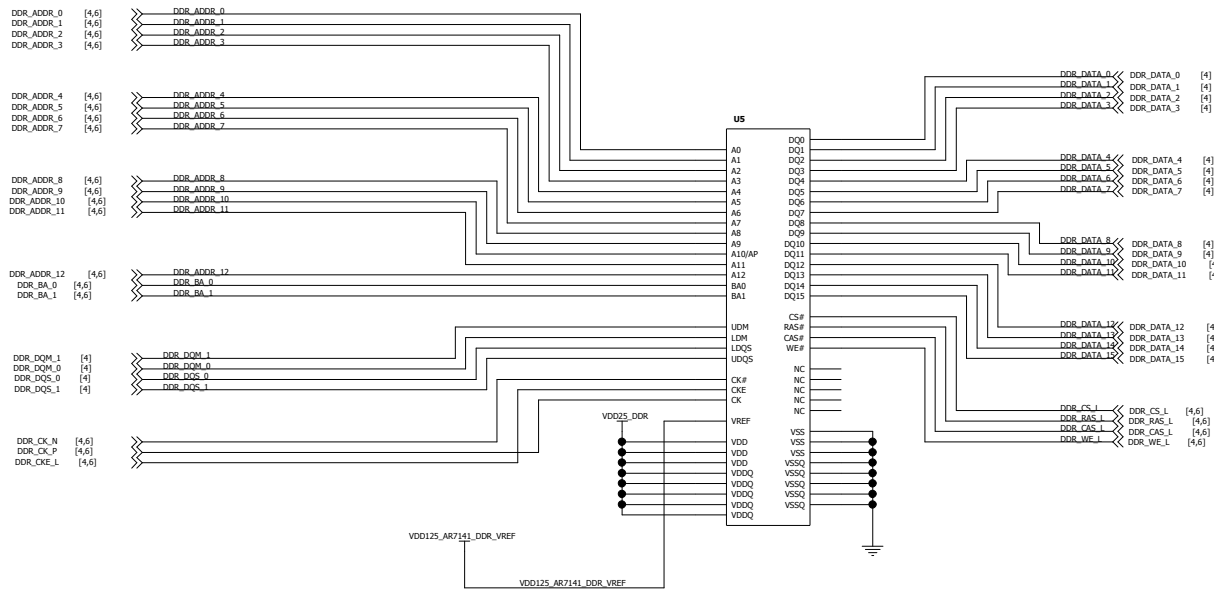


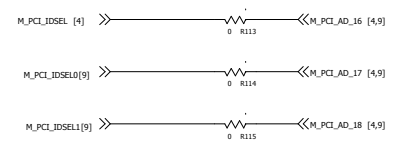
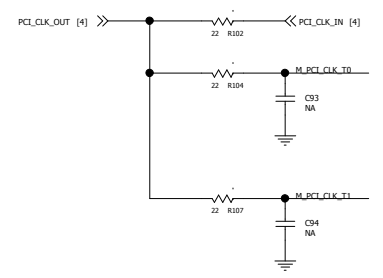
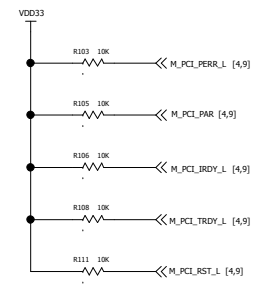
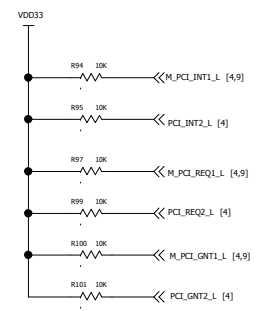
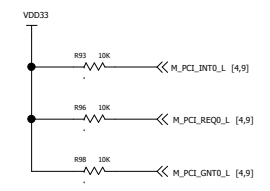
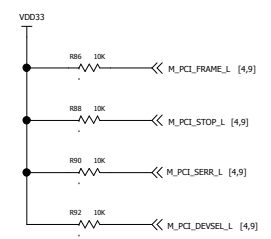
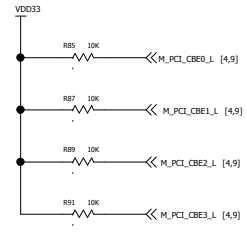
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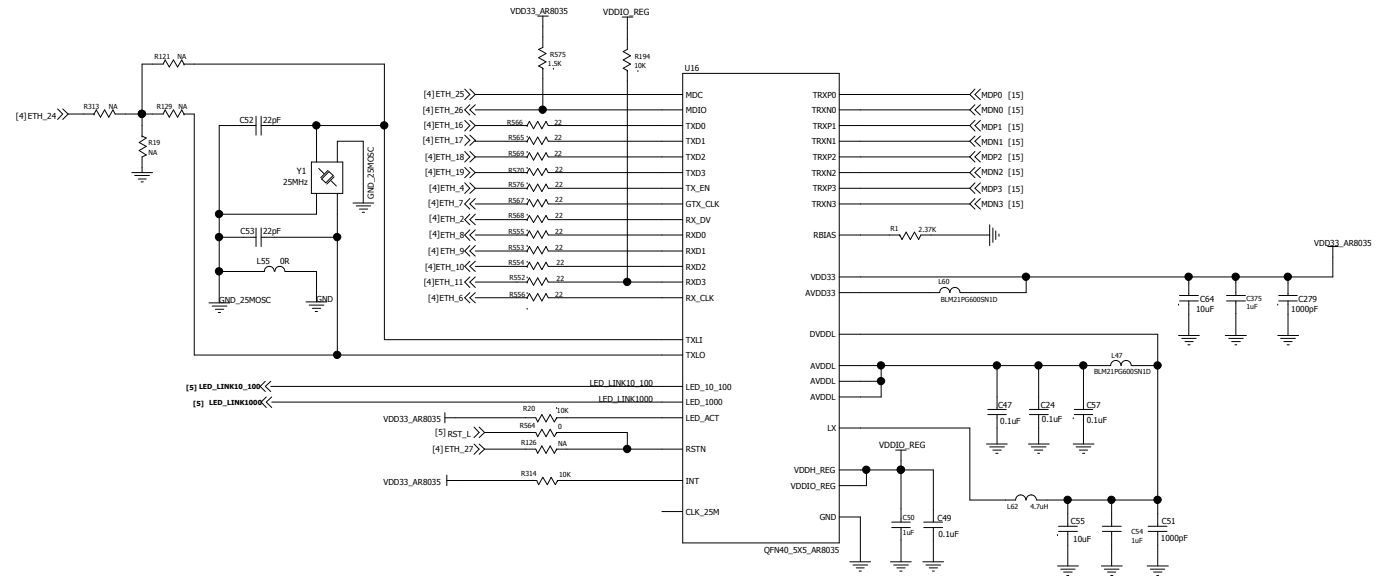


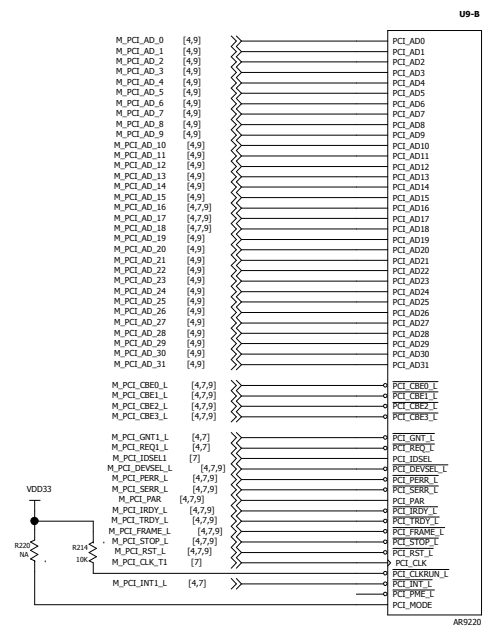
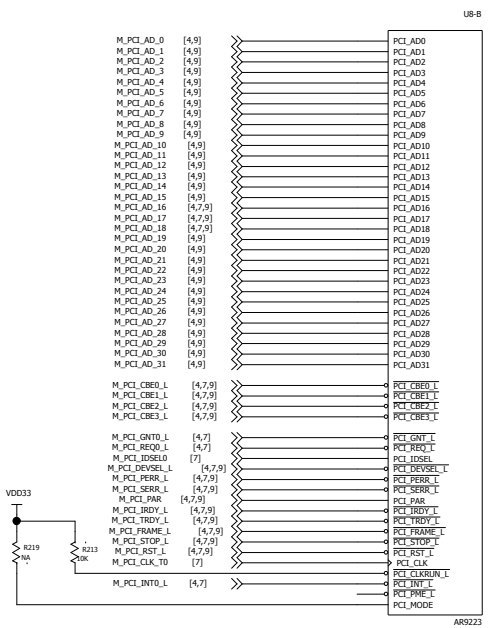
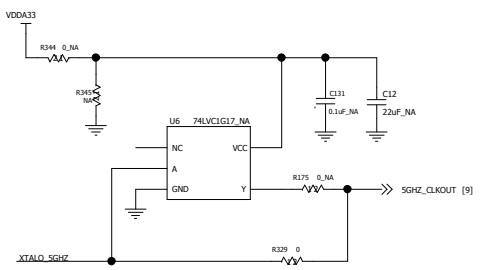
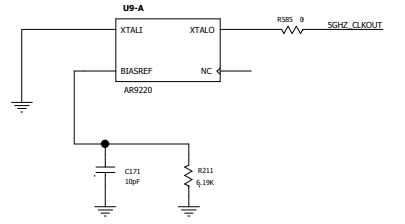
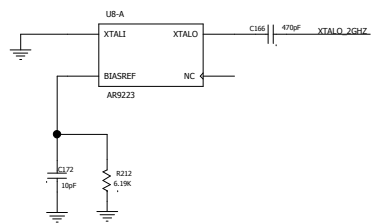
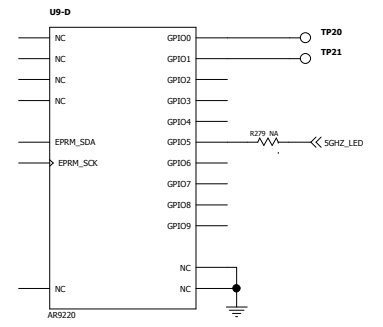
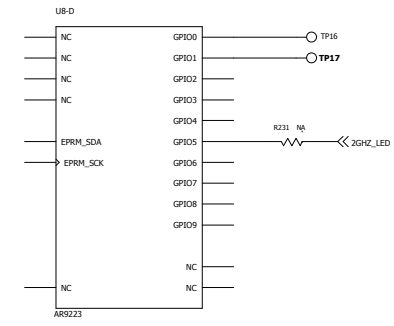
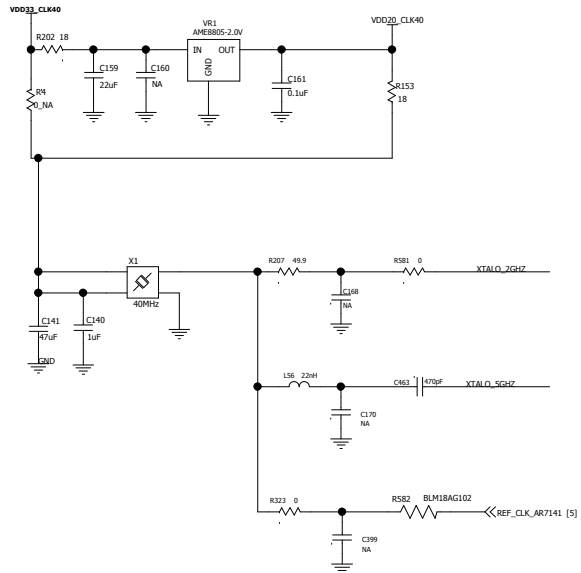
RESET SW





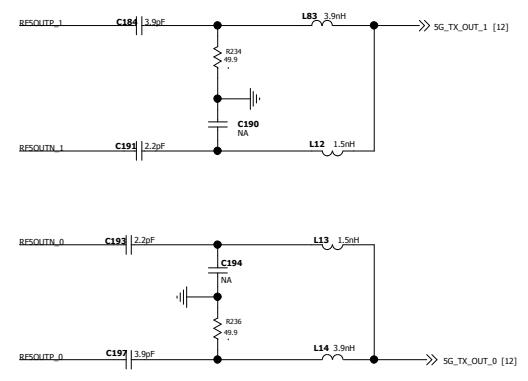
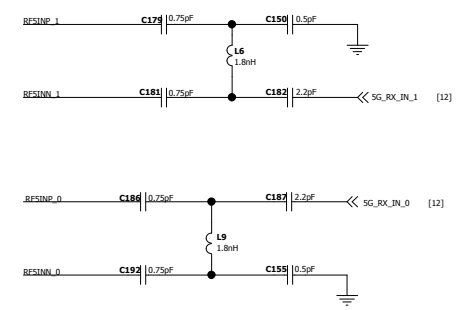
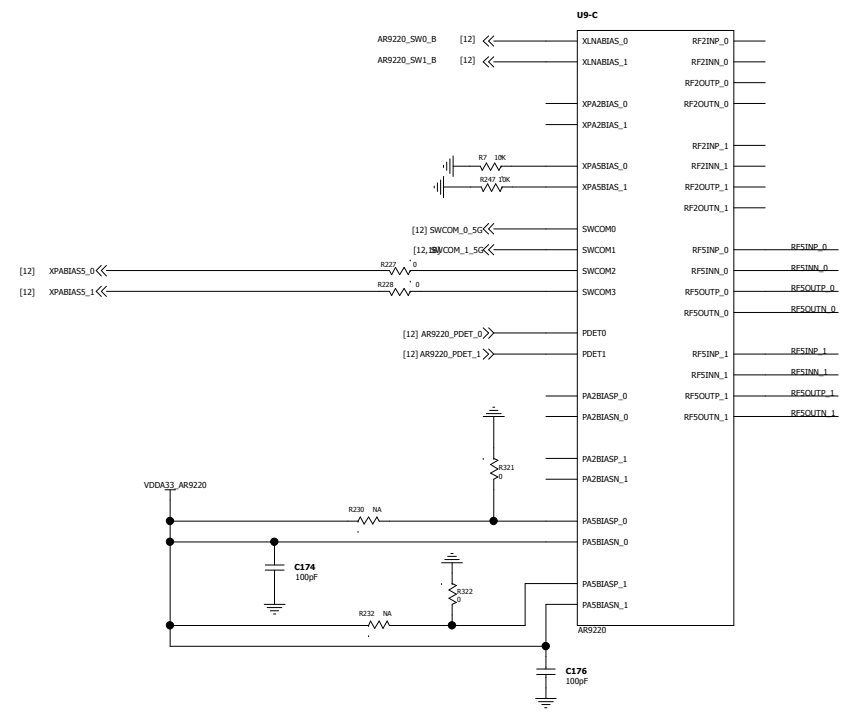
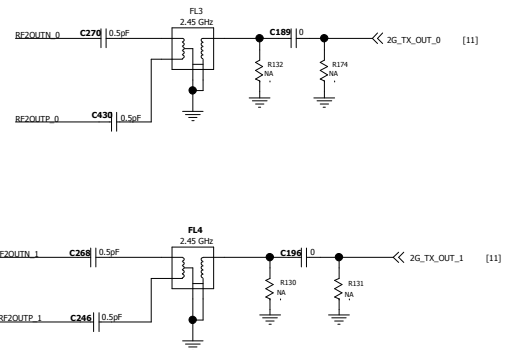
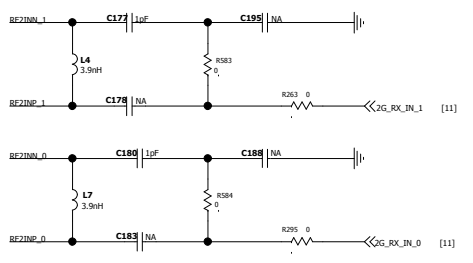
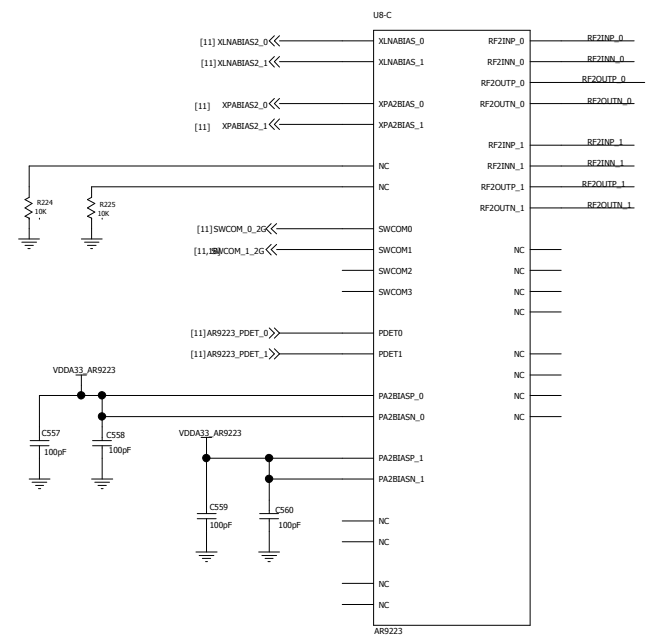


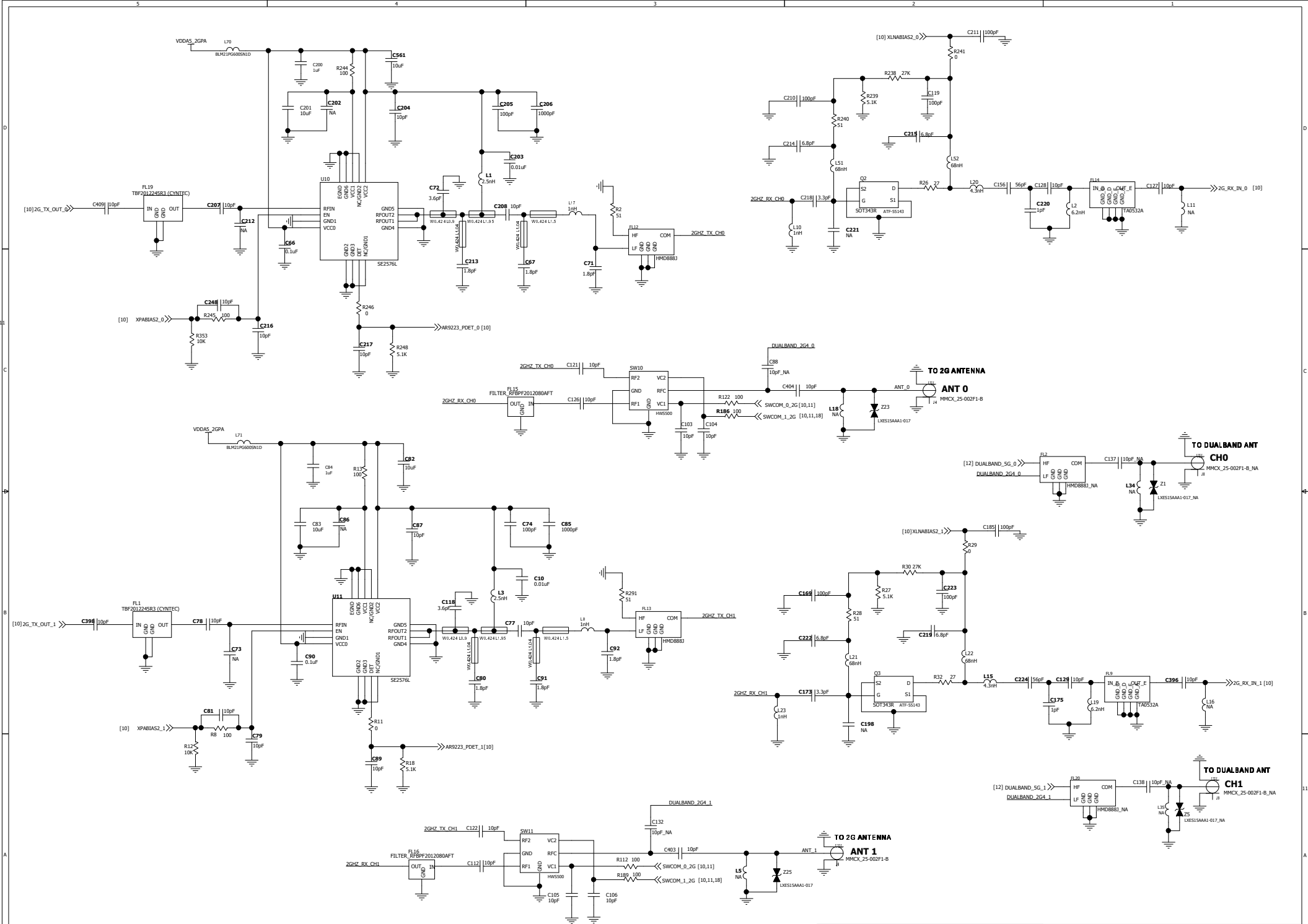




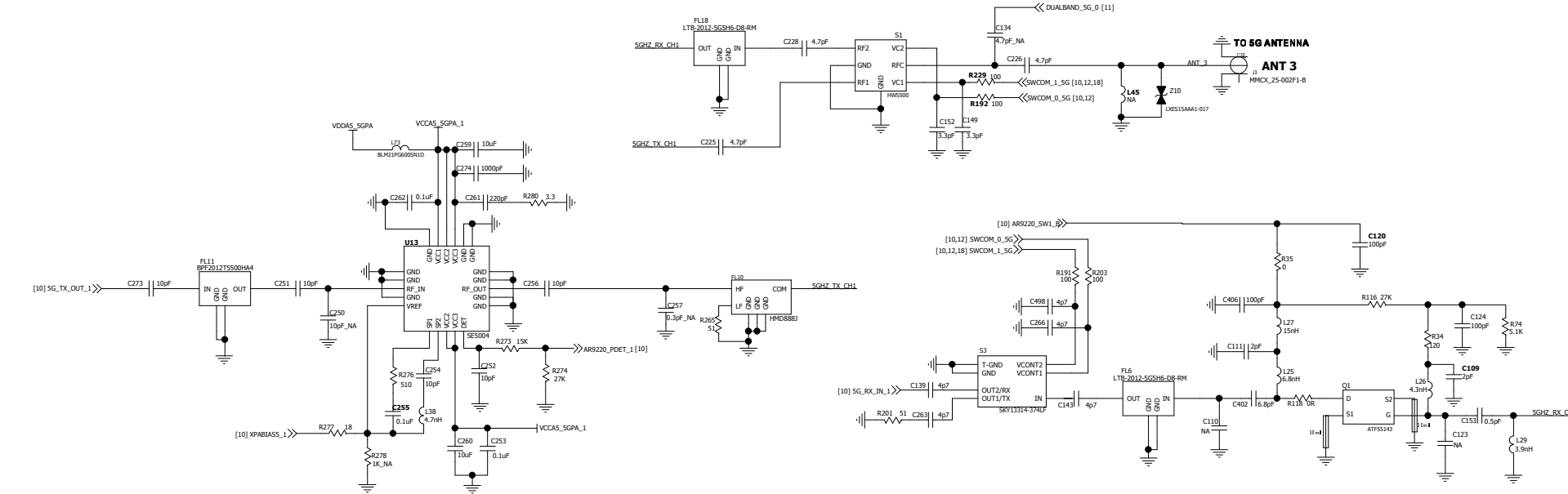
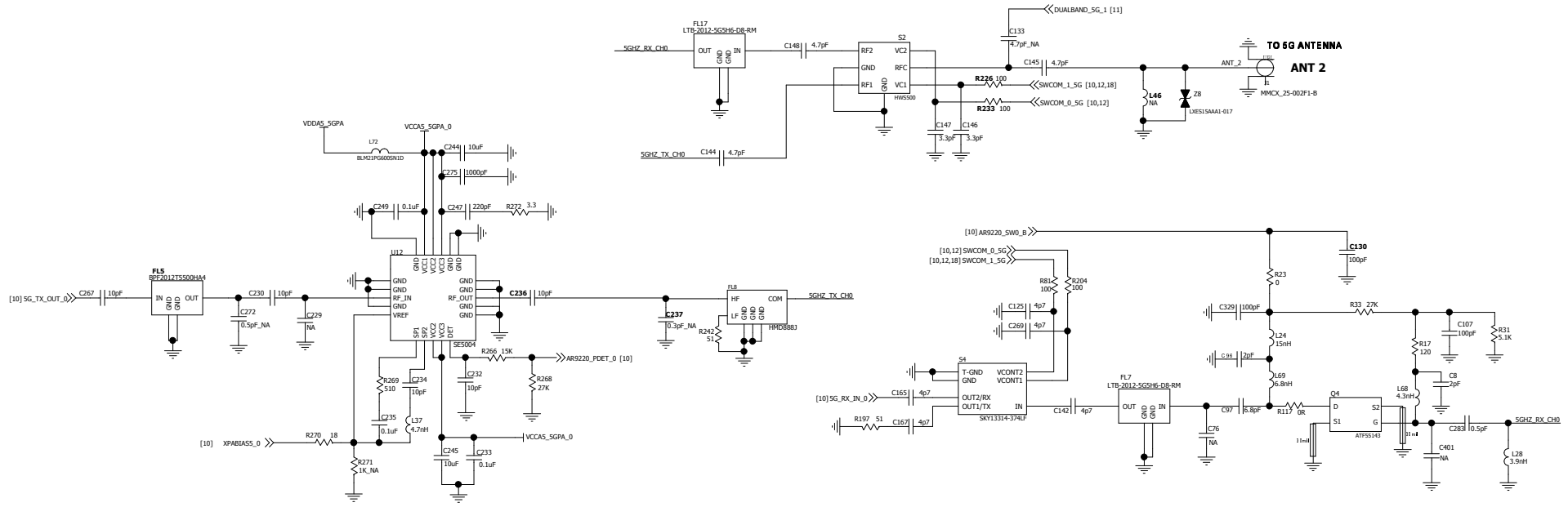
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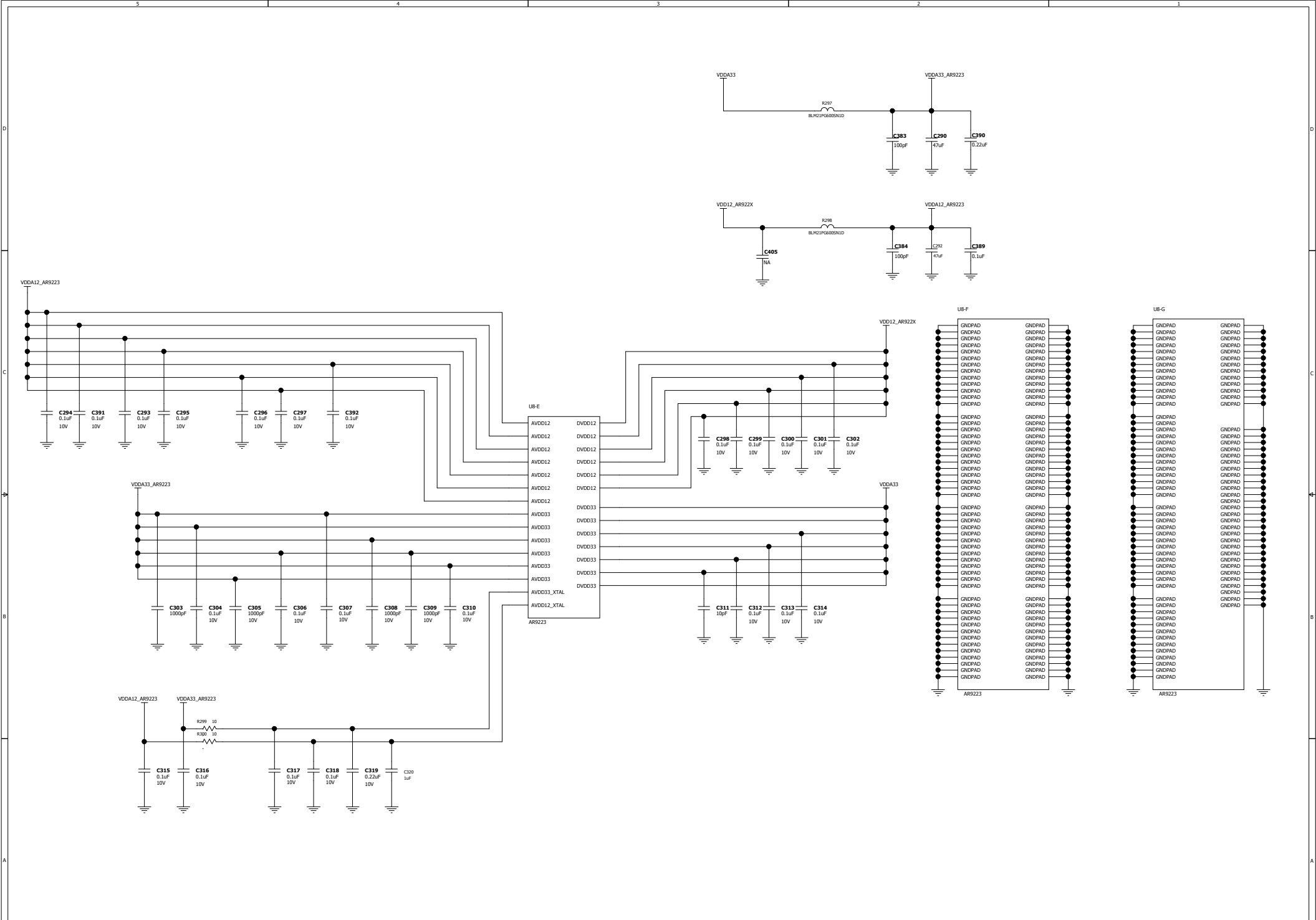
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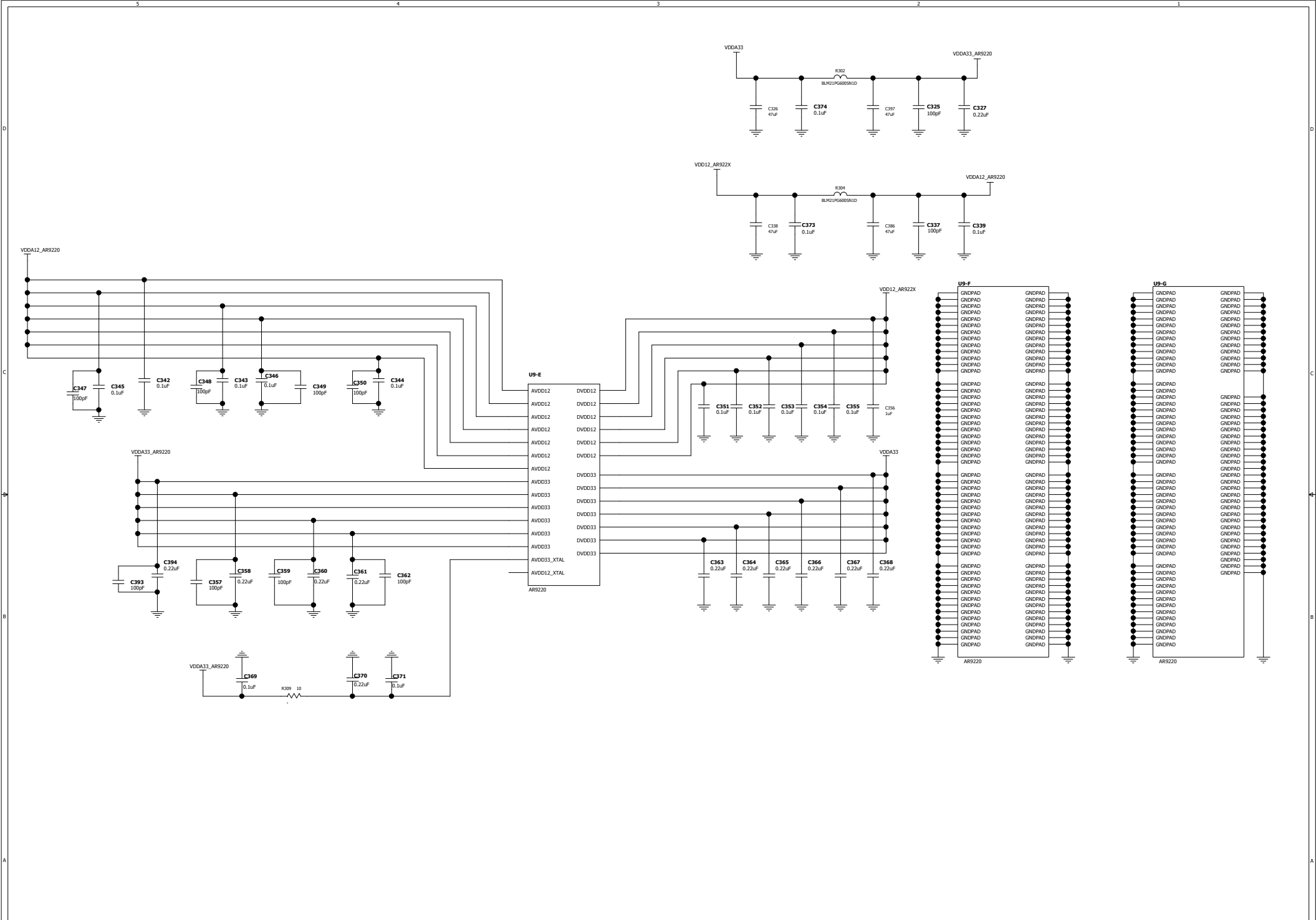


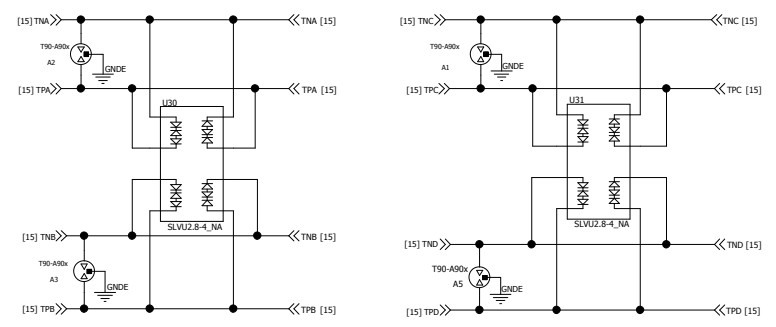
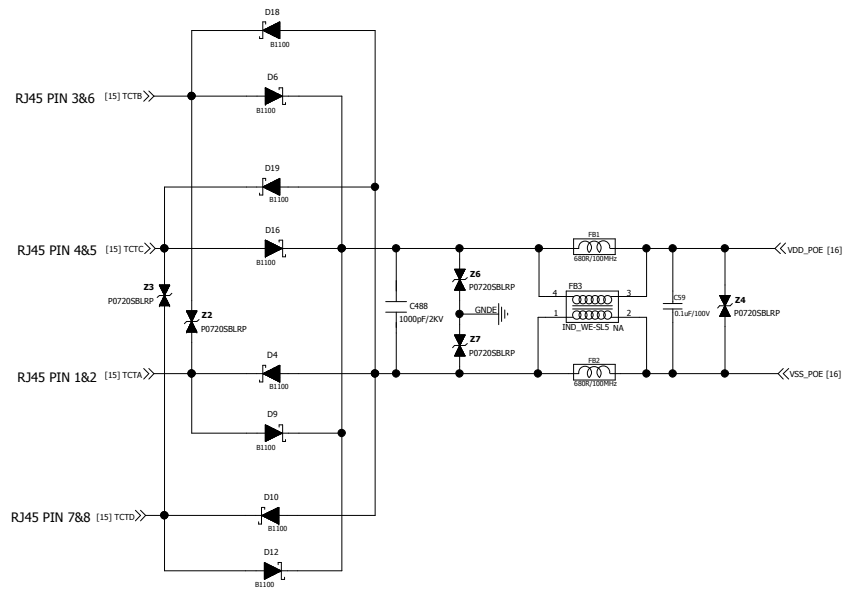
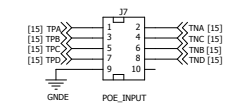
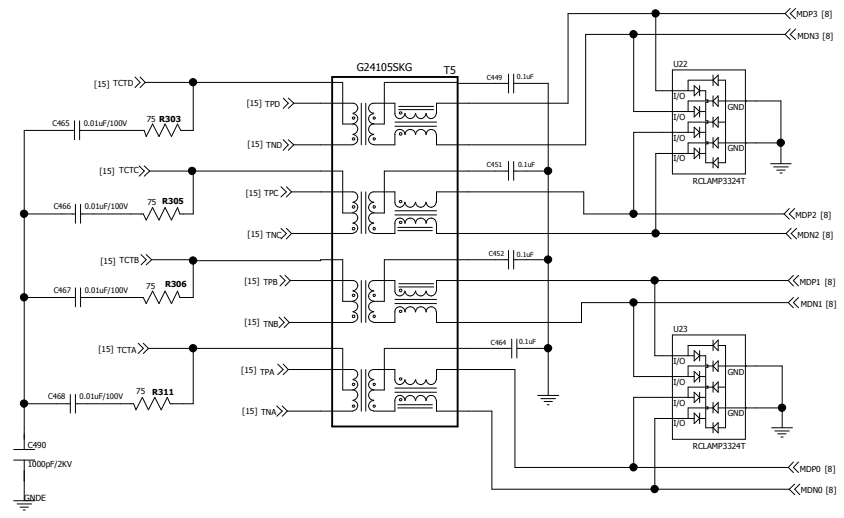


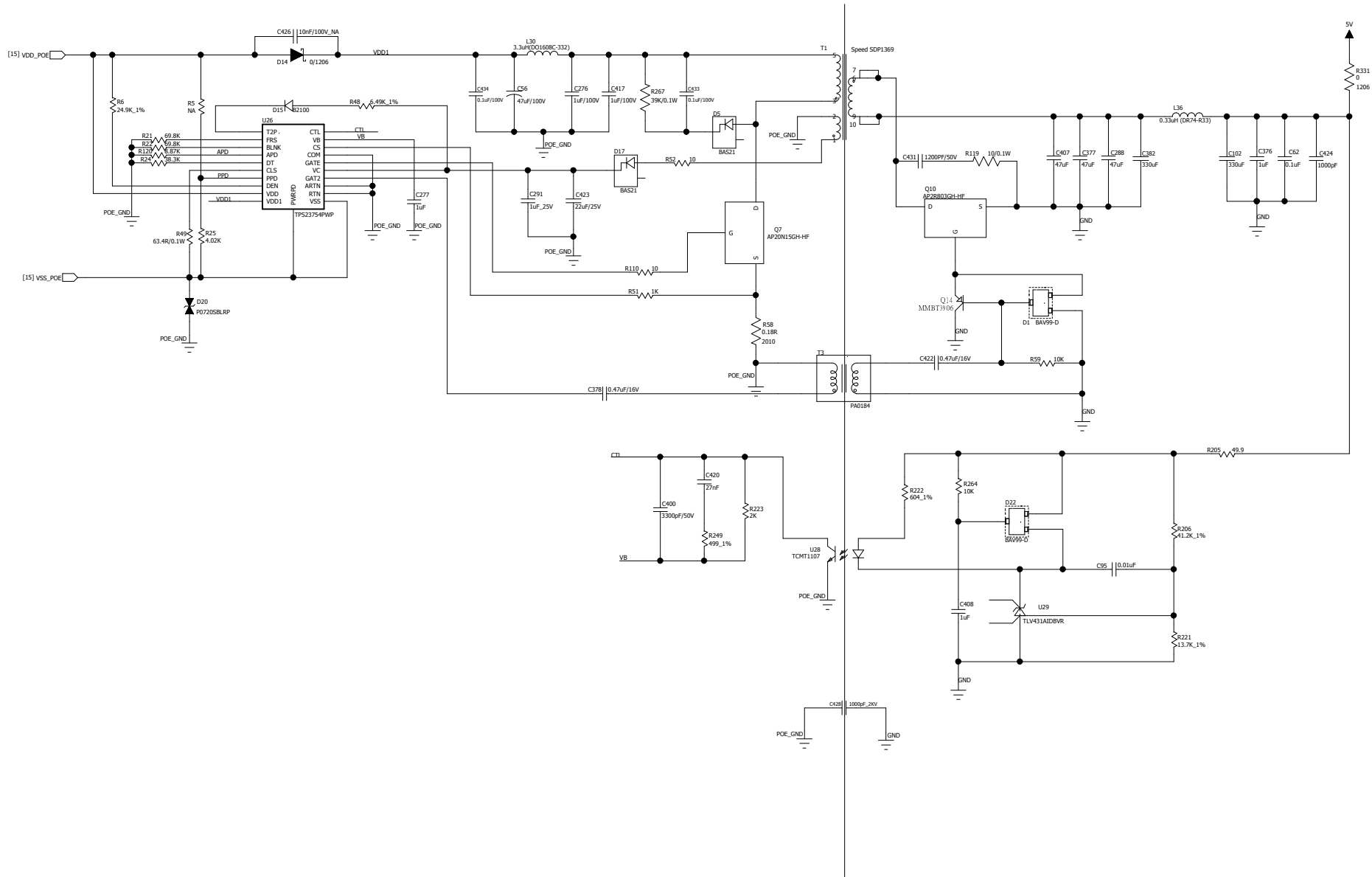
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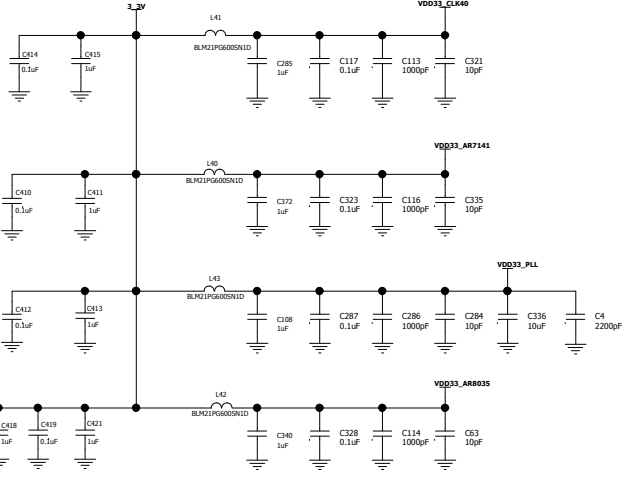
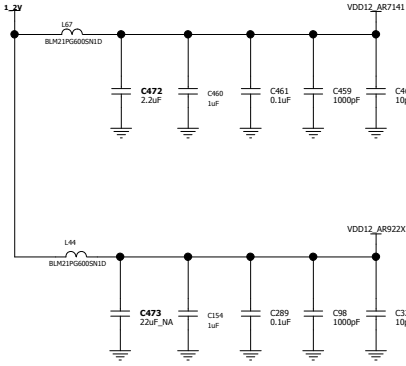
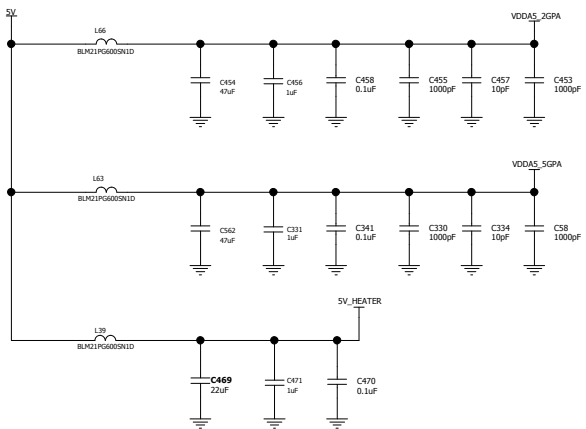
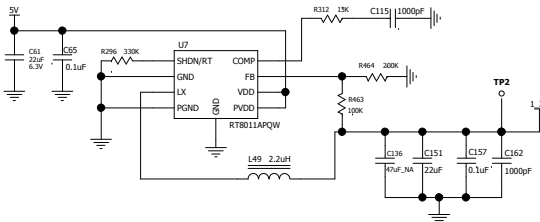
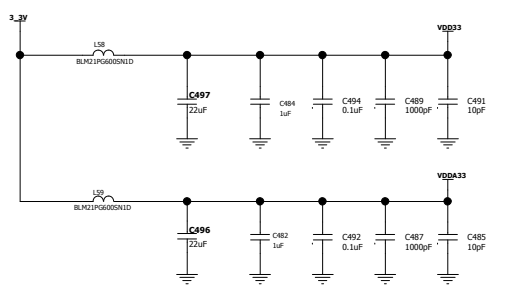
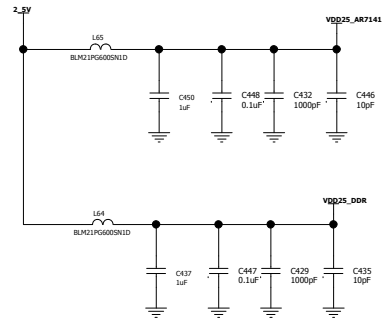
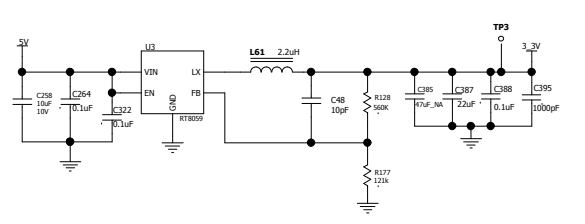
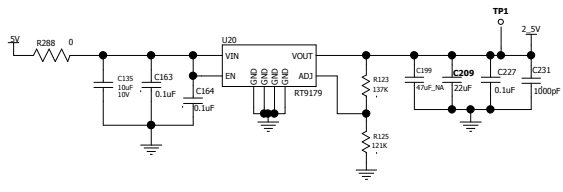
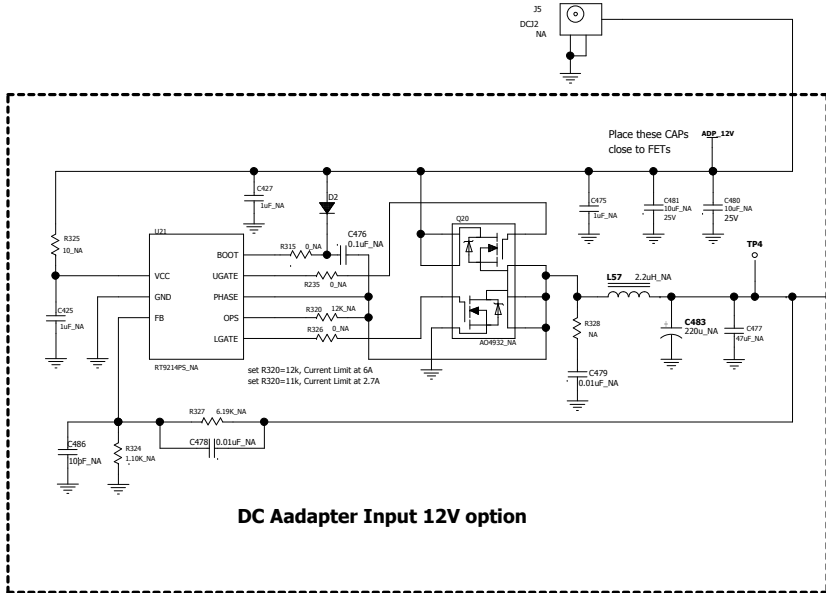












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