Marvell Semiconductor

Kinoma Element

Hardware Technical Reference Manual

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Kinoma Element Hardware Technical Reference Manual

This document describe Kinoma Element Board circuit functions.

Photo of Kinoma Element PCB

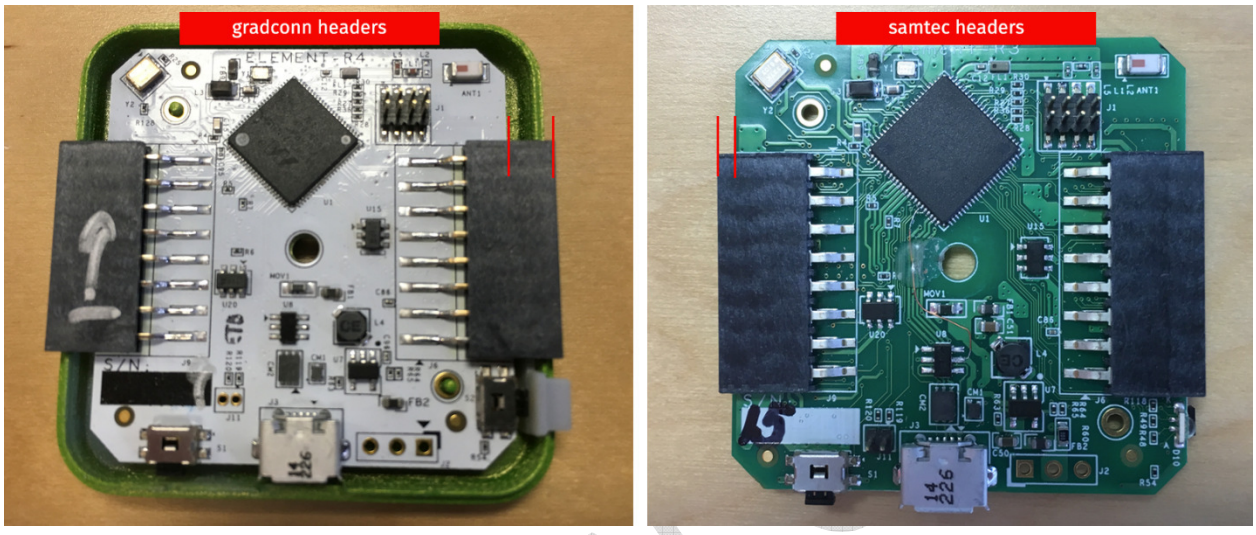

Figure 1 Element PCB assembly

Block Diagram

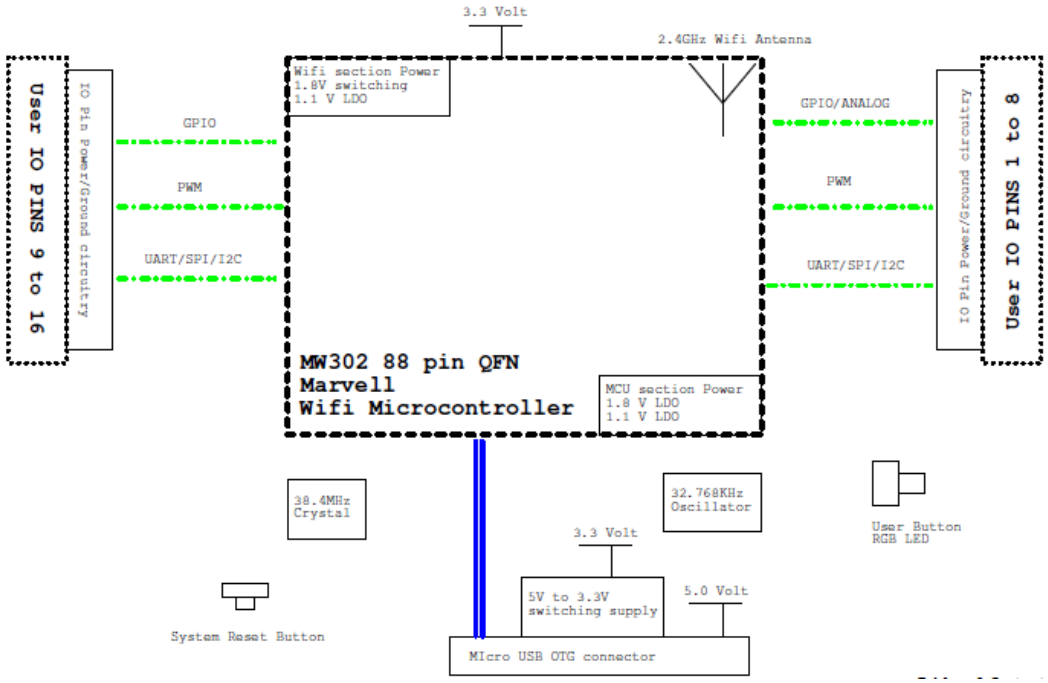

Figure 2 Element Block Diagram

Power supply architecture

Element power supply has two main sections, system wide input from either micro USB connector or from dedicated J2 pins. Both inputs are tied together and feed on board 3.3 volt supply.

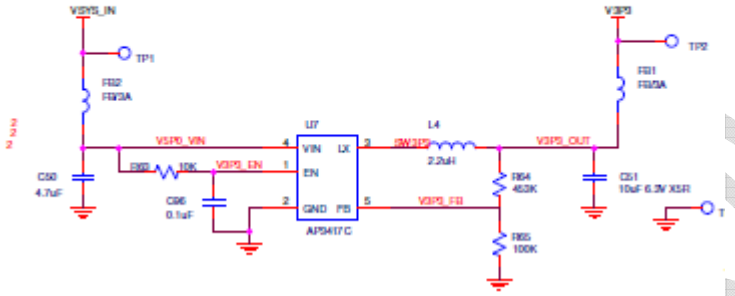

Figure 3 on board 5 volt to 3.3 volt switching supply

On chip power regulators

MW302 contains on-chip power supplies for 1.8 volt and 1.1 volt. There are two sets of on chip power supplies, one for microcontroller part and another for wifi part. The 1.8 volt supply for wifi part is a switching supply controller utilizes L3. All other supplies are low drop out regulators that require output capacitor only.

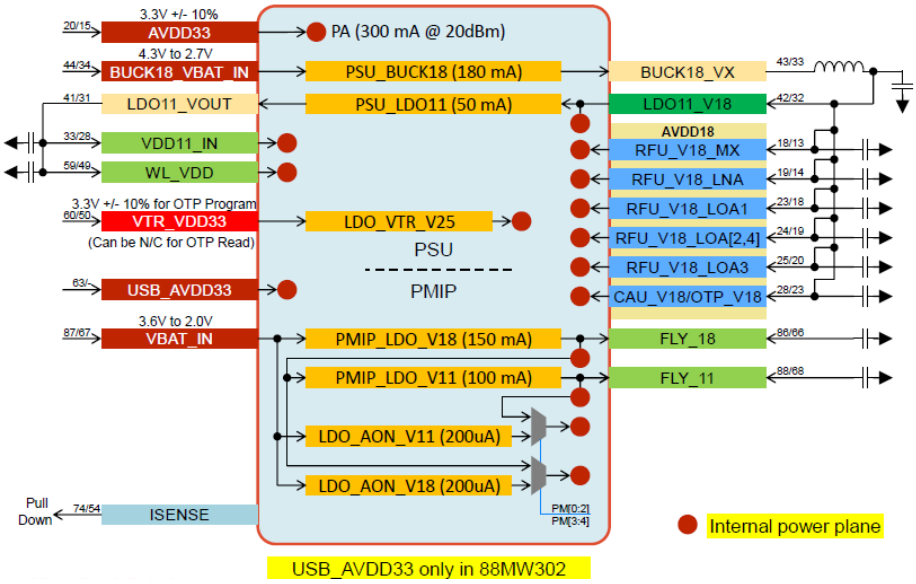

Figure 4 MW302 on chip power supplies

IO power

Element use 3.3 volt IO power for all signals including QSPI flash and sleep clock.

Reference clocks

System wide clock is derived from Y1 38.4 megahertz crystal. For the mw302 power management, a sleep clock oscillator Y2 runs at 32.768 Kilohertz.

Reset

MW302 chip has on chip power on reset circuitry. It is also connected to a reset push button S1.

User Button

A user definable button S2 and RGB color LED D10 is provided on one side of element.

Micro USB OTG port

The USB OTG port can be used to power the device, connect to a PC as USB-CDC device, and connect to a USB device such as flash-drive and USB web cam

User connectors

There are sixteen user IO connections, eight on each side of element. Every pin can be configured as

1. Digital GPIO
2. 3.3 volt Power supply pin
3. Ground pin
4. Pins on the Right hand side (where push button and LED locate) are also capable of analog input
5. Some pins carry serial ports such as UART, I2C and SPI.
6. Pins on the right hand side can be used as General Purpose timers or Pulse width modulated outputs.

Power/Ground circuitry for User IO pins

To provide power or ground to every pin, the element utilizes external logic control and small power mosfets as shown below schematic sections. Every user IO pin has a P-channel mosfet transistor to connect to 3.3 volt power rail and an N-channel mosfet transistor to connect to ground reference. Signal PIN1 is connected to connector PIN1.

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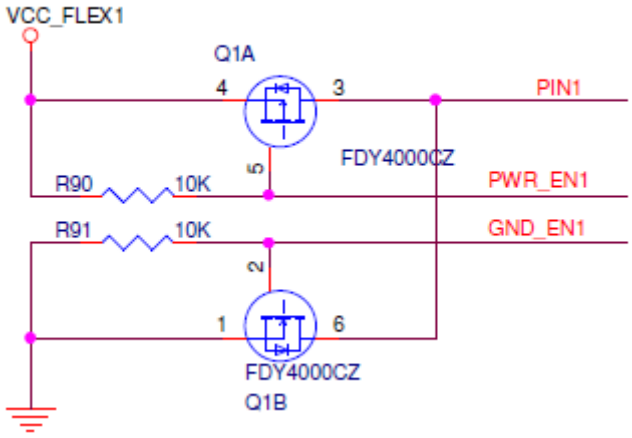

Figure 5 P and N channel mosfets

Each mosfet gate is driven by the serial in parallel out shift registers with separate output latch. Output latches are requires so there will be no spurious switching while shifting out settings serially. There are two shift register chips, each has eight outputs, controls four of eight pins each. For each shift register four outputs controls p-channel mosfet transistors and other four controls n-channel mosfet transistors.

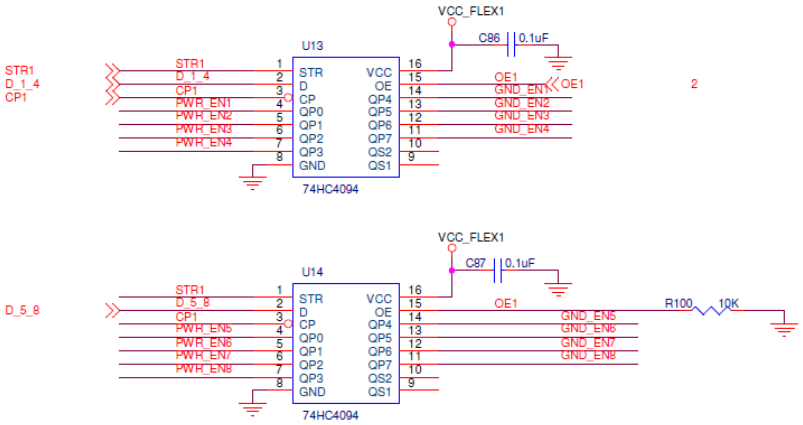

Figure 6 serial in-parallel out shift registers

Setting parallel output signal (PWR_EN1 shown in Figure 3) connected to p-channel mosfet gate to logic HIGH will turn OFF the transistor, setting PWR_EN1 logic LOW will turn the p-channel mosfet transistor ON, connecting IO pins to 3.3 volt power. Similarly, but of opposite logic states, setting logic LOW to parallel outputs of shift register connected to N-channel mosfet transistor gate (GND_EN1 shown in figure 3) will turn the transistor OFF and setting GND_EN1 to HIGH will turn the transistor ON.

Software ensures that both P-channel and N-channel mosfet transistors will NEVER on simultaneously to avoid power to ground low resistance path through transistors.

Boot process

The mw302 boots as soon as power is applied and power on reset released. First instruction is fetched from on chip boot ROM. Boot rom will determine secondary boot source. Element board is configured to boot from a QSPI flash chip. First part of SPI chip has the secondary boot code known as boot2. Boot2 will further fetch microcontroller firmware and wifi firmware from appropriate locations in the flash device.

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Appendix A user pin to mw302 GPIO map

Element Pin No	GPIO	Feature	UART	SPI	I2C	GPT(PWM)	OTHER
1	42	ADC0 0		SSP1 CLK			KP DKIN0
2	43	ADC0 1		SSP1 FRM			KP DKIN1
3	44	ADC0 2	UART1 TX	SSP1 TXD			KP DKIN2
4	45	ADC0 3	UART1 RX	SSP1 RXD			KP DKIN3
5	46	ADC0 4		SSP2 CLK			KP DKIN4
6	47	ADC0 5		SSP2 FRM			KP DKIN5
7	48	ADC0 6	UART2 TX	SSP2 TXD			KP DKIN6
8	49	ADC0 7	UART2 RX	SSP2 RXD			KP DKIN7
9	0			SSP0 CLK		GPT0 CH0	KP MKIN4
10	1			SSP0 FRM		GPT0 CH1	KP MKIN5
11	2		UART0 TX	SSP0 TXD		GPT0 CH2	KP MKIN6
12	3		UART0 RX	SSP0 RXD		GPT0 CH3	KP MKO0
13	18			SSP1 CLK	I2C1 SDA	GPT3 CH1	KP MKO9
14	19			SSP1 FRM	I2C1 SCL	GPT3 CH2	KP MKO10
15	20			SSP1 TXD	I2C0 SDA	GPT3 CH3	KP MKO11
16	21			SSP1 RXD	I2C0 SCL	GPT3 CH4	KP MKO12

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Appendix C Extension power unit connections

A battery power pack can be added to the element board. It is required when USB port is connected to a device. A battery may be connected to J2. For devices which require proper power control switch, two GPIO signals are available on J11, power enable output and fault flag input.

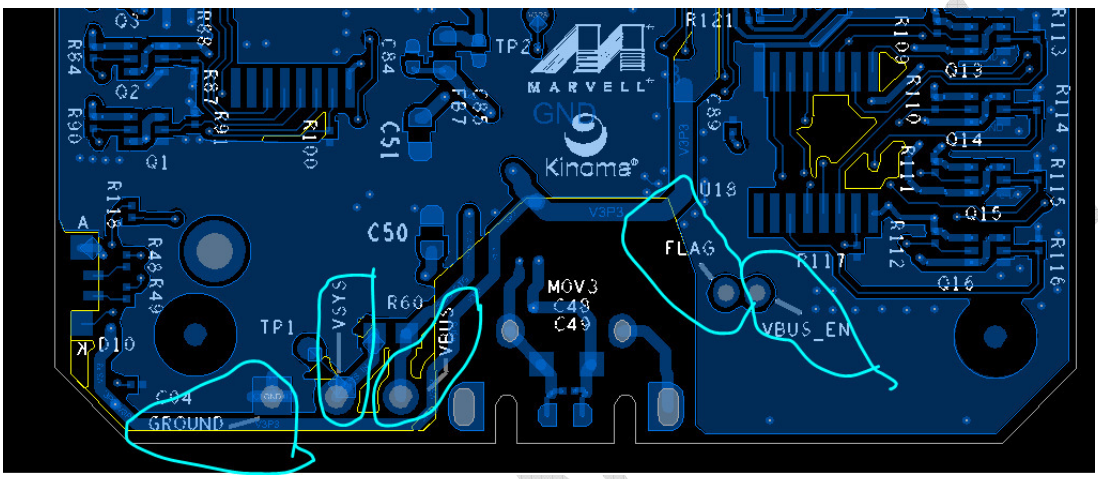

Figure 7 extension power connections

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Appendix D understanding user IO pins

IO pin power capacity

User may be connecting Element user IO pins to small sensors or devices such as LED signs. Every user IO pin is design to deliver 150 milliamps. Any device it would draw more than 150 milliamp should set multiple power AND ground pins.

Total system power budget

If user is connecting to a PC, USB hosts usually provide 5 volt 500 milliamps power. It would translate to about 600 milliamp on 3.3 volt Element board 3.3 volt power source. When using Wifi communication, especially transmitting, the wifi sub system may draw about <> milliamps. So it is important to connect Element to a sufficiently strong power supply if total power requirement is high.

Inductance of the wires

Ground wire also carries signal return current. Signal return current exist only when the output signal is transitioning from high to low or low to high.

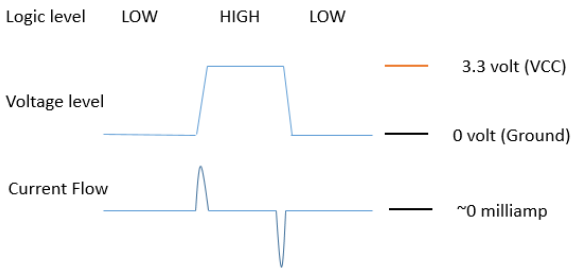

Figure 8 logic state change vs voltage current change

At that very short moment, the wire will act as inductor and create additional impedance proportionate to the rate of change of signal. It applies to outputs on both element and attached device. Use multiple ground wires and IO pins if the rate of change of signal is fast to have effectively lower inductance, for example SPI bus and high baud rate UART.

Stray capacitance on solderless breadboards

Solderless prototyping boards have stray capacitance. Stray capacitance is formed because of contacts form parallel metal plates along adjacent ‘rows’ of connections. The stray capacitance is more important for higher speed signals such as SPI and less concern about slow signals such as I2C.

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I2C bus

Multiple I2C bus devices can be connected to the same I2C BUS. I2C bus can operate only when ALL devices on the bus are powered, and every device has unique bus address. It is also important to calculate total pull up resistance. All pull up resistors between SDA or SCL to 3.3 Volt will form parallel resistance.

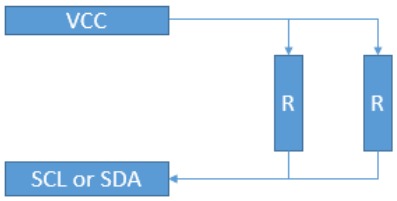

Figure 9 I2C bus pull up resistors in parallel

Total resistance can be calculates as below. There are many web sites offer web based parallel resistance calculations.

$$1/R_{total} = 1/R_1 + 1/R_2 \ldots 1/R_n$$

$$R_{total} = (R_1 * R_2 * \ldots Rn) / (R_1 + R_2 + \ldots R_n)$$

For example, if two i2c devices each has 10 kilo ohm pull up resistor on module would effectively create a 5 kilo ohm pull up for the bus. If 10 devices are connected it would become a 1 kilo ohm pull up.

When total pull up resistance gets smaller, it become stronger driving force towards logic HIGH on the SCL or SDA to a state that the IO driver may not be able to drive it to acceptable logic LOW level on all devices. General rule of thumb, TOTAL resistance should be larger than 3 kilo-ohms.

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Reference documents

1. Marvell semiconductor web site mw300 wifi-microcontroller specifications

http://www.marvell.com/microcontrollers/wi-fi-microcontroller-platform/

2. Kinoma Element Schematics

element-dvt-Nov30.pdf

3. Kinoma Element PCB design files

151441201FBRD.zip, 151441201FAB.zip, 151441201ASSY.zip

4. In-Circuit Tester Functional Specifications

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