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Date 24 July 2023

Federal Communications Commission
Equipment Authorisation Branch
7435 Oakland Mills Road
Columbia, MD 21046
United States of America
To whom it may concern

ANTENNA DESCRIPTION 13.56 MHz Card Reader - FCC ID: UAUWIRELESSCML

The 13.560 MHz Card Reader antenna design used within the UAUWIRELESSCML product is a PCB trace antenna that is inbuilt into the PCB board.

A reference document (see UM11232) supplying the technical information on the design used is attached with this description.

The reference design produces an inductance of 700nH, an impedance match of 50R with an EMC cut off frequency of 21 MHz.

Yours Faithfully

Hayden Burr
Chief Executive Officer.
Integrated Control Technology

UM11232

NFC Antenna Design Tool User Guide

Rev. 1.0 — 3 June 2019
547410

User manual
COMPANY PUBLIC

Document information

Information	Content
Keywords	NFC Antenna Design, NFC Reader IC, Antenna Matching, NFC Antenna Design Tool
Abstract	This document describes the usage of the NFC Antenna Design Tool that can extend or even replace the Excel file mentioned in the different application notes about the NFC antenna design.

Revision history

Revision history

Rev	Date	Description
1.0	20190603	Initial version

1 Introduction

The NFC Antenna Design tool supports the antenna coil synthesis based on some basic input parameters and calculates the matching circuit for the following NXP NFC Reader ICs: PN7462/PN7362/PN7360, PN5180, CLRC663/MFRC630/SLRC610, CLRC663 plus, PN7120, and PN7150.

The details of the antenna design should be checked in each IC application note as there are some considerations to take into account for each of them. Please check the Annex for further reference to this.

This document will limit its explanation to the tool usage and will not explain any other aspect of the NFC antenna design. For information on those aspects, please see the documents of the antenna design mentioned in the references.

2 Application overview

The values in the following figure are the default values for the application:

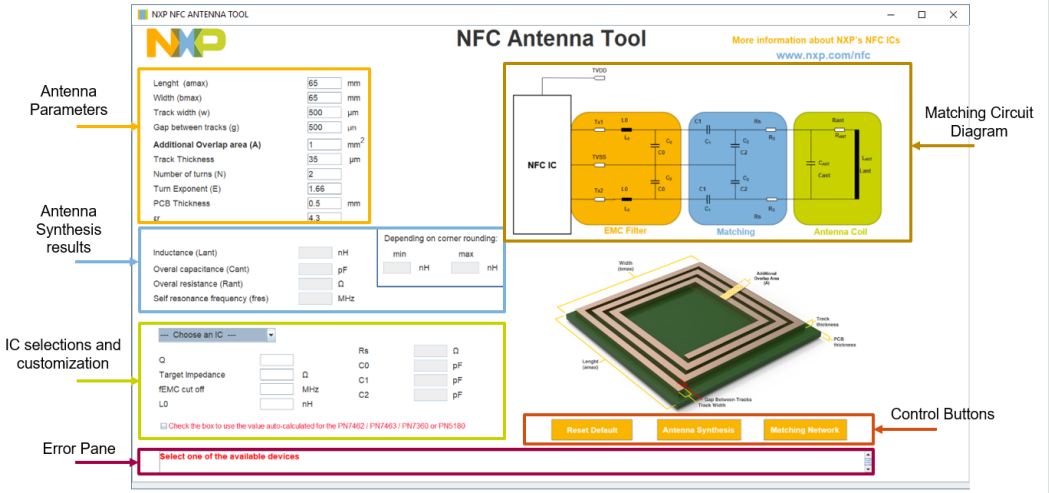

Figure 1. NFC Antenna Design Tool Interface

3 Using the tool

1. Open the location folder of the NFC Antenna Tool. Double click on the *AntennaTool.exe* file.

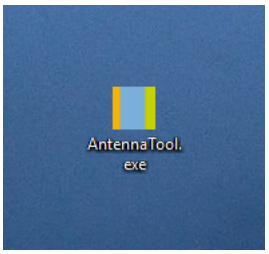

Figure 2. Antenna Tool executable file

2. Accept the license agreement for the tool usage.

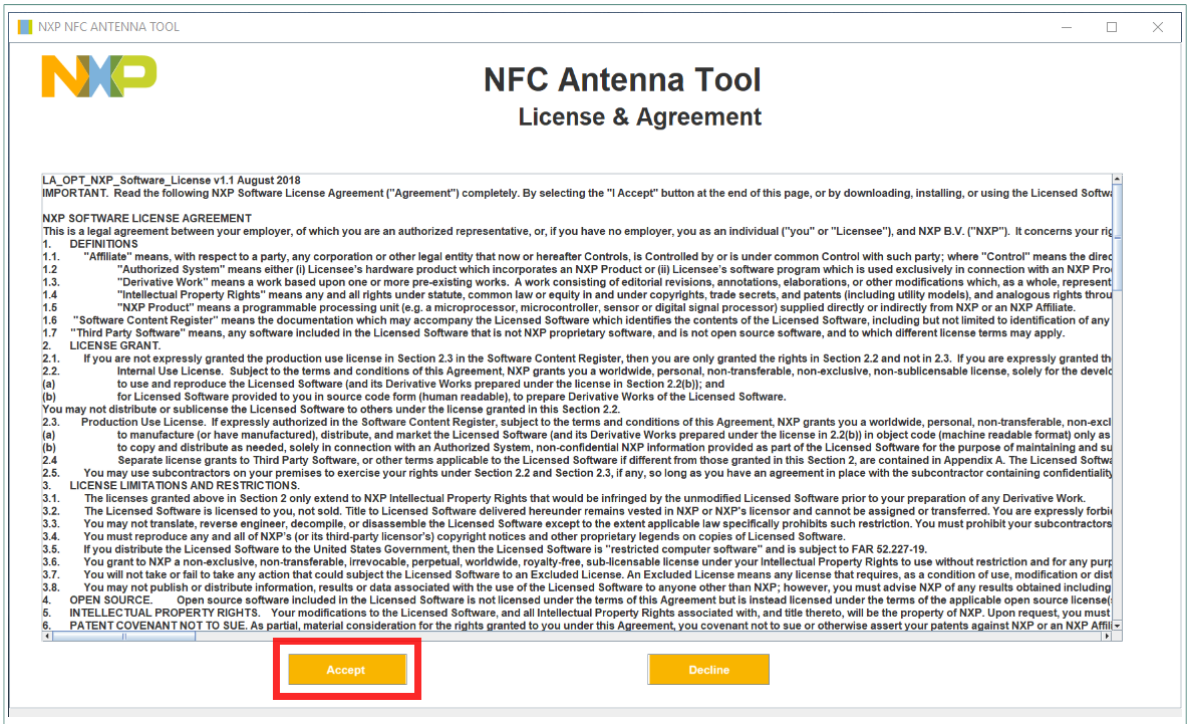

Figure 3. NFC Antenna Tool License and Agreement

3. The input for the antenna coil parameter fields must be a positive number. The tool does not accept any other character. In order to fill the antenna coil input parameters, it is important to follow the recommendations for each NXP NFC Reader IC.

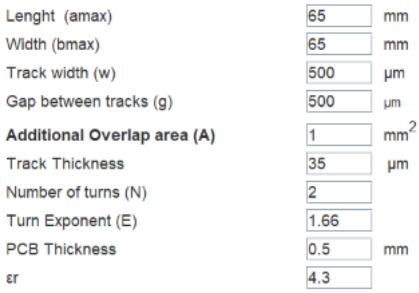

Figure 4. Antenna coil parameters

4. In order to obtain the results for each of the following points, click on the Antenna Synthesis button:
   - Inductance (Lant)
   - Overall capacitance (Cant)
   - Overall resistance (Rant)
   - Self-resonance frequency (fres)

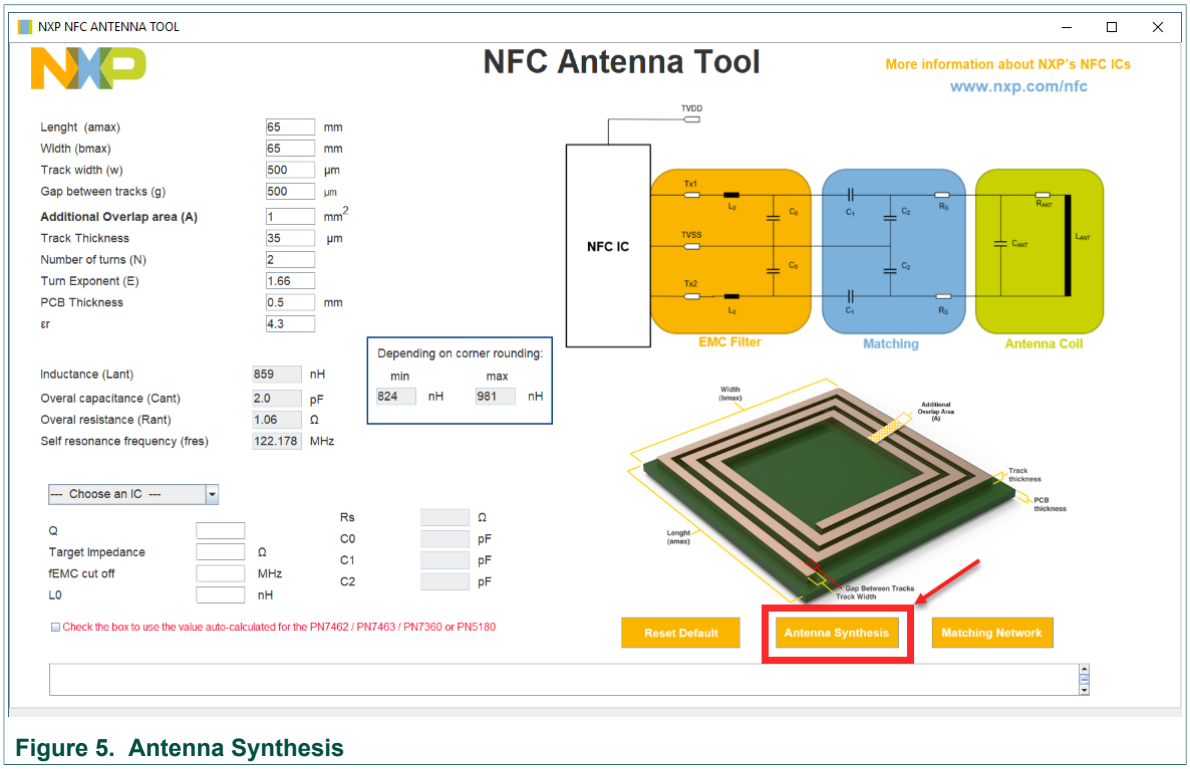

Figure 5. Antenna Synthesis

5. To get the matching circuit there are some input parameters to be defined by the user. It is recommended to choose one of the available NXP NFC Reader ICs in the list. For each of them the tool provides the NXP recommended input values, which give a good starting point. Any of the values can be modified at any time.
To get the recommended value of L0, there is a checkbox for the PN7462/PN7362/PN7360 and the PN5180. The L0 value will be calculated using the values from the synthesis, if checked. Otherwise, the user must enter a value.

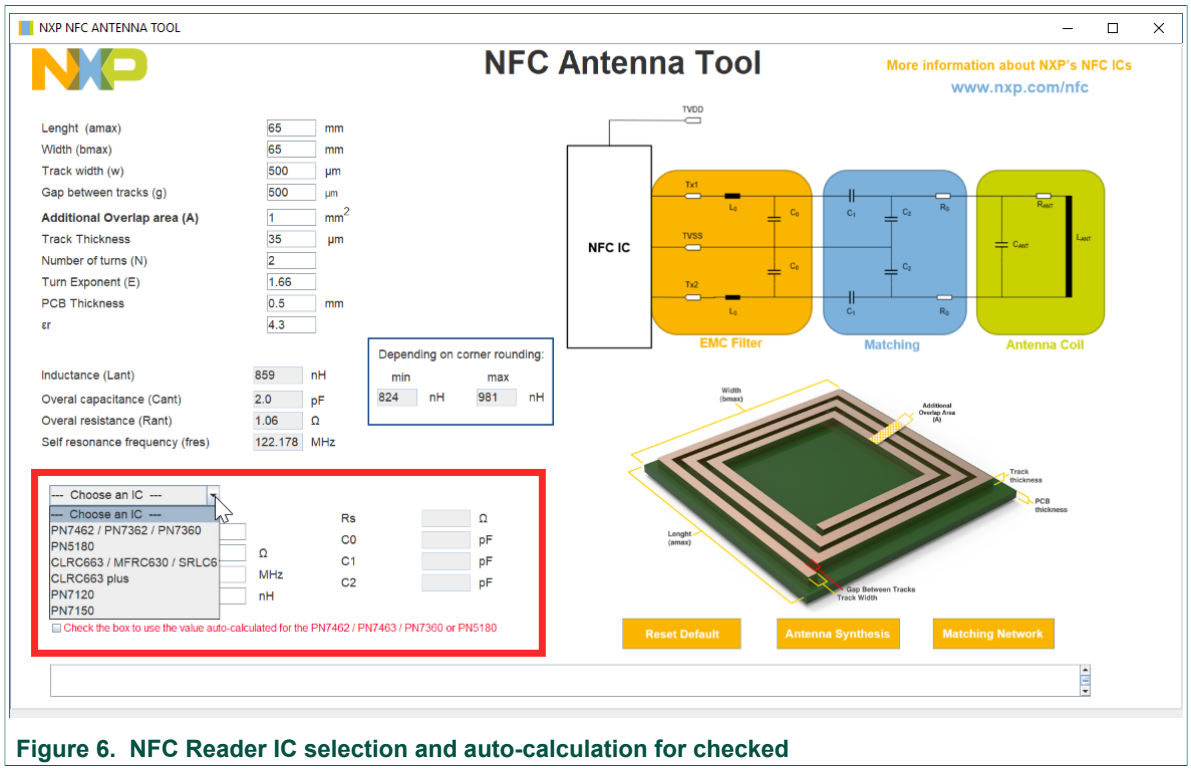

Figure 6. NFC Reader IC selection and auto-calculation for checked

6. In order to get the values for the tuning circuit, click on the Matching Network button.

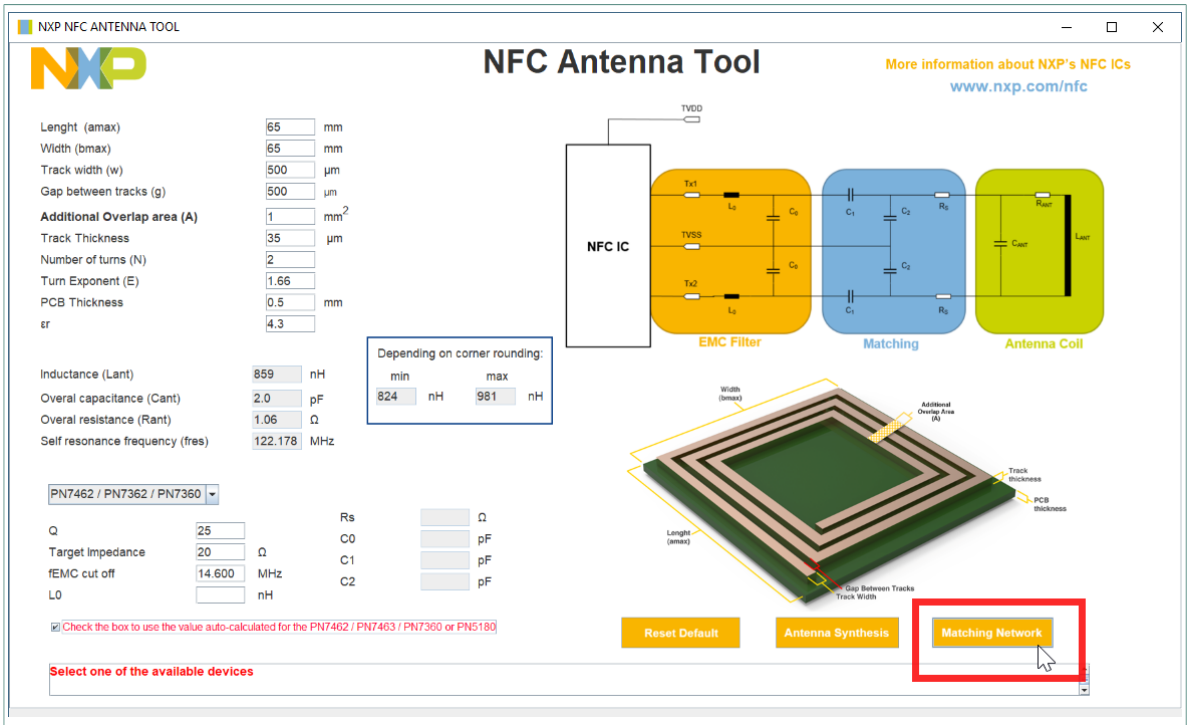

Figure 7. Matching Network for tuning circuit

7. If the button is clicked and there are no errors, the values will be shown in the circuit diagram.

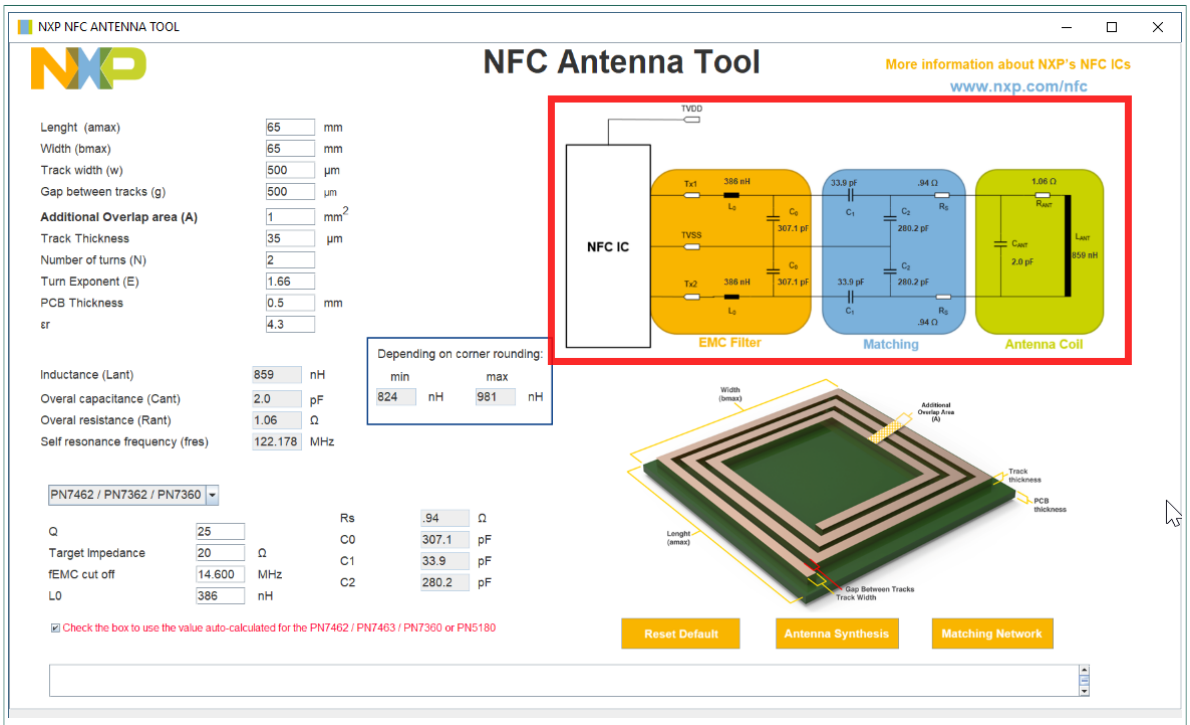

Figure 8. Circuit Diagram with antenna calculation

8. If the user wants to reset the default values and clean the design, there is one button to reset the tool to its default values.

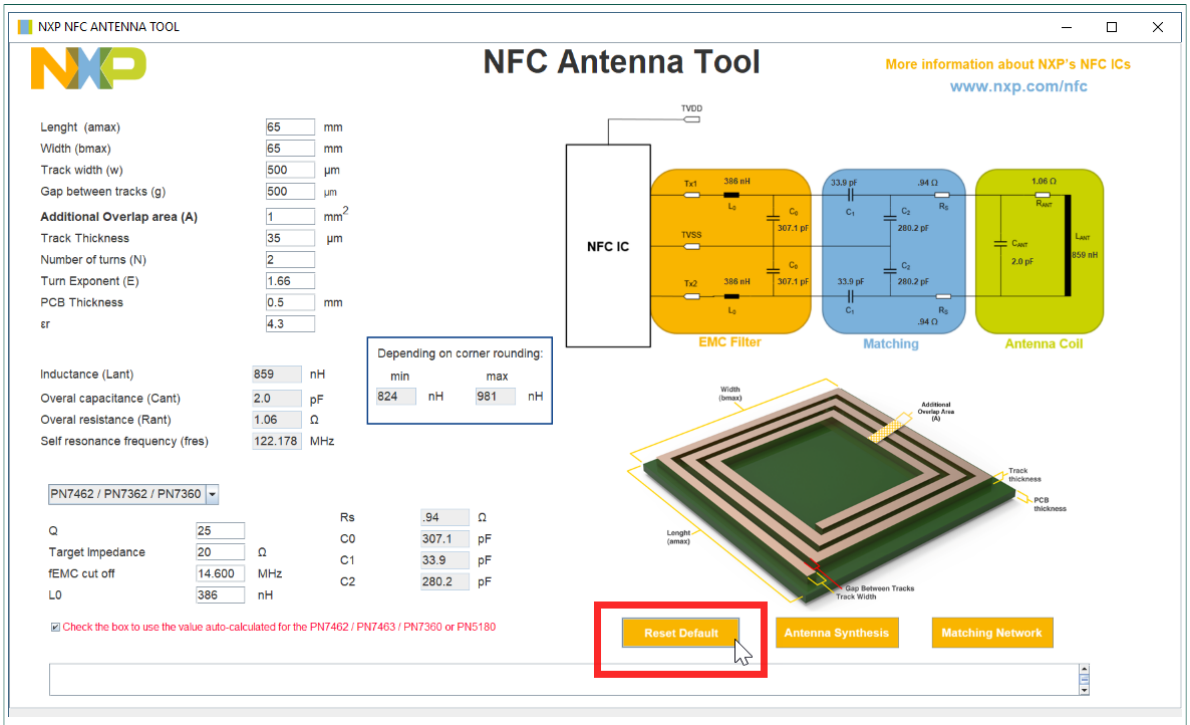

Figure 9. Reset values to default

4 References

- NFC Reader ICs:
  - PN7462
  - PN7362
  - PN5180
  - PN7120
  - PN7150
  - SLRC610 Plus
  - CLRC663 plus
- Antenna Design Guides:
  - PN7462 family Antenna design guide
  - CLRC663, MFRC630, MFRC631, SLRC610 Antenna Design Guide
  - PN7150 Antenna Design and Matching Guide
  - PN7120 Antenna Design and Matching Guide

5 Annex

Lists of parameters and abbreviations.

Table 1. Antenna synthesis input parameters

Abbreviation	Description
Length (amax)	The total length of the rectangular antenna coil. The antenna coil outlines are defined by length (amax) and width (bmax). The antenna coil size defines the operating distance. A typical length value is 50 … 100 mm.
Width (bmax)	The total width of the rectangular antenna coil. The antenna coil outlines are defined by length (amax) and width (bmax). The antenna coil size defines the operating distance. A typical width value is 50 … 100 mm.
Track width (w)	The track width of the antenna coil traces. The tracks should not be too narrow to avoid too high losses. On the other side, wider tracks shrink the average antenna area, which reduces the performance. A reasonable track width is 500 µm.
Gap between tracks (g)	The distance between the antenna coil traces. This gap should not be too small to avoid a too low self-resonance frequency. On the other side, wider gaps shrink the average antenna area, which reduces the performance. A reasonable gap width is 500 µm.
Additional overlap area (A)	The additional area, where additional traces cover the antenna coil traces using the other layer, e.g. if additional traces cross the antenna coil traces. Such additional overlap area then slightly changes the overall antenna behavior. ***Note:*** • *The "normal" overlap area, which is caused by the bridge from the inner trace to the outside (or vice versa) is automatically taken into account. If no additional traces are crossing the antenna traces, this value is 0.* • *A too large additional overlap area will reduce the performance of the antenna.*
Track thickness	The thickness of the copper layer of a PCB. A typical value is 35 µm.
Number of turns (N)	The number of turns should be adjusted in a way that a target inductance of the antenna coil about 1 µH is achieved. Smaller antennas have more turns than larger ones. A typical antenna of 65 mm x 65 mm has 2 turns. ***Note:*** • *Too many (resp. too less) turns increase (resp. decreases) the inductance too much, which causes some weird tuning parameters.* • *Too many turns can cause a low average area as well as a low self-resonance frequency.* • *The inductance of the antenna coil directly impacts the minimum EMC filter inductance for some NXP NFC Reader ICs.*
Turn Exponent (E)	The turn exponent defines the influence of additional turns. It depends on some environmental influences as well as the corner rounding. Typical values are 1.6 … 1.7. The Antenna tool shows a minimum and a maximum value of the estimated inductance, which indicates the possible variation, e.g. depending on corner rounding. ***Note:*** • *Extra metal influence is not taken into account at all.* • *The final inductance of the antenna coil as well as the tuning itself must be measured anyway to adjust the tuning.*
PCB Thickness	The PCB thickness influences the antenna coil via the (normal and additional) overlap area.
Epsilon r (εr)	The relative dielectric constant of the PCB. A typical value of FR4 material is 4.3.

Abbreviation	Description
Inductance (Lant)	The result of the antenna coil synthesis, based on the input fields. The target should be a value around 1 µH. This value is taken as input to calculate the tuning. ***Note:*** • *This synthesis is based on a simple model, and any extra metal influence is not taken into account at all. So, the real value might vary a bit, especially depending on the antenna environment. Especially metal environment close to the antenna coil might decrease the inductance value.* • *The final inductance of the antenna coil as well as the tuning itself must be measured anyway to adjust the tuning.*
Overall capacitance (Cant)	The result of the capacitance of the antenna coil, estimated based on the input fields. This capacitance should be as low as possible. The capacitance value might be higher than calculated, since the antenna synthesis does not take any additional traces into account and assumes an ideal environment. This capacitance value is taken as input to calculate the tuning.
Overall resistance (Rant)	The losses of the antenna coil, given as resistance value. This loss is taken as input to calculate the tuning, and it must be low enough to allow a damping resistor (Rs) > 0 to achieve a realistic tuning. The resistance value in reality might be higher than calculated, since the antenna synthesis does not take any additional traces in to account. Additional connection losses or losses due to metal environment are ignored in this calculation.
Self-resonance frequency (fres)	The self-resonance frequency is just shown as a reference value. The lower this value, the more critical the tuning might become. In any case it must be >30 MHz to allow a proper and stable tuning. A typical theoretical value is above 100 MHz.

Table 2. Antenna tuning input parameters

Abbreviation	Description
NXP NFC Reader IC choice	Based on the NXP NFC Reader IC choice some basic antenna tuning input parameters are set automatically: Q, Target impedance, and cut-off frequency. Any of the values can be manually modified, if needed.
Q-factor (Q)	The antenna q-factor (requirement) depends on the type of tuning and might vary a lot. Typical values are 15…25, when an NXP NFC Reader IC is chosen. It might be helpful to slightly modify this value a bit to achieve a reasonable value (E-series!) for the damping resistor Rs. **Example:** The tool might calculate Rs = 0.94 Ω, based on Q = 25. Then it makes sense to change the Q = 24 to get Rs = 1 Ω.
Target impedance	The target impedance defines the RF power. The typical, nominal value is chosen automatically together with the NXP NFC Reader IC. A higher impedance (to reduce the power consumption) can always be chosen, but that normally reduces the performance, too.
fEMC cut off	The cut-off frequency of the EMC filter defines the type of tuning (“asymmetrical” or “symmetrical” tuning). The choice of an NXP NFC Reader IC automatically defines this frequency. In any case, this frequency should be in the range of 14.5 … 21 MHz.
L0	The EMC filter inductor value. This value can be determined automatically in combination with the used NFC Reader IC and the antenna synthesis, if the checkbox is selected: In case of a DPC tuning the minimum recommended value for the L0 is calculated automatically. It might make sense to manually set this value to the next available real inductor value (E-series!). **Example:** The Antenna tool calculates 386 nH, and the real choice might be 390 nH. This inductor is a critical component in the overall tuning. It must be able to drive the full power level without saturation effects, and it must provide the highest possible Q-factor.

Table 3. Antenna tuning results

Abbreviation	Description
Rs:	The damping resistor reduces the Q-factor to the required value. This is important to ensure the required bandwidth. It is important to choose a resistor, which can survive the proper power level. It might make sense to place two resistors (double the resistance value) in parallel to cover the required power level.
C0:	The C0 defines the cut-off frequency (in combination with L0). Together with L0 it must be placed as close to the NXP NFC Reader IC as possible to keep the radiation of unwanted harmonics as low as possible. It might make sense to provide two capacitors in parallel for each C0 to be able to achieve the required value. Consider the voltage rating!
C1:	The serial capacitance should not get < 15 … 20 pF, otherwise the overall performance might be reduced. The tolerances must be considered! It might make sense to provide two capacitors for each C1 in parallel to be able to achieve the required value. Consider the voltage rating!
C2:	The parallel capacitance normally is in the range of > 100 pF. The overall tuning gets unreliable, if the C2 < 50 pF. The tolerances must be taken into consideration! It might make sense to provide two capacitors for each C2 in parallel to be able to achieve the required value. Consider the voltage rating!

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Tables

Figures

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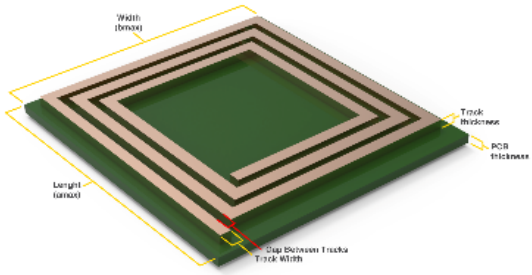
Date of release: 3 June 2019
Document identifier: UM11232
Document number: 547410

Readers

DOWNLOAD DATA

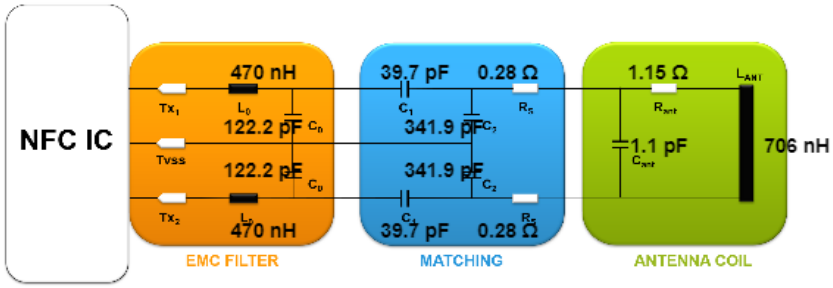
Length (amax)	33	mm
Width (bmax)	27	mm
Track width (w)	200	µm
Gap between tracks (g)	400	µm
Additional Overlap Area (A)	0	mm²
Track Thickness	35	µm
Number of Turns (N)	3	
Turn exponent (E)	1.66	
PCB Thickness	1.59	mm
Er	4.3	

Inductance (Lant)	706	nH
Lant min	661	nH
Lant max	870	nH
Capacitance (Cant)	1.1	pF
Resistance (Rant)	1.15	Ω
Self resonance (Fres)	177	MHz



RESET ANTENNA SYNTHESIS

Q	35	
Target impedance	50	Ω
fEMC cut off	21	MHz
L0	470	nH



Check the box if you want to use the autocalculated value for the PN7462/PN7360 or Pn5180

MATCHING NETWORK

Rs	0.28	Ω
C0	122.2	pF
C1	39.7	pF
C2	341.9	pF

Errors / Warnings