Wireless 2 Wireless

WLAN-Bluetooth Module
W2CBW009S

Product Datasheet

Revision 1.1
October 20, 2009

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Revision History:

Revision	Revision Date	Originator	Changes
1.0	10/20/2009	EK	Complete Formatting, Pre-Release Changes, Info addition

1 General Description

This specification provides a general guideline on the performance and the integration of W2CBW009S, a complete wireless subsystem featuring full 802.11 b/g WLAN capability as well as class 1.5 Bluetooth capability in a small form factor module solution. The W2CBW009S device was designed to simplify the process of adding wireless capability without lengthy design cycles or complex RF design. Both radios are fully tested for coexistence, both internally and with other external radio technologies. A full menu of certifications will also be provided, simplifying the certification process for your entire end product and further reducing valuable time-to-market. Based on world-class silicon from Wi2Wi partner Marvell, the W2CBW009S has also been fully optimized for throughput and receive sensitivity through careful design practices. State-of-the art software development resources are also available to create drivers for unique processors and operating systems if needed, or to optimize the wireless subsystem to fit your needed application with ease.

The specification maximum and minimum limits presented herein are those guaranteed when the unit is integrated into the Wi2Wi's W2CBW009S-DEV Development System. These limits are to serve as the representative performance characteristics of the W2CBW009S when properly designed into a customer's product. Wi2Wi makes no warranty, implied or otherwise specified, with respect to a customers design and the performance characteristics presented in this specification.

The W2CBW009S module is available in single antenna configuration.

This device also complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Modifications or changes to this equipment not expressly approved by Wi2Wi may void the user's authority to operate this equipment.

2 Features

- Compact design for easy integration:16 mm x 16mm x 2.3mm
- LGA with 76 pins
- WLAN technology based on Marvell's 88W8688
- Bluetooth technology based on Marvell's 88W8688
- Certified dual mode radio
- Optimized RF and electrical design for better performance in co-existence with other wireless standards
- Dual-antenna design with separate antenna pins for Bluetooth and WLAN (option is available for single antenna solution)
- Operates in 2.4 GHz ISM band
- ROHS Compliant
- Fully integrated coexistence solution
- WLAN Specific Features
  SDIO 1.1 and G-SPI interfaces
  - 802.11s Mesh Networking
  - 802.11h Dynamic Frequency Selection
  - 802.11e Quality of Service
  - 50-Ohm antenna launch
  - Support for WinCE, WinMobile, Windows XP SP3, Vista 32 bit, and Linux 2.6.xx(can be ported to other operating systems)
  - 1, 2, 5.5 and 11 Mbps data rates for 802.11b (DSSS/CCK modulation)
  - 6, 9, 12, 18, 24, 36, 48 and 54 Mbps data rates for 802.1 1g (OFDM modulation)
- Bluetooth Specific Features
  UART, PCM, I2S interfaces
  - 50-Ohm antenna launch
  - Support for WinCE, WinMobile, Windows XP SP3, Vista 32 bit and Linux 2.6.xx (can be ported to other operating systems)
  - GFSK modulation for Bluetooth version 2.1
  - Data rate up to 1Mbps for Bluetooth version 2.1

- Data rate up to 3 Mbps for Bluetooth EDR
- Support for Class 1.5 Bluetooth

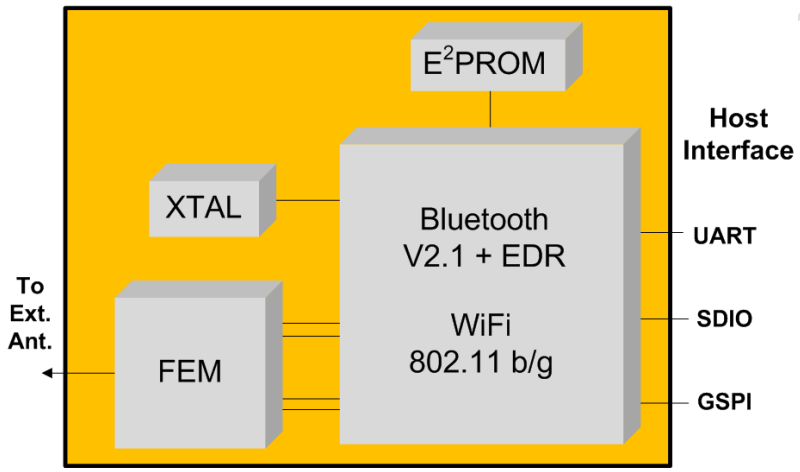
3 System Description

W2CBW009S is a complete module combination of 88W8688 802.1b/g and Bluetooth. It includes all the components needed to operate both the radios. It preserves the characteristics from Marvell chipset while providing the optimized system level functionality and performance.

3.1 Block Diagram

Figure #1 shows the detailed block diagram of W2CBW009S.

Figure 1: Block Diagram



3.2 Pin Description

Table 1: Pin Description

Pin	Pin Name	Type	Supply	Description
1	HSPWR1	Power		Host Power
2	HSPWR2	Power		Host Power
3	HSPWR3	Power		Host Power
4	GND4	Ground		Ground
5	GND5	Ground		Ground
6	ANT_SEL_N	O	HOST_ PWR	Differential Antenna Select Negative Output Default value is 0
7	TR_N	O	HOST_ PWR	Transmit Switch Control Negative Output Default value is 0

8	TR3_N	O	HOST_ PWR	Transmit Switch 3 Negative Output Default value is 0
9	INPACKn	O	VIO_X1	PC Card I/O Mode Input Acknowledge
10	SD_D2	I/O	VIO_X1	SDIO 4-bit Mode: SD_DAT[2] Data Line Bit [2]
11	SD_CLK	I	VIO_X1	SDIO 4-bit Mode: SD_CLK Clock Input
12	SD_CMD	I/O	VIO_X1	SDIO 4-bit Mode: SD_CMD Command
13	SD_D1	I/O	VIO_X1	SDIO 4-bit Mode: SD_DAT[1] Data Line Bit [1]
14	SD_D0	I/O	VIO_X1	SDIO 4-bit Mode: SD_DAT[0] Data Line Bit [0]
15	SD_D3	I/O	VIO_X1	SDIO 4-bit Mode: SD_DAT[3] Data Line Bit [3]
16	GPIO0	I/O	VIO_X1	General Purpose Input/Output 0 External oscillator control
17	GPIO1	I/O	VIO_X1	General Purpose Input/Output 1 WiFi LED
18	GPIO4	I/O	VIO_X1	General Purpose Input/Output 4 WLAN MAC wake-up input
19	GPIO3	I/O	VIO_X1	General Purpose Input/Output 3 UART DSR input
20	GPIO5	I/O	VIO_X1	General Purpose Input/Output 5 UART DTR output
21	GPIO6	I/O	VIO_X1	General Purpose Input/Output 6 UART SOUT output
22	GPIO8	I/O	VIO_X1	General Purpose Input/Output 8 UART CTS input
23	SLEEP_CLK	I	VIO_X1	External Sleep Clock Input
24	BT_STATE	I	VIO_X1	Bluetooth State
25	BT_FREQ	I	VIO_X1	Bluetooth Frequency
26	BT_TX_CONFIRM	O	VIO_X1	Bluetooth Transmit Confirm 0 = Bluetooth allow to transmit 1 = Bluetooth not allow to transmit
27	PDn	I	VIO_X1	Full Power Down (active low)
28	GPIO7	I/O	VIO_X1	General Purpose Input/Output 7 UART SINT input
29	GND29	Ground		Ground
30	GND30	Ground		Ground
31	BT_REQ	I	VIO_X1	Bluetooth Request (3-Wire BCA Mode) 1 = Bluetooth is requesting to transmit or receive packets
32	RESETn	I	VIO_X1	Reset (active low)

33	GPIO2	I/O	VIO_X1	General Purpose Input/Output 2 UART RTS output
34	BRF_TR_P	O	HOST_ PWR	BRF Transmit Switch Positive Output
35	CF_RESET	I	VIO_X1	PC Card I/O Mode Reset (active high)
36	BRF_TR_N	O	HOST_ PWR	BRF Transmit Switch Negative Output
37	TRSTn	I/O	VIO_X2	JTAG Test Reset (active low)
38	TMS	I	VIO_X2	JTAG Test Mode Select Select the internal CPU JTAG controller
39	SCLK	I/O	VIO_X2	SPI Serial Interface Clock
40	SRWB	I	VIO_X2	SPI Serial Interface Data Input
41	ECSn	I/O	VIO_X2	SPI EEPROM Chip Select
42	SDA	I/O	VIO_X2	SPI Serial Interface Data Output
43	TCK	I	VIO_X2	JTAG Test Clock Input
44	TDO	O	VIO_X2	JTAG Test Data Output
45	TDI	I	VIO_X2	JTAG Test Data Input
46	TMS2	I	VIO_X2	JTAG Test Mode Select Select the system JTAG controller
47	SCAN_EN	I	VIO_X2	Scan Enable
48	GPIO10	I/O	VIO_X2	General Purpose Input/Output 10 AIU_TWSI_Data/SD_DAT[0]
49	GPIO9	I/O	VIO_X2	General Purpose Input/Output 9 AIU_TWSI_CLK
50	GPIO12	I/O	VIO_X2	General Purpose Input/Output 12 BT_PCM_DOUT/I2S_DOUT
51	GPIO11	I/O	VIO_X2	General Purpose Input/Output 11 BT_PCM_DIN/I2S_DIN
52	WLAN_RF_IO	RF		Wi-Fi /Bluetooth RF
53	GPIO17	I/O	VIO_X2	General Purpose Input/Output 17 Bluetooth LED
54	GND54	Ground		Ground
55	GND55	Ground		Ground
56	GND56	Ground		Ground
57	GPIO16	I/O	VIO_X2	General Purpose Input/Output 16 AIU_SPDIF
58	GND58	Ground		Ground
59	GND59	Ground		Ground
60	GND60	Ground		Ground
61	GND61	Ground		Ground
62	GPIO13	I/O	VIO_X2	General Purpose Input/Output 13 BT_PCM_CLK/I2S_MCLK
63	GPIO14	I/O	VIO_X2	General Purpose Input/Output 14 BT_PCM_SYNC/I2S_LRCLK
64	GPIO15	I/O	VIO_X2	General Purpose Input/Output 15 BT_PCM_MCLK/I2S_CCLK

65	VIO_X12	Power		1.8V/3.3V Host Support
66	VIO_X11	Power		1.8V/3.3V Host Support
67	GND67	Ground		Ground
68	V18D1	Power		1.8V Digital Host Support
69	V18D2	Power		1.8V Digital Host Support
70	GND70	Ground		Ground
71	VIO_X22	Power		1.8V/3.3V Host Support
72	VIO_X21	Power		1.8V/3.3V Host Support
73	GND73	Ground		Ground
74	HSPWR74	Power		Host Power 3.3V
75	HSPWR75	Power		Host Power 3.3V
76	HSPWR76	Power		Host Power 3.3V

4 Electrical Characteristics

Table 2: Electrical Characteristics

Parameter	Test Condition	MIN	TYP	MAX	UNIT
Absolute Maximum Ratings					
Storage Temperature		-55	-	125	°C
Supply Voltage		-	3.0	4.2	V
Recommended Operating Conditions					
Operating Temperature		-30	-	70	°C
Supply Voltage		2.7	3.0	3.3	V
802.11b Current Consumption					
Initialization Current		-	100	-	mA
Continuous Transmit	@11Mbps	190	210	230	mA
Continuous Receive	@11Mbps	160	180	190	mA
IEEE 802.11 Power Save Mode		-	10	-	mA
Deep Sleep		-	2	-	mA
802.11b RF System Specifications					
Transmit Power Output		-	15	-	dBm
Receive Sensitivity	1 Mbps, 8% PER	-	-90	-	dBm
	2 Mbps, 8% PER	-	-90	-	dBm
	5.5 Mbps, 8% PER	-	-90	-	dBm
	11 Mbps, 8% PER	-	-88	-	dBm
Maximum Receive Level	PER<8%	-	IEEE Compliant	-	dBm
Transmit Frequency Offset	Low, Middle, High Channels	-	±10	-	
Spectral Mask	Max. TX Power	-	-40@fc±11MHz	-	dBc
		-	-60@fc±22MHz	-	
Error Vector Magnitude	Max. TX Power @ 11Mbps	-	-36	-	dB

Carrier Suppression	Max. TX Power	-	-25	-	dBc
Adjacent Channel Rejection	Desired channel is 3dB above sensitivity, PER<8%	-	48	-	dBc
802.11g Current Consumption					
Initialization Current		-	100	-	mA
Continuous Transmit	@54Mbps	220	230	240	mA
Continuous Receive	@54Mbps	200	210	220	mA
IEEE 802.11 Power Save Mode		-	10	-	mA
Deep Sleep		-	2	-	mA
802.11g RF System Specifications					
Transmit Power Output		-	15	-	dBm
Receive Sensitivity	6 Mbps, 10% PER	-	-90	-	dBm
	9 Mbps, 10% PER	-	-88	-	dBm
	12 Mbps, 10% PER	-	-88	-	dBm
	18 Mbps, 10% PER	-	-87	-	dBm
	24 Mbps, 10% PER	-	-83	-	dBm
	36 Mbps, 10% PER	-	-80	-	dBm
	48 Mbps, 10% PER	-	-75	-	dBm
	54 Mbps, 10% PER	-	-74	-	dBm
Maximum Receive Level	PER<10%	-	IEEE Compliant	-	dBm
Transmit Frequency Offset	Low, Middle, High Channels	-	±10	-	PPM
Spectral Mask	Max. TX Power	-	-30@fc±11MHz	-	dBc
		-	-40@fc±20MHz	-	
		-	-50@fc±30MHz	-	
Error Vector Magnitude	Max. TX Power @ 54Mbps	-	-29	-	dB
Carrier Suppression	Max. TX Power	-	-25	-	dBc
Adjacent Channel Rejection	Desired channel is 3dB	-	15	-	dBc
	above sensitivity, 54Mbps,				
	PER<1 0%				
Bluetooth Current Consumption (USB BUS)					
Initialization Current		-	15	-	mA
Continuous Transmit		40	45	50	mA
Continuous Receive		28	32	38	mA
Deep Sleep		-	2	-	mA
Bluetooth RF System Specifications					
Transmit Power Output		1.5	3	4	dBm

Receive Sensitivity	1 Mbps, 0.1% BER	-	-84	-	dBm
	2 Mbps, 0.1% BER	-	-87	-	dBm
	3 Mbps, 0.1% BER	-	-82	-	dBm
Initial Carrier Frequency Tolerance		-	5	-	kHz

5 WLAN External Host Interfaces

For connection to a host processor, the W2CBW009S supports the Secure Digital Input Output (SDIO) and Generic SPI (G-SPI) interfaces for WLAN. The choice of interface is dependent on the required data throughput, with SDIO having a throughput that is approximately four times greater than G-SPI.

If the WLAN SDIO interface is selected for connection to a host processor, then the host processor must support SDIO – (SD is not sufficient). If the selected processor does not have an integrated SDIO controller, then an external SDIO bridge can be used (e.g. SDIO-PCI Bridge for interfacing with a process supporting PCI interface only).

If the WLAN G-SPI interface is selected for connection to a host processor, then the host processor must support G-SPI – (SPI is not sufficient). If the selected processor only has SPI, then it might be possible to implement G-SPI with a combination of the SPI and a GPIO pin for interrupt. If the selected processor does not have SPI interface, then it might be possible to implement a G-SPI interface using a combination of GPIO pins. Please contact your sales representative if your processor does not support SDIO or G-SPI interfaces.

5.1 SDIO Interface

W2CBW009S supports SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the WLAN device. The SDIO interface contains interface circuitry between an external SDIO bus and the internal shared bus.

W2CBW009S acts as a device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

The SDIO device interface main features include:

- On-chip memory used for CIS
- Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes at the full clock range of 0 to 50 MHz
- Special interrupt register for information exchange

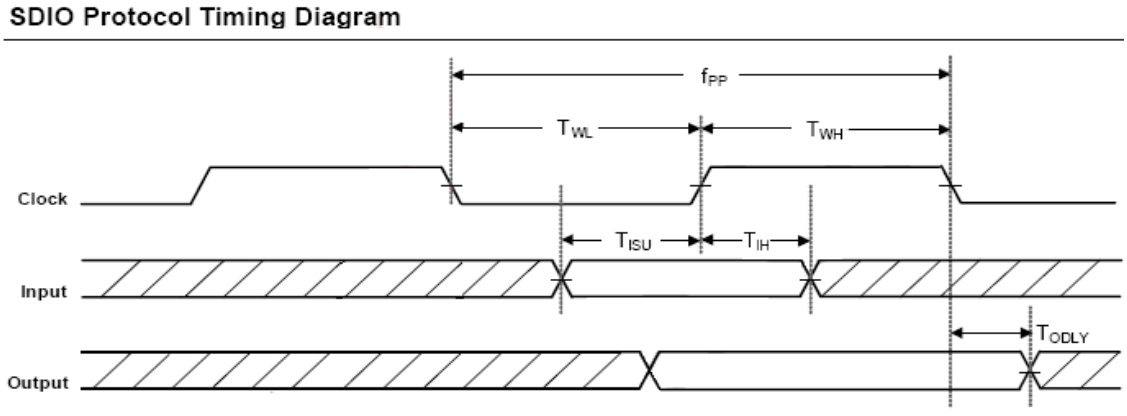
- Allows card to interrupt host

Table 3: SDIO Pin Map

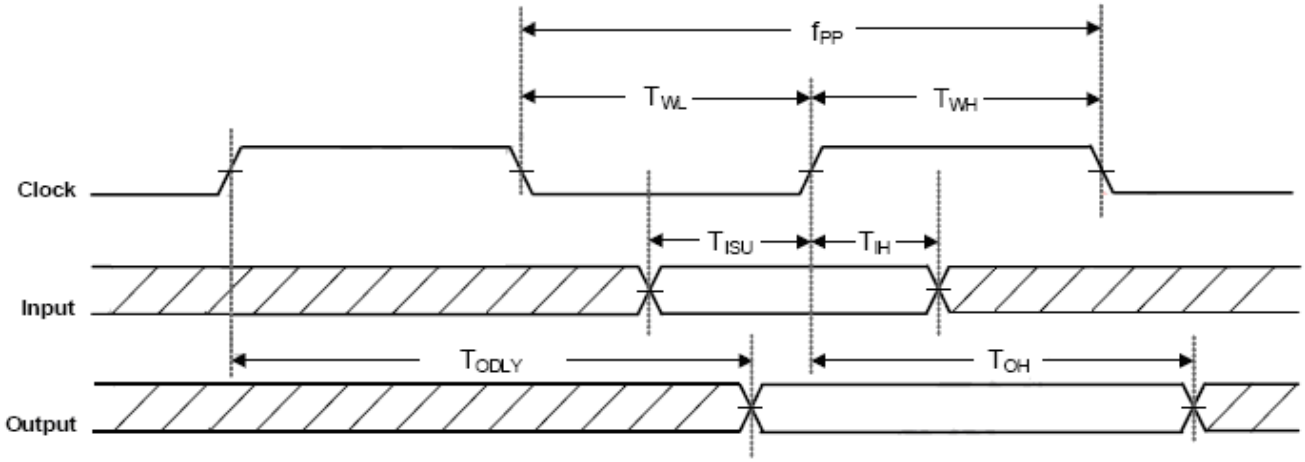
W2CBW009S Pin Name	Signal Name	Type	Description
SD_D3	DAT 3	I/O	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used SDIO SPI mode: Chip select (neg true)
SD_D2	DAT 2	I/O	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPI mode: Reserved
SD_D1	DAT 1	I/O	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt SDIO SPI mode: Interrupt
SD_D0	DAT 0	I/O	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line SDIO SPI mode: Data out
SD_CMD	CMD	I/O	SDIO 4-bit mode: Command/Response SDIO 1-bit mode: Command Line SDIO SPI mode: Data in
SD_CLK	CLK	I/O	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock SDIO SPI mode: Clock

5.2 SDIO Protocol Timing Diagrams

Figure 2: SDIO Protocol Timing



SDIO Protocol Timing Diagram—High Speed Mode



***Note**: The SDIO-SPI CS Signal timing is identical to all other SDIO inputs*

Table 4: SDIO Timing Data

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{pp}	Clock Frequency	Normal	0	--	25	MHz
		High speed	0	--	50	MHz
T_{WL}	Clock Low Time	Normal	10	--	--	Ns
		High speed	7	--	--	Ns
T_{WH}	Clock High Time	Normal	10	--	--	Ns
		High speed	7	--	--	Ns
T_{ISU}	Input Setup Time	Normal	5	--	--	Ns
		High speed	6	--	--	
T_{IH}	Input Hold Time	Normal	5	--	--	Ns
		High speed	2	--	--	
T_{ODLY}	Output Delay Time	--	0	--	14	Ns
T_{OH}	Output Hold Time	High speed	2.5	--	--	Ns

***Note**: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified*

5.3 G-SPI Interface

W2CBW009S supports a generic, half-duplex, DMA-assisted G-SPI host interface (G-SPI) that allows a host controller using a Generic SPI bus protocol to access the WLAN device. The G-SPI interface contains interface circuitry between an external G-SPI bus and the internal shared bus.

The 88W8688 acts as the device on the G-SPI bus. The host unit can access the G-SPI registers directly and can access shared memory in the device through the use of BARs and a DMA engine.

The G-SPI unit supports Generic SPI Interface protocols as detailed in the following sections. The design is capable of 50 MHz operation. The interface supports the following functionality:

- G-SPI unit bus device operation
- G-SPI unit register read / write
- Interrupt generation to internal CPU
- Interrupt generation to the SPI unit host
- DMA to internal memories
- Wake Interrupt to the Power Management Unit

Table 5: GSPI Pin Map

W2CBW009S Pin Name	Generic SPI Bus Name	Type	Description
SPI_CLK	SCLK	Input	SPI Unit Clock Input
SPI_SCSn	CSn	Input	SPI Unit Active Low Chip Select Input
SPI_SDI	DI	Input	SPI Unit Data Input
SPI_SDO	DO	Output	SPI Unit Data Output
SPI_SINTn	INTn	Output	SPI Unit Active Low Interrupt Output
SPI_CLK_REQ	CLK_EN	Output	SPI Unit Clock Enable Output
RESETn	RSTn	Input	Reset Input

6 Bluetooth External Interfaces

For connection to a host processor, the W2CBW009S supports UART interface. There is also a PCM interface for connection to audio PCM devices such analog to digital and digital to analog converters. The PCM selection is made in firmware.

6.1 UART Interface

W2CBW009S UART interface provides a simple mechanism for communicating with other serial devices using the RS232 standard. Four signals are used to implement the UART function:

- BT_UART_TX
- BT_UART_RX
- BT_UART_RTS
- BT_UART_CTS
- BT_UART_DSR
- BT UART DTR

When W2CBW009S is connected to another digital device, BT_UART_RX and BT_UART_TX transfer data between the two devices. The remaining two signals, BT_UART_CTS and BT_UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC. An external RS232 transceiver chip is also needed.

Table 6: UART Baud Rates

Parameter		Possible values
Baud Rate	Minimum	1200 Baud (≤2% Error)
		9600 Baud (≤1 % Error)
	Maximum	4MBaud (≤1% Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Channel		8

The UART interface is capable of resetting W2CBW009S upon reception of a break signal.

6.2 PCM Interface

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, W2CBW009S has hardware support for continual transmission and reception of PCM data, so reducing processor overhead for wireless headset applications. W2CBW009S offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer. Hardware on W2CBW009S allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time.

W2CBW009S can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. W2CBW009S is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ-law or A-law compounded sample formats at 8k samples/s, and can receive and transmit on any selection of three of the first four slots following PCM_SYNC.

W2CBW009S interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- W2CBW009S is also compatible with the Motorola SSI interface

7 Antenna and Clock

W2CBW009S has single antenna interfaces for Bluetooth and WLAN. The antenna interfaces has 50 Ohm impedance.

W2CBW009S has an internal crystal oscillator with 38.4 MHz frequency (frequency stability +/- 20ppm) and requires no external clock source. This crystal provides clock for both WLAN and Bluetooth.

8 Software Specifications

8.1 Wireless LAN

Wi2Wi can provide the end user driver needed for operating WLAN part of W2CBW009S, if available, otherwise a 3rd part developer can create for a fixed NRE. This driver is specific to the operating system, processor and host bus – it cannot be used for any other processors, operating systems or host buses. Since the operating system and platform matrix is quite large, it is not possible to have all the combinations off the shelf. Please contact your sales representative on the actual driver availability.

The following is a brief description of the driver features along with the processors, operating systems and host buses.

- Key Features
  - WEP encryption (64 bit/128 bit)
  - IEEE power save mode
  - Deep sleep mode
  - Infrastructure and ad-hoc mode
  - Rate adaptation
  - WPA TKIP security
  - WPA2
  - Bluetooth coexistence
- Operating System Support
  - WinCE 6.0, WinMobile 6.0
  - Linux: Slackware 9.1, Fedora Core 1.0; Kernel: 2.4.22 & above
  - Windows XP SP3, Vista 32 bit
- Platform Support
  - Intel x86
  - Marvell PXA270, PXA300, PXA310, PXA320, OMAP35xx, i.Mx31, SMDK2443
- Host Buses
  - SDIO
  - G-SPI

In addition to the end user driver, Wi2Wi also provides engineering tools needed for production testing and certification when available.

8.2 Bluetooth

Bluetooth portion of W2CBW009S needs stack and profiles for operation. It uses a standard HCI interface – any commercial stack or profile supporting the standard interface will work with W2CBW009S. Wi2Wi does not provide this stack, though a free 30 day evaluation version from Toshiba is included on the DevKit CD.

WinCE, WinMobile and Vista 32 bit have embedded stack and basic profiles that work with W2CBW009S. Advanced profiles for these operating systems can be procured from commercial vendors like IVT, CSR, iAnywhere and Toshiba.

Wi2Wi will work with the customers to provide a suitable solution for the stack and profiles. There may be some additional cost associated with this based on the requirements. Please contact your sales representative to get more details.

The following are the key features of a typical HCI stack:

- Bluetooth v2.1 + EDR mandatory functionality
  - EDR, 3Mbps payload data rate
  - Support 2-DH1, 2-DH3, 2-DH5, 3-DH1, 3-DH3 and 3-DH5 packet types
  - Support 2-EV3, 2-EV5, 3-EV3 and 3-EV5 packet types
- Bluetooth v1 .2 mandatory functionality:
  - Adaptive Frequency Hopping (AFH), including classifier
  - Faster connection enhanced inquiry scan (immediate FHS response)
  - LMP improvements
  - Parameter ranges
  - Support of AUX1 packet type
- Optional v2.1 + EDR functionality supported:
  - AFH as Master and automatic channel classification
  - Fast connect interlaced inquiry and page scan plus RSSI during inquiry
  - Extended SCO (escort), eV3 + CRC, eV4, eV5
  - SCO handle
  - Synchronization
- The firmware has been written against the Bluetooth Core Specification v2.0 + EDR:
  - Bluetooth components: Baseband (including LC), LM and HCI
  - Standard USB v2.0 (full speed) and UART HCI transport layers
  - All standard radio packet types
  - Full Bluetooth data rate, up to 723.2Kbits/s asymmetric(1)
  - Operation with up to seven active slaves(1)
  - Maximum number of simultaneous active ACL connections: 7(2)
  - Maximum number of simultaneous active SCO connections: 3(2)
  - Operation with up to three SCO links, routed to one or more slaves o All standard SCO voice coding, plus .transparent SCO.
  - Standard operating modes: page, inquiry, page-scan and inquiry-scan

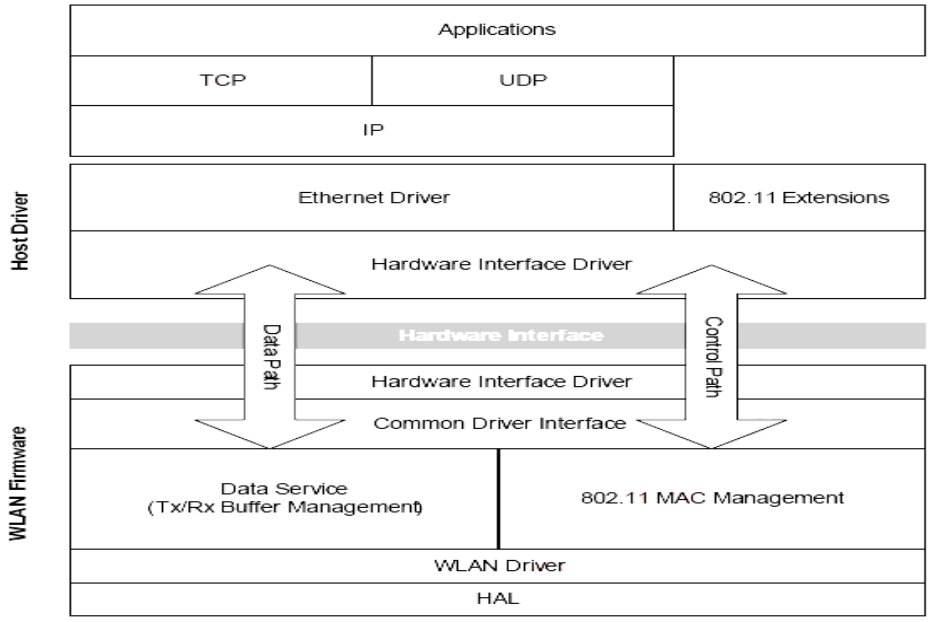
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power-saving mechanisms: Hold, Sniff and Park modes, including Forced Hold.
- Dynamic control of peers.
- Master/slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth Test Modes

- Operating System Support
  - WinCE 6.0, WinMobile 6.0
  - Linux
  - Windows XP SP3, Vista 32 bit
- Host Buses
  - UART

9 WLAN Software Architecture

A simplified view of the overall WLAN software architecture is illustrated in the figure below. It is partitioned between the host processor and the WLAN firmware that resides on the Wi2Wi WiFi module.

Figure 3: Software Architecture



9.1 Host Processor

The TCP/IP stack, Ethernet Driver and the 802.11 extensions reside on the host processor. The Hardware Interface Driver, which can be G-SPI or SDIO, is partitioned between the host and the firmware on the WiFi.

The WLAN firmware for the WiFi is downloaded through the selected host interface (G-SPI or SDIO) by the Hardware Interface Driver at power up.

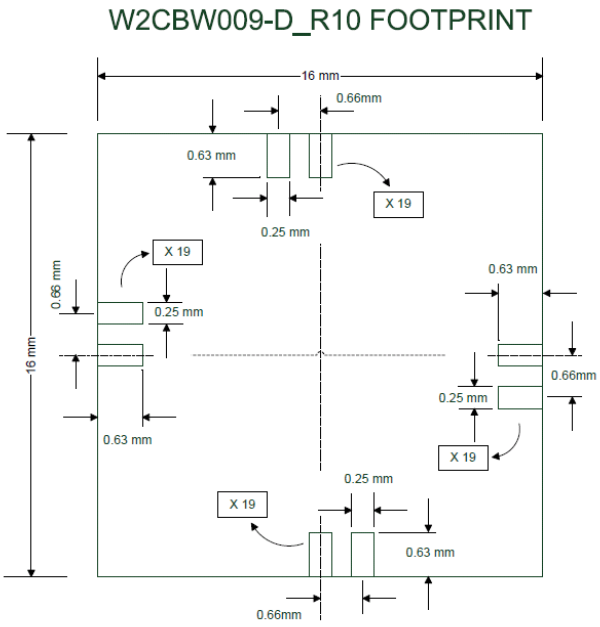
Once the firmware is downloaded, the Data Path and the Control Path between the host and WiFi are established, and information can flow between the two devices.

10 Manufacturing Notes

10.1 Physical Dimensions and Pin Locations

- Physical Size: 15mm x 15mm
- Pad Size: 0.25mm X 0.63mm
- Pad Spacing: 0.66 mm
- Pins: 76 (4 x 19) +4 Corner ground Pads for shield

Figure 4: Physical Dimensions and Pin Locations for a Single Antenna Device



10.2 Storage and Baking Instructions

W2CBW009S is an MSL3 grade part. After opening the bag, the parts should be:

a. Stored as per J-STD-003 standard
b. Mounted within 72 hours of factory conditions (<=30C, 60% RH)

If any of the above conditions is not met, the parts should be baked as listed below prior to assembly:

a. S90C for 4 hours

b. M125C for 12 hours

10.3 Recommended Reflow Profile

Figure 5: Reflow Profile
TBD

11 Disclaimers

Wi2Wi, Inc. PRODUCTS ARE NOT AUTHORISED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE MANAGING DIRECTOR OF Wi2Wi, Inc.
The definitions used herein are:
a) Life support devices or systems are devices which (1) are intended for surgical implant into the body, or (2) support or sustain life and whose failure to perform when properly used in accordance with the instructions for use provided in the labeling can reasonably be expected to result in a significant injury to the user. b) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
Wi2Wi does not assume responsibility for use of any of the circuitry described, no circuit patent licenses are implied and Wi2Wi reserves the right at any time to change without notice said circuitry and specifications.

11.1 Data Sheet Status

Wi2Wi, Inc. reserves the right to change the specification without prior notice in order to improve the design and supply the best possible product. Updated information, firmware and release notes will be made available on www.wi2wi.com. Please check with Wi2Wi Inc. for the most recent data before initiating or completing a design.

12 Certifications

W2CBW009S shall conform to the following standards when integrated to the W2CBW009S-DEV development system (these certifications have not been completed yet as the part will go into production in Sep 2008).

EMC/Immunity

- United States: FCC Part 15
- Canada: ICES 033
- European Union: EN 55022, IEC 1004/CISPR 22
- Taiwan: CNS 13438
- Korea: MIC

Product Safety

- United States/Canada: UL/CSA 60950, UL 61010, UL 60065, CSA 601,CSA 61010,C22.2 No. 225
- European Union: EN 60950, EN61010, IEC 60065, IEC 60601
- Restriction of Hazardous Substances Directive (RoHS) 2002/95/EC

13 References

13.1 Specifications

- IEEE 802.11 b/g wireless LAN Specification
- Specification of the Bluetooth System, v2.1+EDR,
- SDIO full-speed card specification
- Universal Serial Bus Specification, v2.0, 27 April 2000

13.2 Trademarks, Patents and Licenses

- Trademarks: Bluetooth, Wi-Fi
- Licenses: 88W8688 Software from Marvell;

13.3 Other

- W2CBW009S-DEV: Development Kit, WLAN – Bluetooth Module