WB222

AR9462 based
WLAN 2 x 2 802.11 a/b/g/n +
BT Combo Reference Design
PCIe Half-Mini Form Factor

DATE	REVISION NUMBER	INITIALS	DESCRIPTION
8/1/2010	250-02062-010	HT	Initial release; based on 8675_245-02010-010-sch.dsn
11/24/2010	250-02062-011	HT	BOM Changes: 1) R31=NL. R43=0ohm. (Rework6 - configure to use internal switcher). 2) C61=C66=8.2pF; C64=1.5pF;C62=C63=C67=C68=1.0pF;L25=L27=2.7nH. (Rework10 - 2G TX Chain1 matching improvements). 3) C17=C22=8.2pF; C20=0.5pF;C18=C19=2.2pF; C23=C24=2.7pF;L4=2.7nH;L6=3.3nH. (Rework11 - 2G TX Chain0 matching improvements). 4) L30=L28=10nH. (Rework12 - 5G TX Chain1 matching improvements). 5) C27=0.4pF;C38=0.6pF. (Rework13 - Chain0 Diplexer improvements).
01/06/2011	250-02062-012	HT	BOM Changes: 1) R19=2.7pF. (Rework14 - Chain0 Diplexer tuning). 2) C52=C53=L19=NL;L18=4.7nH;C48=2.2pF;C49=2.7pF;L17=2.0nH (Rework17 - Chain1 RX tuning). 3) L12=4.7nH;C39=2.0pF. (Rework21 - Chain0 Diplexer tuning).
02/07/2011	250-02062-013	HT	BOM Changes: 1) C17=C22=2.2pF. (Rework22 - Chain0 2G TX).
05/19/2011	250-02062-021	FM	BOM Changes: 1) C20=1.5pF, C17=C22=10pF, C23=C24=3pF, L4=3.3nH. (Chain0 2G TX). 2) C67=C68=2pF (Chain1 2G TX). 3) C41=C45=C42=C46=0.3pF, L14=L15=2.1nH (Chain0 5G TX).
05/24/2011	250-02062-022	FM	BOM Changes: 1) C67=C68=1.8pF, C116=0ohm, L37=C119=1.8pF, R50=2.7nH (Chain1 2G TX).
05/27/2011	250-02062-040	FM,TH	1) Add R56 and R57 for Jupiter 1.0 or Juipter 2.0 selection. 2) Add L42 and L43 for ESD protection. 3) Add R55, C65 for isolation. Add R59/R60 (EEPROM SCL pull up Res backup). 4) Del C34 5) Chain#0 xLNA refer from Chain#1 and HB112/116.
06/21/2011	250-02062-041	TH	1) Manually add the C45, C46, C133, C134 and cut U1 pin5, 8 to solve 2G Tx Chain#0 oscillation. Its matching also changed.
06/24/2011	250-02062-050	TH	1) Del C58. Change 2G Rx chain#0,1 structure. 2) Add R61, R62 to bypass xLNA.
07/15/2011	250-02062-051.betaA	TH	1) L20=22nH, L23=1.6nH for better Rx performance. 2) C130=NL, L44=2nH, C119=1pF for Chain#1 2G Tx EVM.
08/04/2011	250-02062-052	RL	1. Page 5, Fix Chain1, 2.4G, TX EVM and 2-nd Harmonic: L44=2.2nH, C130=1.0pF, C119=1.0pF,L27=1.8nH 2. Page 6, Fix PCIe Interface: C104=C105=100nF 3. Page 3, Fix BT bring up: R44=10K ohm
08/14/2011	250-02062-053	RL	1. Page 5, Fix 2.4G TX: L27=2.2nH
09/01/2011	250-02062-060	RL	1. Page 3, fix chain1 2.4G Tx: Remove C13,C14 2. Page 4, 5G Rx: Non-deposit LNA and relative components 3. Page 4, 5G Rx without LNA: Modify L10=L11=1nH 4. Page 4, Fix 5G Tx: Modify L14=L15=2.4nH,C41=C46=0.5pF,C42=0.2pF 5. Page 4, Fix 2.4G Tx: Modify L4=L6=3nH, C18=C19=C23=C24=1.2pF 6. Page 5, Non-deposit LNA and relative components 7. Page 5, 2.4G Rx without LNA: Modify L9=L47=3.0nH,C135=1pF, C53=1.5pF,L17=2.4nH,C51=1.2pF 8. Page 5, 5G Rx without LNA: Modify L21=L23=1nH,C59=0.3pF 9. Page 5, Fix chain1 2.4G Tx: Add L52=L53=10nH, Modify L27=2.7nH,C67=C68=1pF,L44=2.4nH,C130=C119=1.5pF 10. Page 3, WOW function: Reserve R28 for WOW function
09/13/2011	250-02062-061	RL	1. Page 3, Modify R11=10K ohm, R13=0 ohm and R12=NA
09/14/2011	250-02062-070	RL	1. Page 3, Reserve R51, R53 for case of without BT EEPROM 2. Page 3, Reserve R71, R72 for case of without WLAN EEPROM 3. Page 3, Reserve one serial Flash 4. Page 3, Reserve R50 for WOW function
11/02/2011	250-02062-071	RL	1. Page 3, Remove: U2,U3,R37,R46; Put R51=R53=R71=R72=10K ohm for Non-EEPROM 2. Page 5, Modify: L22=1.8nH,C135=1.3pF,C52=1.5pF,C51=1.8pF,L27=3.3nH 3. Page 6, Remove: C65,C88
11/25/2011	250-02062-072	RL	1. Page 4: Modify C42=0.3pF to fix Tx mask 2. Page 5: Modify C71=0.5pF to fix Tx mask

CONTRACT NO.	
DRAWN BY	DATE
ENGINEER	
PROJECT ENGINEER	
QUALITY ASSURANCE	
CONFIGURATION	
DESIGN ACTIVITY APPROVAL	
DESIGN APPROVAL	

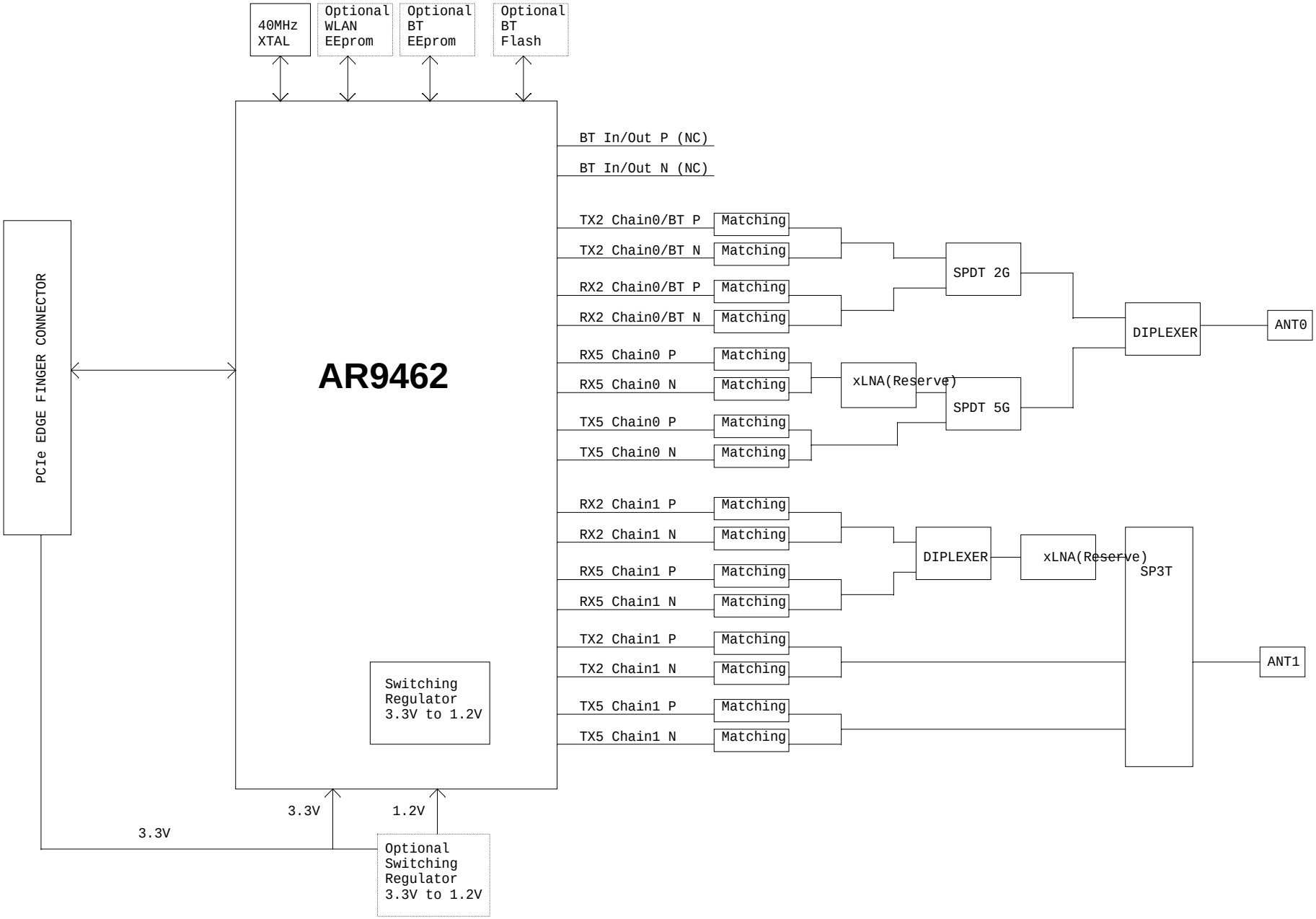
QUALCOMM ATHEROS
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110, USA

TITLE

Title_and_Rev

SIZE	CAGE Code	DWG NO	REV
C	<Cage Code>	WB222-245-02062-072	072

SCALE	RELEASE DATE	SHEET
NONE	Friday, November 25, 2011	1 of 6



Qualcomm ATHEROS CONFIDENTIAL -- PRELIMINARY

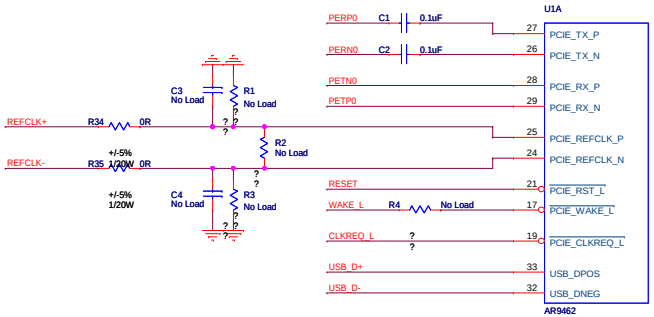
<Variant Name>

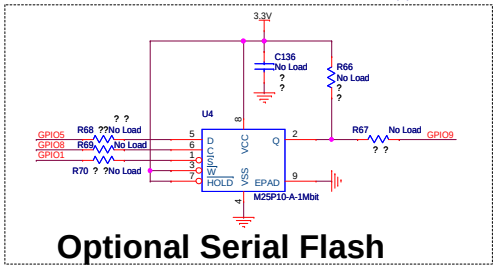
Qualcomm ATHEROS

QUALCOMM ATHEROS
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110

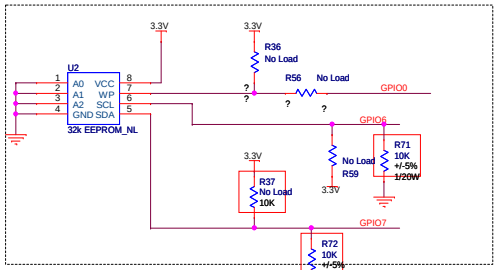
TITLE: **Block_Diagram**

DATE	SIZE	REV	SHEET	DWG NO
Friday, November 25, 2011	C	072	2 OF 6	WB222-245-02062-072



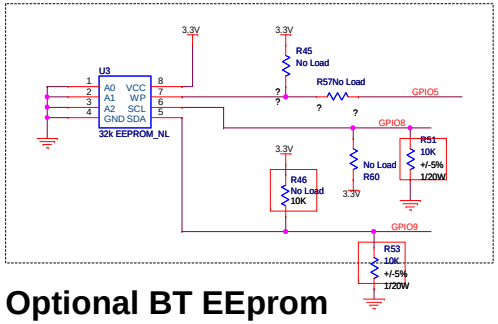


Optional Serial Flash



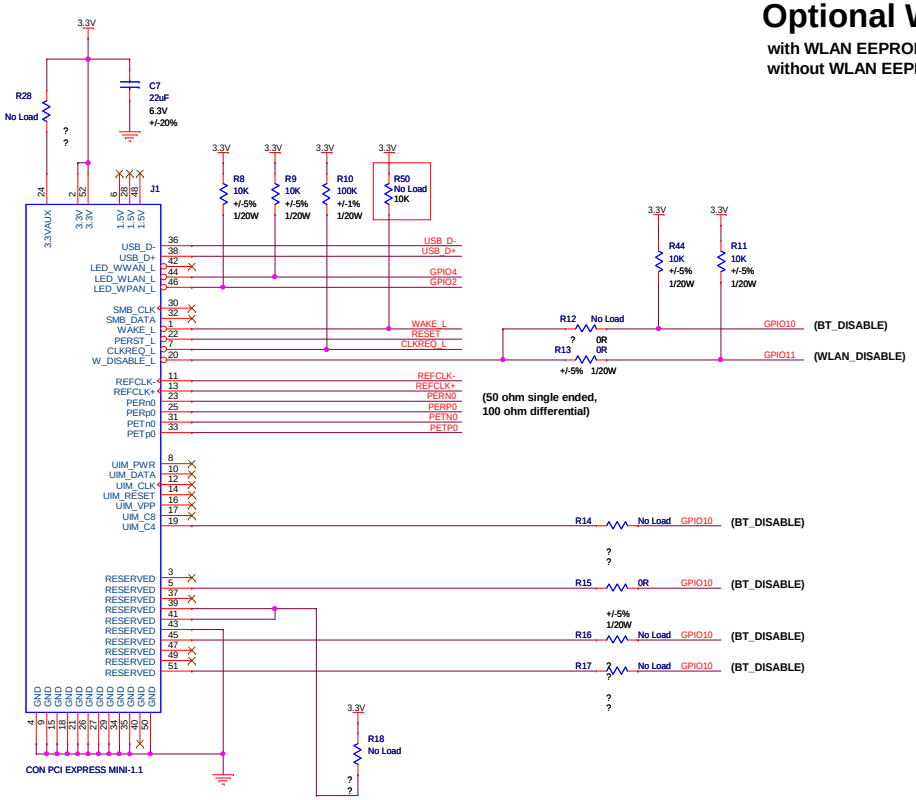
Optional WLAN EEprom

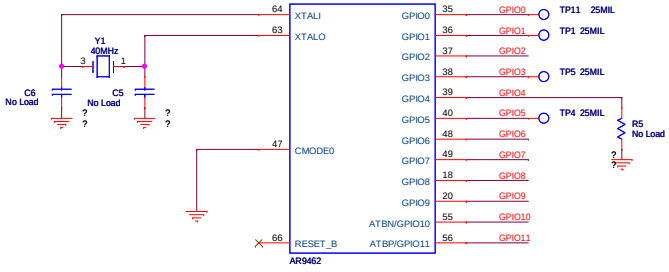
with WLAN EEPROM, put U2, R37=10K ohm
without WLAN EEPROM, U2=R37=NA, put R71=R72=10K ohm

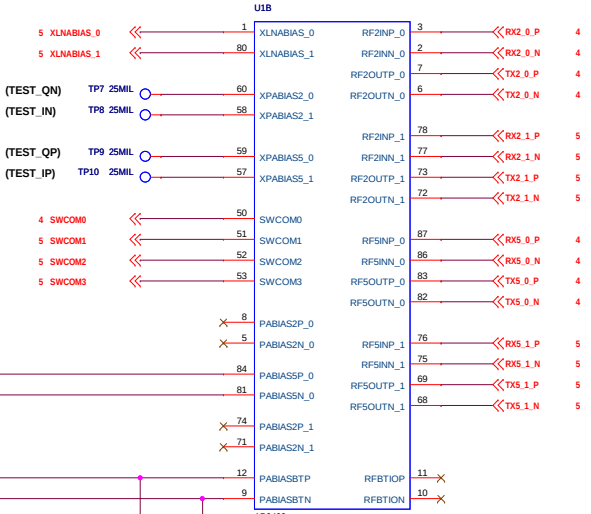


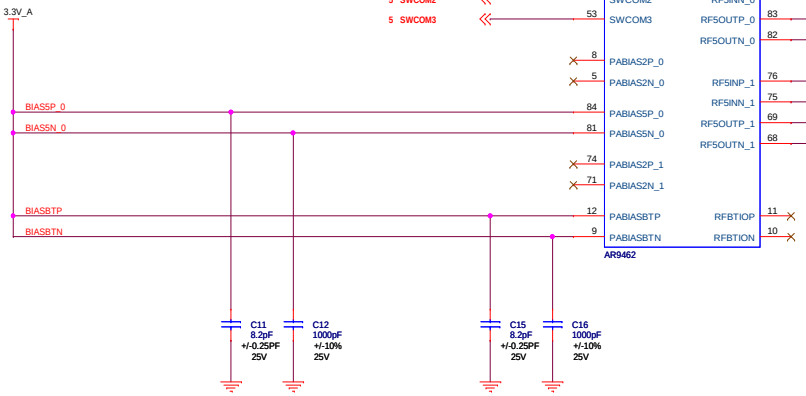
Optional BT EEprom

wtih BT EEPROM, put U3, R46=10K ohm
wthout BT EEPROM, U3=R46=NA, put R51=R53=10K ohm





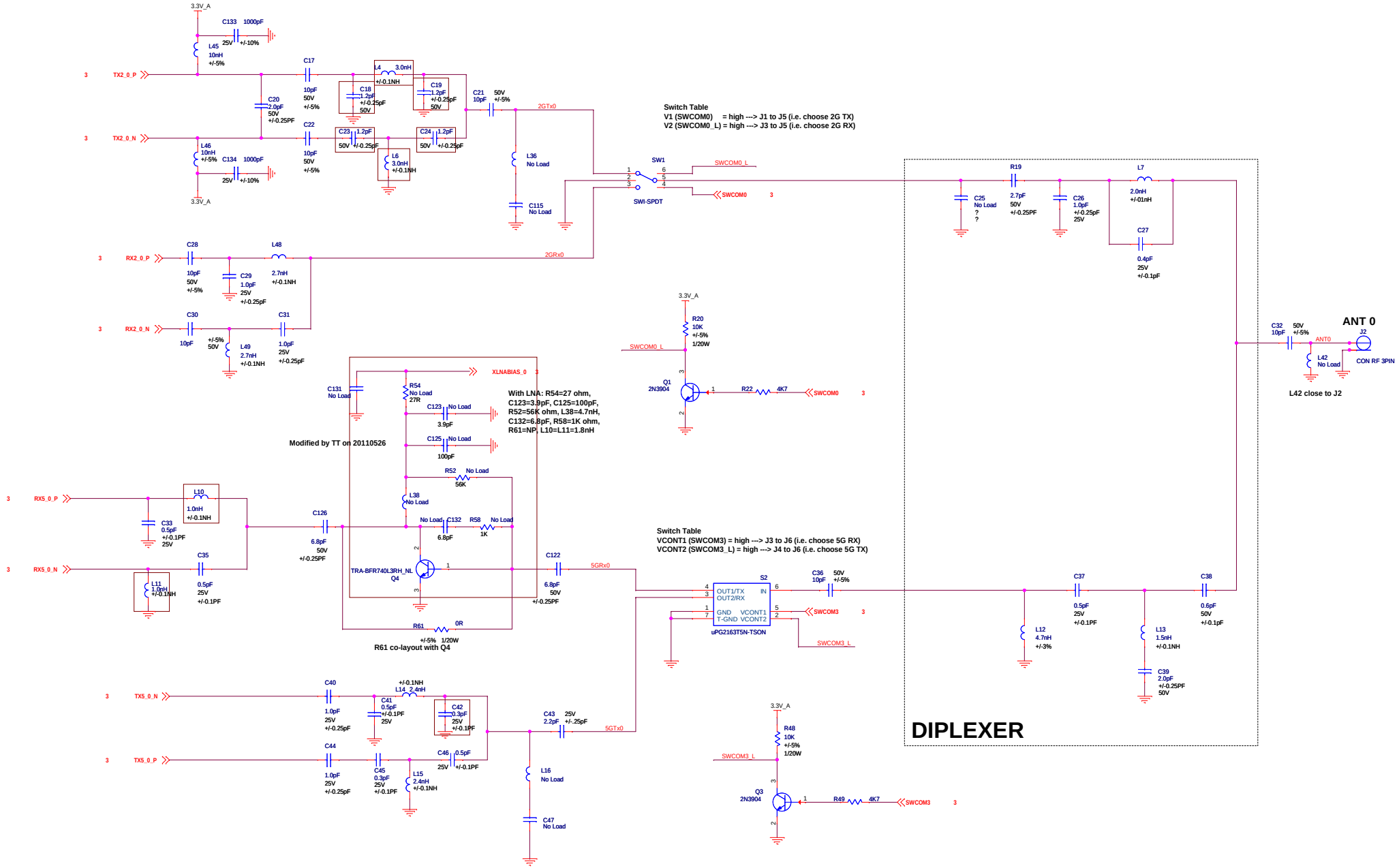




Qualcomm ATHEROS CONFIDENTIAL -- PRELIMINARY

<Variant Name>

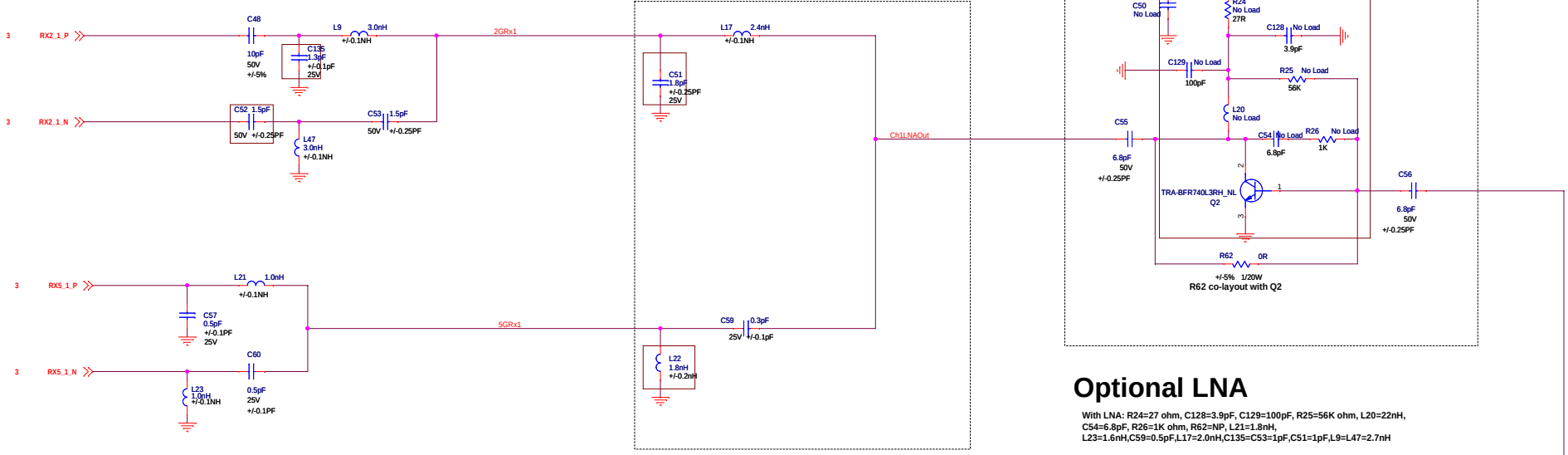
QUALCOMM ATHEROS 1700 TECHNOLOGY DRIVE SAN JOSE, CA 95110				TITLE: Digital	
DATE: Friday, November 25, 2011	SIZE: C	REV: 072	SHEET: 3 OF 6	DWG NO: WB222-245-02062-072	



Qualcomm ATHEROS CONFIDENTIAL -- PRELIMINARY

<Variant Name>

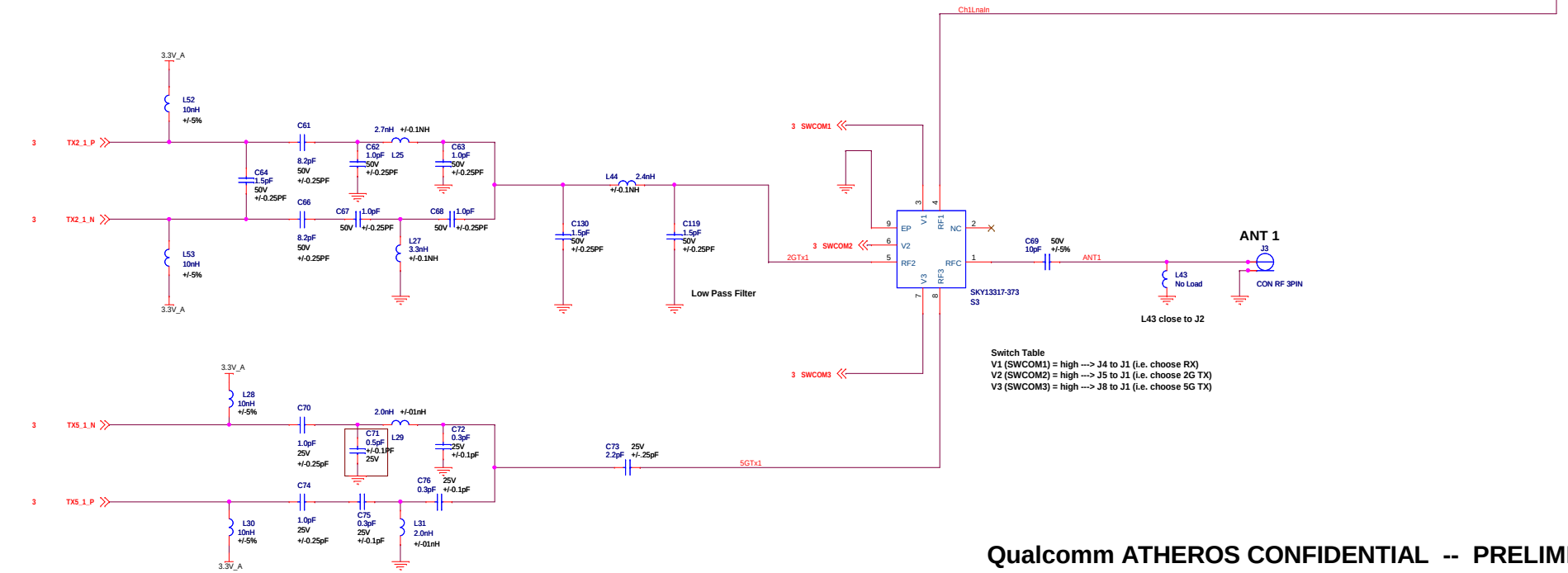
QUALCOMM ATHEROS 1700 TECHNOLOGY DRIVE SAN JOSE, CA 95110				TITLE **Chain0**	
DATE Friday, November 25, 2011	SIZE C	REV 072	SHEET 4 OF 6		DWG NO **WB222-245-02062-072**



Optional LNA

With LNA: R24=27 ohm, C128=3.9pF, C129=100pF, R25=56K ohm, L20=22nH,
C54=6.8pF, R26=1K ohm, R62=NP, L21=1.8nH,
L23=1.6nH,C59=0.5pF,L17=2.0nH,C135=C53=1pF,C51=1pF,L9=L47=2.7nH

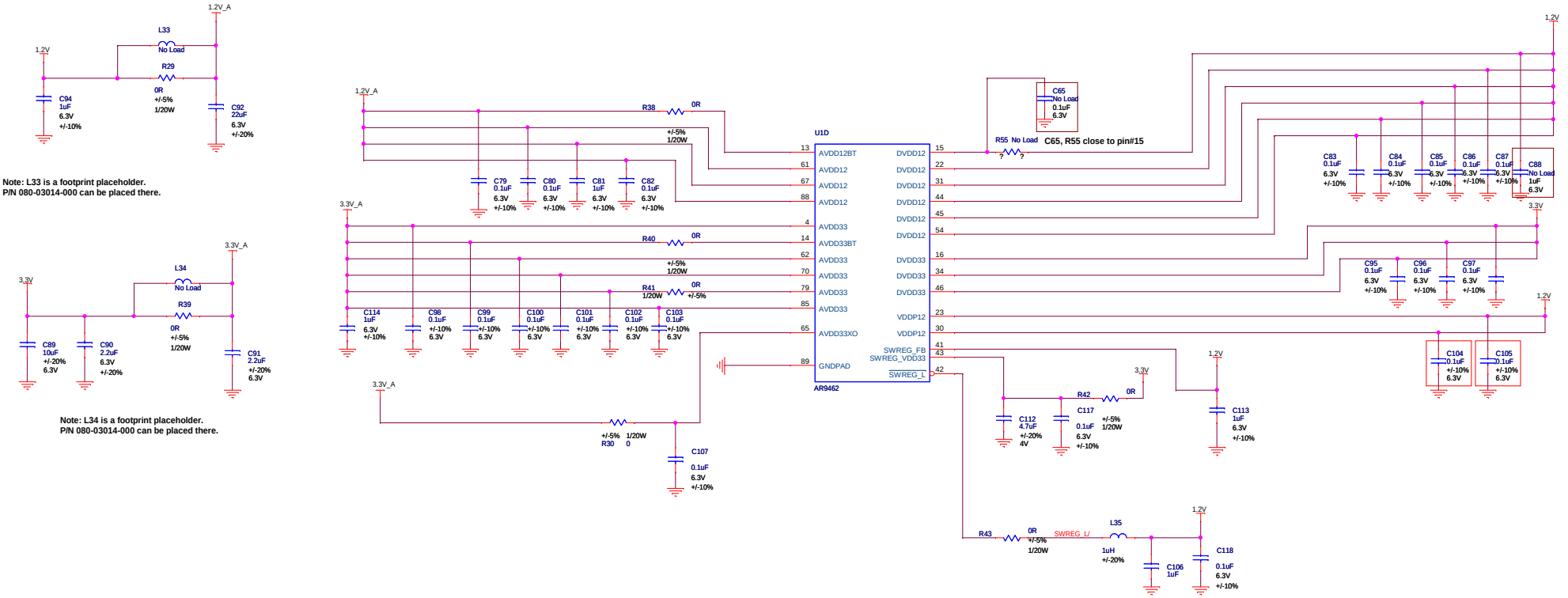
DIPLEXER



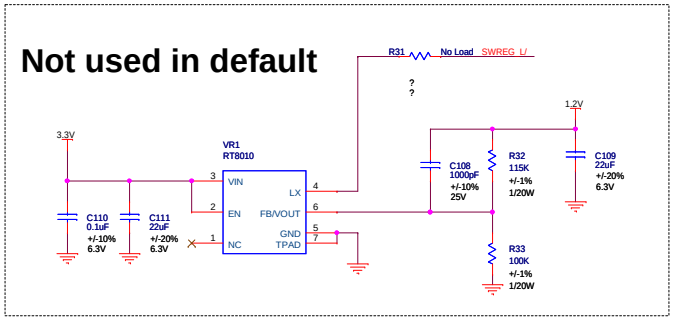
Switch Table
V1 (SWCOM1) = high ---> J4 to J1 (i.e. choose RX)
V2 (SWCOM2) = high ---> J5 to J1 (i.e. choose 2G TX)
V3 (SWCOM3) = high ---> J8 to J1 (i.e. choose 5G TX)

<Variant Name>

QUALCOMM ATHEROS 1700 TECHNOLOGY DRIVE SAN JOSE, CA 95110			TITLE Chain1		
DATE Friday, November 25, 2011	SIZE C	REV 072	SHEET 5 OF 6		DWG NO WB222-245-02062-072



Not used in default



Optional "External" Switching Regulator

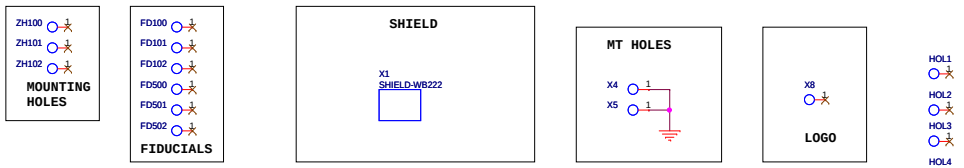
Notes:
To enable the Switching Regulator,
R31=0ohm.
R43=NL.

To bypass the Switching Regulator,
R31=NL.
R43=0ohm.
Do not unload C110, C111, or C109.

For Production,
VR1=C108=R31=R32=R33=NL.
R43=0ohm.
Do not unload C110, C111, or C109.

As shown, the switching regulator is loaded but bypassed.

PANEL



Qualcomm ATHEROS CONFIDENTIAL -- PRELIMINARY

<Variant Name>

Qualcomm ATHEROS QUALCOMM ATHEROS 1700 TECHNOLOGY DRIVE SAN JOSE, CA 95110				TITLE **Power_and_Misc**	
DATE Friday, November 25, 2011	SIZE C	REV 072	SHEET 6 OF 6	DWG NO **WB222-245-02062-072**	