RTX

Technical Documentation

Summit base

1 Document history

Description	Version	Responsible	Date
Initial document	V01	JW	02-06-2014
RF part updated	V02	KPE	10-02-2015

Table of Contents

2 Scope

This document serves as hardware documentation for the Summit base (FP). Summit is a new range of desktop devices including wireless capability between the base and the associated handset.

3 Base (FP) overview

The main goal of this project is to remove the cord between the handset and the base and implement a wireless connection using DECT. The base PCB is made as add on module to the AVAYA base main board. The interface connection between the main board and the base PCB is implemented using a 20-pin header with pitch 1,27mm.

3.1 Power supply

Power supply to the DECT base module is provided from the AVAYA base via the interface connector. The supply includes +3V3 for the SC14CVMDECT module, interface signals and +5V for the charging interface.

3.2 PCB

The design is based on conventional four layer PCB, without blind and buried via's. Components are only mounted on one side of the PCB to avoid extra cost in the mounting process.

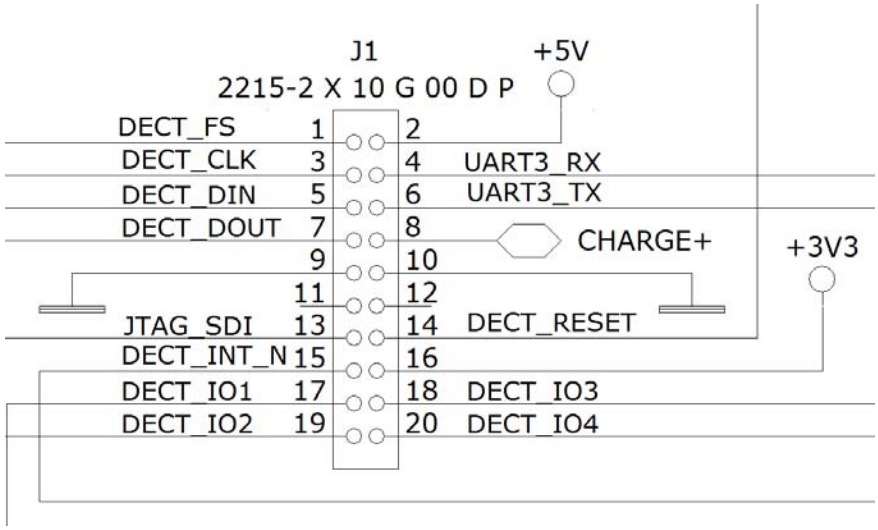
4 Summit base (FP) hardware.

4.1 DECT module

The main unit on the Summit base module is the cordless voice module from Dialog semiconductor type CVM DECT module (P.N. SC14CVMDECT SF01). The module contains a single chip package with integrated radio transceiver and baseband, program and parameter memory, voltage regulators, a 20.736MHz crystal and built-in antenna circuit (one antenna is integrated into the module. For additional information about the module please refer to the datasheet SC14CVMDECT SF01 Datasheet_xxx.pdf

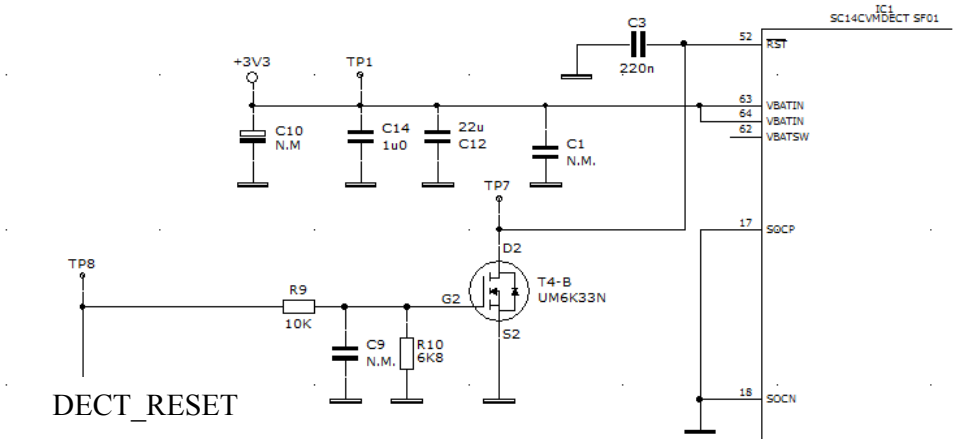
4.2 Main board interface

The base module is connected to the AVAYA main board using a 2 row 20 pin connector (2 x10 pins). This interface connector provides all necessary supply and control signals between the DECT base module and the main board. Since the AVAYA main board is implemented using +3V3 logic and the DECT base module +1V8 logic it is necessary to implement logic level shifting on the control signals between the two boards.



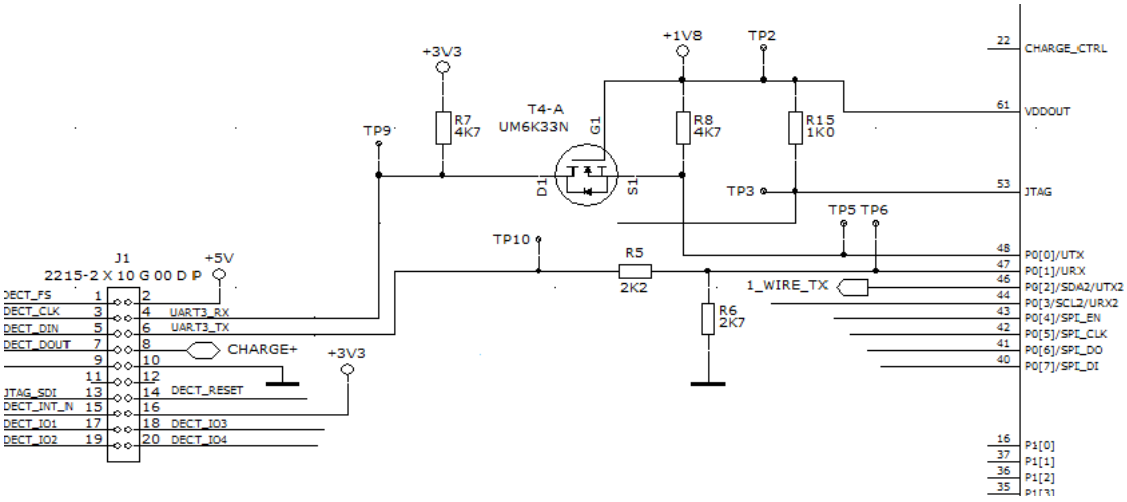
4.2.1 Reset control

A small circuit is implemented to enable external reset of the SC14CVMDECT module from the AVAYA main board. An external reset is provided by setting the signal DECT_RESET (TP8) too high for at least 15µS while the module is in active mode. A voltage divided formed by to resistors is inserted to avoid reset if small spikes would occur on the DECT_RESET input.



A logic high +3V3 signal on the DECT_RESET will drive the gate on T4 above the threshold level and short the capacitor C3 to GND. A low level on the /RST pin will reset the SC14CVMDECT module and keep the module in reset condition until asserting the DECT_RESET low again.

4.2.2 UART interface



Description of TX (UART3_RX) level shift operation:

UTX = high (+1V8) – Gate and source on T4 are both at +1V8 level, V(gate-source) is below threshold voltage and T4 is not conducting. In this state the UART3_RX signal is pulled up by its pull-up resistor R7 to +3V3.

UTX = low (0V) – The source of T4 is asserted low, while the gate stay at +1V8. V(gate-source) rises above the threshold voltage and T4 becomes conducting. . In this state the UART3_RX signal is pulled low via the conducting FET T4. Both signal lines low at the same voltage level.

Description of RX (UART3_TX) level shift operation:

The level shifting on the UART receive signal (URX) is implemented using a voltage divider:

UART3_TX = high (+3V3) – The input voltage on the URX pin after the voltage divider is 3,3 x (2K7/(2K7 + 2K2)) = 1,82V

UART3_TX = low (0V) – The input voltage on the URX pin after the voltage divider is 0V

4.2.3 PCM interface

Digital audio interface between the AVAYA main board and the Summit BS is implemented using the PCM interface, where the AVAYA main board is master and the Summit BS is slave.

Interface signals:

DECT_FS: Frame strobe signal 8 or 16 kHz (input).
DECT_CLK: PCM clock (input).
DECT_DI: PCM data in (input).
DECT_DOUT: PCM data out (output).

The setting of the PCM interface is done from the AVAYA main board using API commands over the serial interface.

4.2.4 Spare signals

The interface connector between the Summit BS and AVAYA main board is provided with five spare signals. These signals are currently not in use and are provided as spare signals if it should become necessary. One of the signals is however reserved as an interrupt for the Summit BS to be able to signal to the main board.

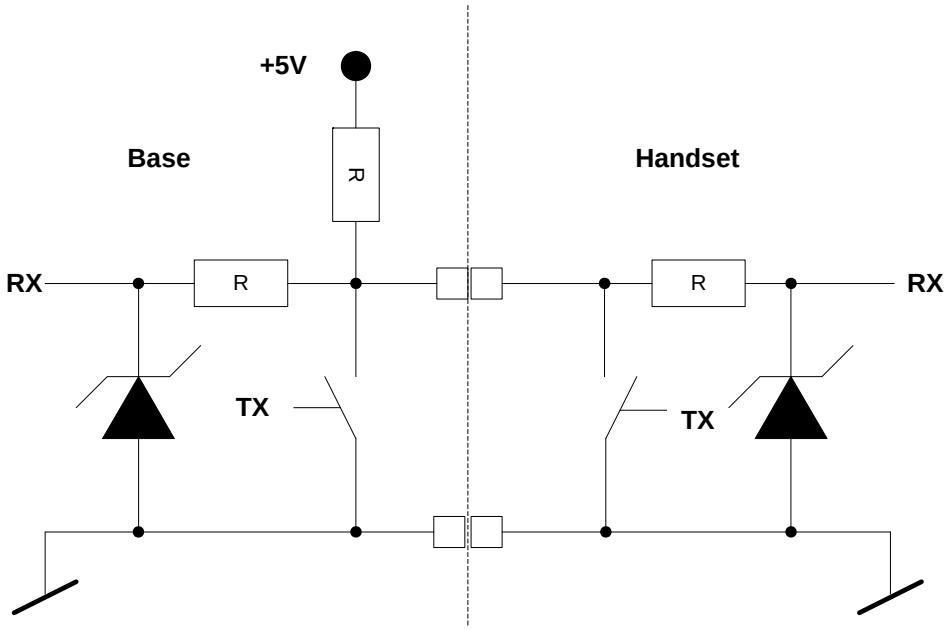
Spare signals:

DECT_INT_N (reserved as interrupt output from the Summit BS – no pull up)
DECT_IO1 (Spare – pull up to +3V3)
DECT_IO2 (Spare – pull up to +3V3)
DECT_IO3 (Spare – pull up to +3V3)
DECT_IO4 (Spare – pull up to +3V3)

All these signals are as default initialized as back-drive protected on the DECT module. This set-up allows interfacing with signals up to 3,45V. The DECT_IO1 to 4 signals are all provided with an external pull-up resistor to +3V3 while the DECT_INT_N signal expect the pull-up resistor to be placed on the AVAYA main board.

4.3 1-Wire interface

Registration information between the Summit base and handset is provided over a 1-wire interface. This 1-wire interface is implemented using the positive charge terminals as communication path for receiving and transmitting data between base and handset.



The drawing above shows a simplified diagram of the 1-wire communication interface between the base and handset.

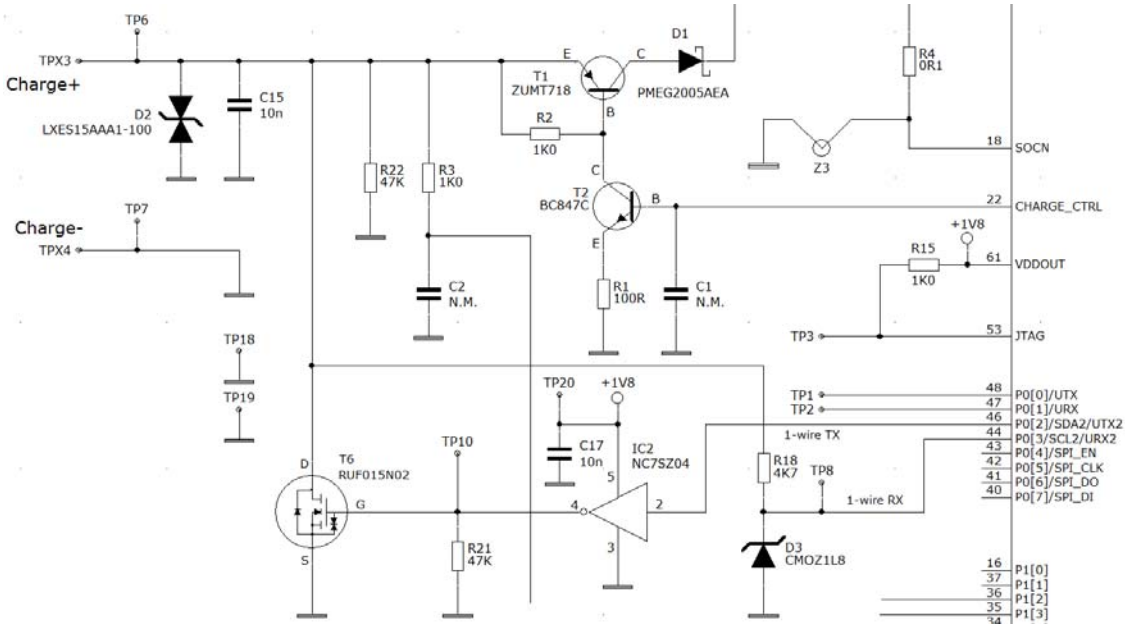
In both base and handset the 1-wire communication is implemented using the UART2 interface block.

TX = UTX2
RX = URX2

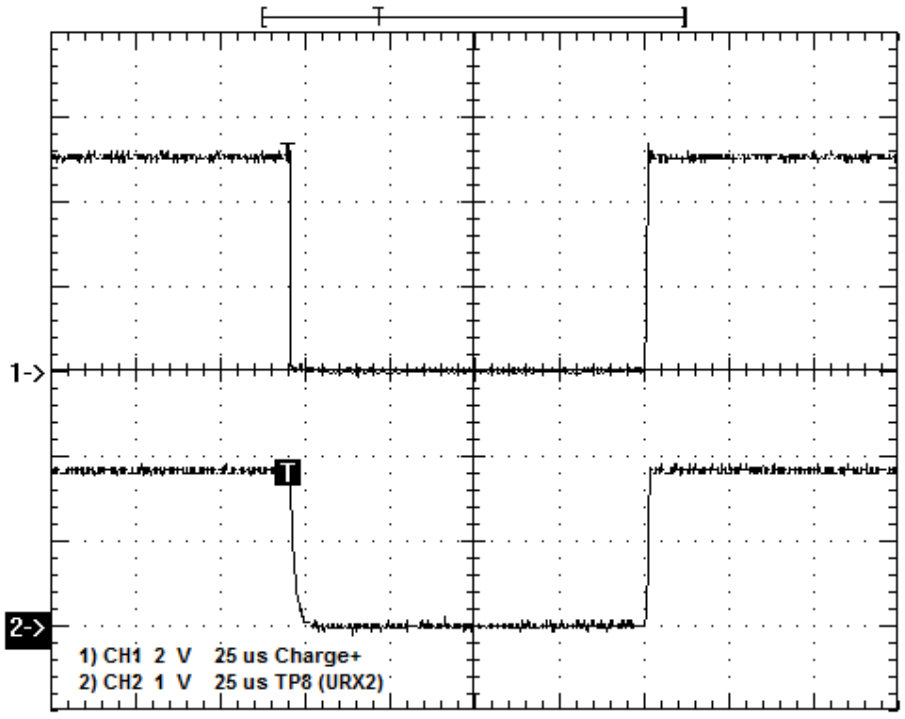
With this implementation it is possible to use the internal UART hardware block in the DECT processor as control unit for the serial communication. This implementation will limit the load on the DECT processor compared to an implementation when the signal lines are controlled by general purpose ports.

When placing the handset in the charging cradle, voltage is applied to the Charge+ terminal. This charging voltage is detected by the handset using the charge input on the module (IC1 pin 23/Charge). The handset can now start to communicate with the base using the 1-wire interface. When closing the TX switch the 1-wire line is pulled to low level, while opening the switch again will drive the 1-wire interface to high level. Since a high level on the gate of FET T6 will pull the line low it is necessary to add an inverter (IC2) between the UTX pin and the T6 gate to ensure same the polarity on the UART (TX) and the 1-wire interface.

Since there is only one line for communication it is necessary to implement some kind of time sharing in the SW to ensure that the two units is not communication at the same time. When placed in the cradle the Summit handset starts to send information over the 1-wire interface to the base.



Both data send from the handset itself and data returned from the base is clocked into the receive part of the serial interface (URX2). Since the voltage level on the charge+ line can be anywhere between 0V to 5V it is necessary to have some kind of limitation on the 1-wire RX to protect the input pin (URX2) against overvoltage (voltage above recommended maximum input voltage). This is implemented using the zener diode D3 with 1,8V zener voltage in series with the resistor R18. The zener diode will limit voltages above the zener voltage to ensure that the level applied to the URX2 pin is inside the safe operating area.



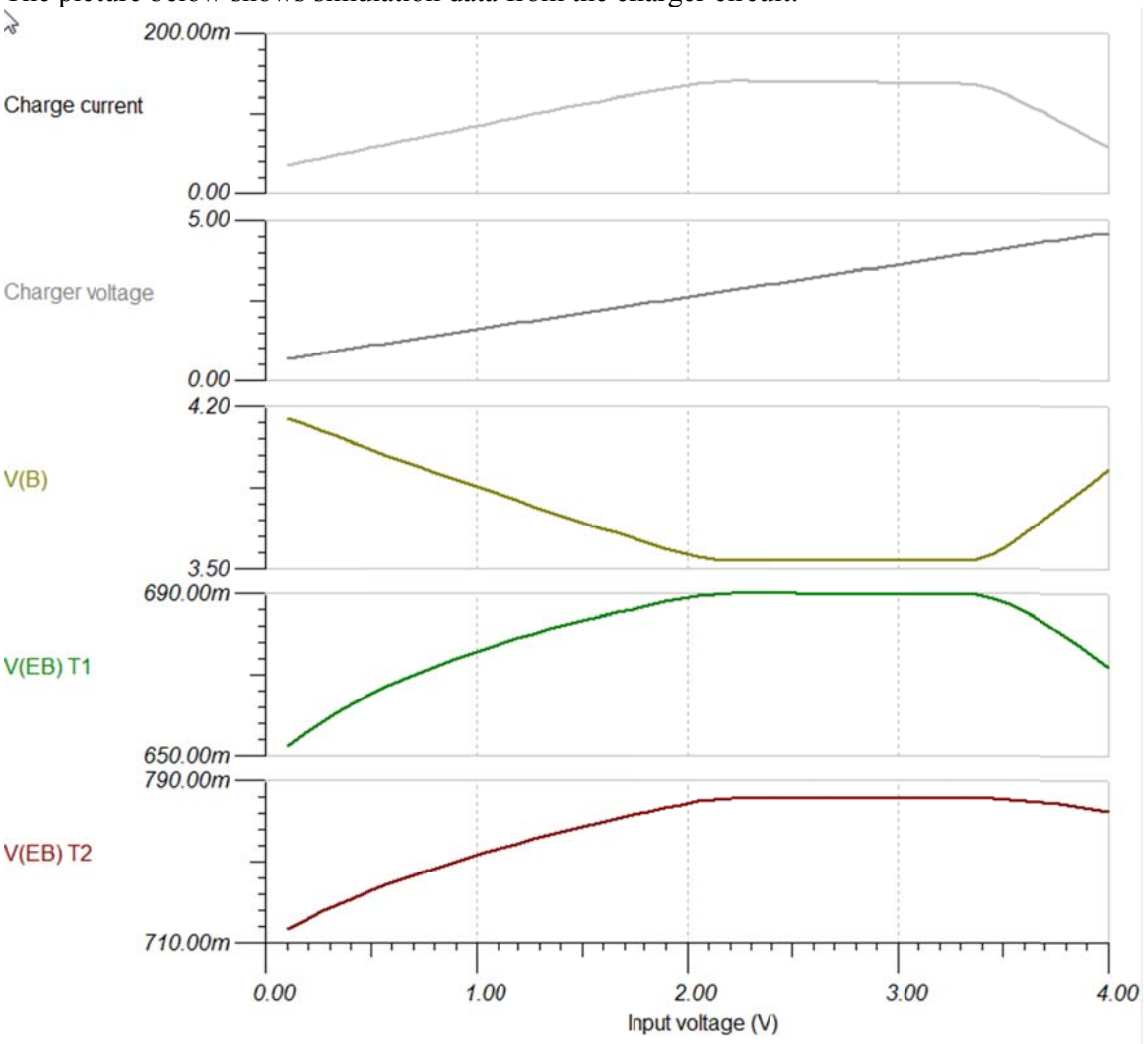
The picture above show the signal levels on the charge+ input and on the UART receive input pin (UART2). In high state the voltage level on the charge+ input is as high as 5V while the input voltage level on UART2 receive input is about 1,8V. This limitation in voltage is as mentioned implemented using the zener diode D3 in series with resistor R18.

The logic 1 input level for the UART2 input should be minimum 1,26V while maximum operating voltage on the pin is 1,98V.

4.4 Charger circuit

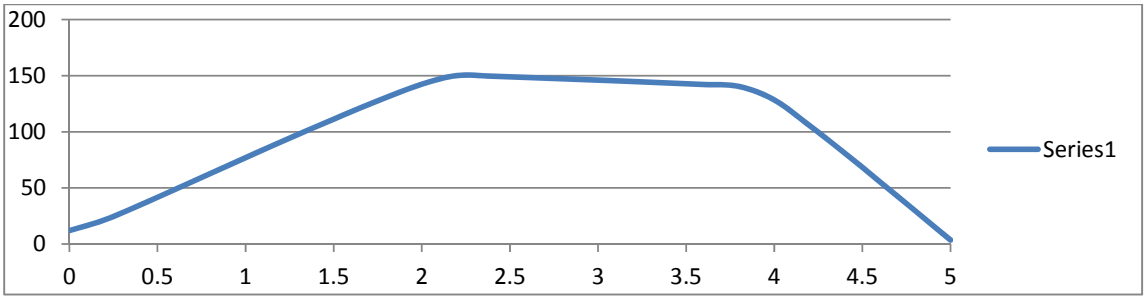
The charging circuit in the Summit base is built around a current mirror. The idea with this current mirror and the surrounding circuit is to provide a constant charging current in the normal battery charging voltage range as well as to provide very low output current when the battery terminals is shorted due to the 1-wire communication between the base and the handset. Since the base (B) on the two transistors T1 and T2 are tied together, the voltage at this point is the same. The charge current can be calculated as +5V- T2 $V_{EB} - V_B$ divided by the parallel value of R3 and R4.

The picture below shows simulation data from the charger circuit:



Charge current: Output current from charger
Charger voltage: Voltage on base charger terminals
V(B): Base to GND voltage on T1 and T2
V(EB) T1: T1 emitter base voltage
V(EB) T2: T2 emitter base voltage
Input voltage (V): Voltage across batteries in the Summit handset.

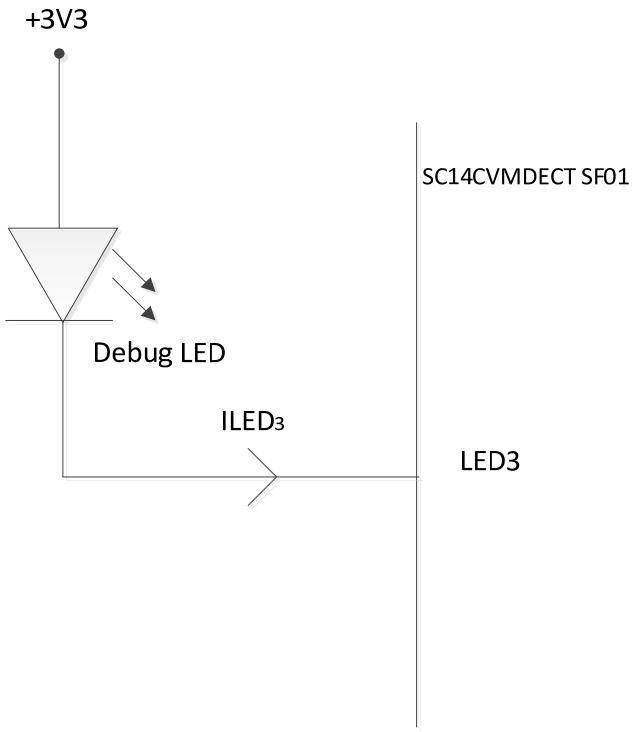
The picture above show simulated voltage and current levels at different points in the charger circuit. The horizontal axis (input voltage) simulates the voltage across the two AAA battery cells in the Summit handset, while the Charger voltage curve show the voltage on the Summit base charging terminals. The simulation data show that the charging current is fairly linear at approximately 150mA from 2,2V up to about 3,5V across the batteries. The output current from the charger is reduced linear at voltages from 2,2V down to 0V and from about 3,5V up to 5V. Especially the low output current at 0V is important when communicating over the 1-wire interface. Logic 0 on the 1-wire interface is generated by pulling the charger voltage to GND using the FET T5 on the base PCB or T6 on the handset PCB. In this state the charger will limit the current to about 12mA, reducing the power dissipation in the FET transistors.



The above curve shows a practical measurement on the Summit base charger circuit. The charger voltage and current is monitored in steps of 0,2V from 0V up to 5V. The curve from the practical measurement is very similar to the curve generated from the simulation tool.

4.5 Debug LED

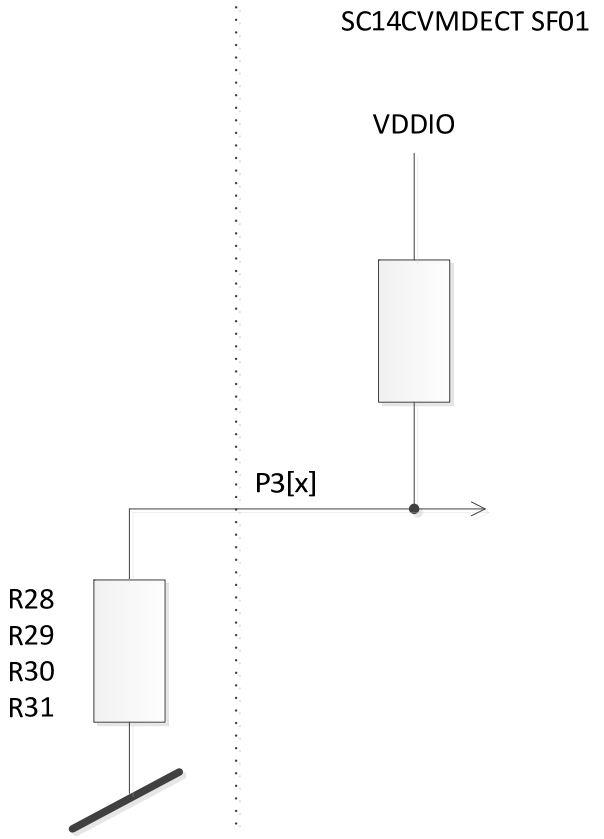
As debug notification the base is equipped with one green side view LED. The LED is controlled by a current sources available on the DECT module pins P2[0]/PWM0/LED3 (connected to LED cathode). This port is back-drive protested and can handle up to 3,45V. The LED current (ILED) can via internal registers be programmed to 2,5mA, 5mA or 10mA.



The anode of the LED is connected to the +3V3 power supply.

4.6 HW version control

The hardware version control can set the handset to 16 different version numbers using the four resistors R28, R29, R30 and R31. Internal pull-up in the DECT processor will ensure that the input pin is high when the external resistors are not mounted.

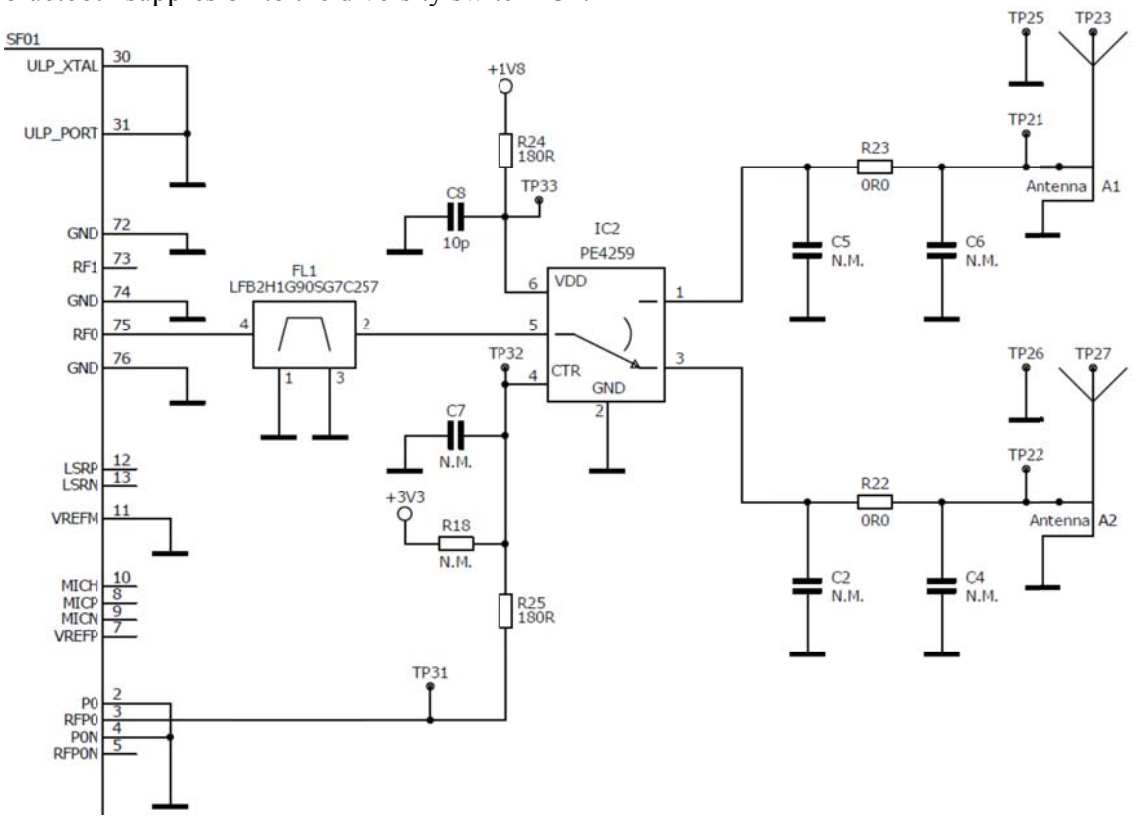


The reason for using 2K2 resistors as external pull-down instead of 0Ω is that the ports in this case can be used as output ports during for example debug without drawing more current out of the port than maximum rating.

4.7 RF interface

P0 and P0n is used on the SC14CVMDECT SF01 module, to allow the use of two external antennas.

The RF path is from pin RF1 on the module, though the ceramic filter (FL1) with WiFi and bluetooth suppresion to the diversity switch IC2.



RFP0 is used to select antenna and is also used to switch antennas during fast antenna diversity. C2, R22 and C4 is optional antenna match for antenna A2, while C5, R23 and C6 is optional antenna match for antenna A1.

TP23 and TP25 should be shorted with as short connection as possible in production, because this will improve the RF measurements done at TP21. The same apply to TP26 and TP27 for RF measurements on TP22.