RTL8763B Series

RTL8763BM, RTL8763BF, RTL8763BFR, RTL8763BS, RTL8763BA

BLUETOOTH 5 DUAL MODE SOC

PRELIMINARY DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 0.95
14th, FEB 2018
Track ID: JATR-8275-15

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface.
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
0.92	2017/11/14	Preliminary Release.

Revision	Release Date	Summary
0.93	2017/12/7	1. Change AUXLDO/VDDIO spec 2. Correct block diagram, AUXIN and MIC2 3. Correct BF pin ordering in pin description 4. Update the reference circuit, correct the UART RX/TX
0.94	2017/12/14	Correct power tree diagram Figure.2
0.95	2018/2/14	1. Update pin description 2. Update I2S timing diagram 3. Update reference circuit 4. Update current consumption number

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1. General Description

The RT8763B series are single-chip Bluetooth ROM audio solutions for mono (RTL8763BM) and stereo (RTL8763BF/BFR, RTL8763BS, RTL8763BA) applications. The RT8763B is composed of an ARM core and an ultra-low power DSP core with high efficiency computing power, high performance audio codec, power management unit, ADC, ultra-low current RF transceiver, and smart I/O distribution controller.

The parameter configuration tools, the EVB kits, and the MP kits, including controller hardware and software, provide a simple and flexible procedure for customers to quickly design and proceed to mass production with Realtek's new generation of audio solutions. These complete total solutions provide a fast and highly reliable development path with a very competitive R-BOM.

2. Features

General Features

- Bluetooth 5 specification compliant
- Supports HFP 1.7, HSP 1.2, A2DP 1.3, AVRCP 1.6, SPP 1.2 and PBAP 1.0
- Single-end RF radio output with high performance 10dBm of transmitter power and -94dBm 2M EDR receiver sensitivity
- Supports Bluetooth classic (BDR/EDR)
- Supports Bluetooth Low Energy (BLE)
  - Generic access service
  - Device information service
  - Proprietary services for data communication
  - Apple Notification Center Service (ANCS)
- Real Wireless Stereo (RWS)
- Supports USB type-C audio
- Supports iAP2
- Realtek's latest RCV (Real Clear Voice) technology for narrowband and wideband voice connection, including wind noise reduction
- Supports high resolution audio codec up to 24bits, 192kHz audio data format
- Supports dual analog and digital MIC, AUX-IN, I2S digital audio, analog output
- Supports high speed UART, I2C, SPI and USB2.0 compatible interface
- Supports high resolution 12-bits multi-channel ADC
- Supports PWM I/O and smart LED controller
- Supports USB BC1.2 battery charging
- Smart I/O distribution scheme with MUX
- Built-in 8Mbits FLASH memory (RTL8763BF/RTL8763BFR)
- Integrated dual switch mode power regulator, linear regulators, and battery charger; charging current up to 400mA
- Built-in battery voltage monitoring and thermal protection scheme with external thermal resistor
- SBC, AAC decoder support
- Package: 5x5mm^2 QFN40 (RTL8763BM, RTL8763BF, RTL8763BFR), 6x6mm^2 QFN48 (RTL8763BS) and 8x8mm^2 QFN68 (RTL8763BA) with 0.4mm pitch
- Supports OTA and USB firmware upgrade
- GSM 217Hz interference block out design
- Low BOM cost
- Green (RoHS compliant and no antimony or halogenated flame retardants)
- Supports PTA (Packet Traffic Arbiter) when co-existing with Wi-Fi

Baseband Features

- 40MHz main clock
- Supports serial flash for FW storage and parameter upgrade
- Adaptive Frequency Hopping (AFH)
- Multi-link support
- Supports Serial Copy Management System (SCMS-T) content protection

RAM and ROM Size

- ROM size 768KB
- MCU RAM size 16KB x 8 Data RAM + 8KB X 2 cache RAM
- DSP RAM 8KB x 22

RF

- Supports TX +10dBm (typ.) maximum output power for Bluetooth classic
- Supports TX +10dBm (typ.) maximum output power for Bluetooth BLE
- Supports TX +4dBm (typ.) maximum output power for Bluetooth BLE low power TPM mode
- Receive sensitivity: -94dBm (2Mbps EDR)
- Receive sensitivity: -97dBm (BLE)
- Receiver sensitivity: -106.5dBm (125K BLE long range)
- Single-end TX/RX RF port without matching component required (when TX power is below +4dBm and using PIFA type PCB antenna)
- Crystal oscillator with built-in integrated capacitor for clock offset digital tuning (0~20pF), could save 2-compensation CL cap following Realtek design guidelines

MCU

- 32-bit ARM Cortex-M4F Processor
- Supports hardware Floating Point Unit (FPU)
- Supports Memory Protect Unit (MPU)
- Supports SWD debug interface
- Executed external SPI flash
- 4-way association cache controller

DSP Audio Processing

- Enhanced Tensilica Hi-Fi-mini compatible 24-bit DSP core
- 2 single-cycle MACs: 24 x 24-bit multiplier and 56-bit accumulator
- Supports G.711 A-Law, μ-Law, continuous-variable-slope-delta (CVSD) and mSBC voice codecs
- Supports 8/16 kHz 1/2-mic noise suppression and echo cancellation
- Packet Loss Concealment (PLC) for voice processing
- SBC, and AAC-LC audio codecs supported for BT audio streaming

Audio Codec

- Dual operation voltage range 2.8V and 1.8V
- Supports cap-less, single-ended, and differential mode at the DAC path
- Supports 16ohm and 32ohm speaker loading
- Stereo 24-bit digital-to-analog (DAC) with 102dBA SNR
- Stereo 24-bit analog-to-digital (ADC) with 97dBA SNR
- 5-band configurable EQ at both DAC/ADC paths
- Sampling rates of 8, 16, 32, 44.1, 48, 88.2, and 96kHz are supported.
- Built-in MIC bias generator

Digital Audio Interface

- Supports two PDM digital MIC inputs
- Supports 24-bit, 192kHz on I2S digital audio
- Sampling frequency 8/16/32/44.1/48/88.2/96/176.4/192kHz

Radio

- Compliant with Bluetooth Core Specification including BR/EDR/LE-1M/LE-2M/LE-Coded (LongRange)
- Fully integrated balun and synthesizer minimizes external components.
- RF circuit design minimizes power-consumption while keeping excellent performance

PMU

- Highly integrated PMU design for the system application

- Dual switching mode regulator for digital core, radio and audio codec respectively
- Built-in LDO for the I/O and FLASH memory
- Built-in Li-Ion battery charger with up to 400mA charger current capability
- Supports ambient thermal detection to detect the battery temperature
- Built-in OVP, OCP, UVP protection to protect the system.

Operating Condition

- Operating voltage: 2.8V to 4.35V (VBAT)
- Temperature range: -40℃ to +85℃

Package

- 5mmx5mm, QFN40 package (RTL8763BM)
- 5mmx5mm, QFN40 package (RTL8763BF/BFR)
- 6mmx6mm, QFN48 package (RTL8763BS)
- 8mmx8mm, QFN68 package (RTL8763BA)

3. System Applications

- Mono headset
- Stereo headset
- Real Wireless Stereo (RWS) headset
- Mono speaker
- Stereo speaker

4. Block Diagram

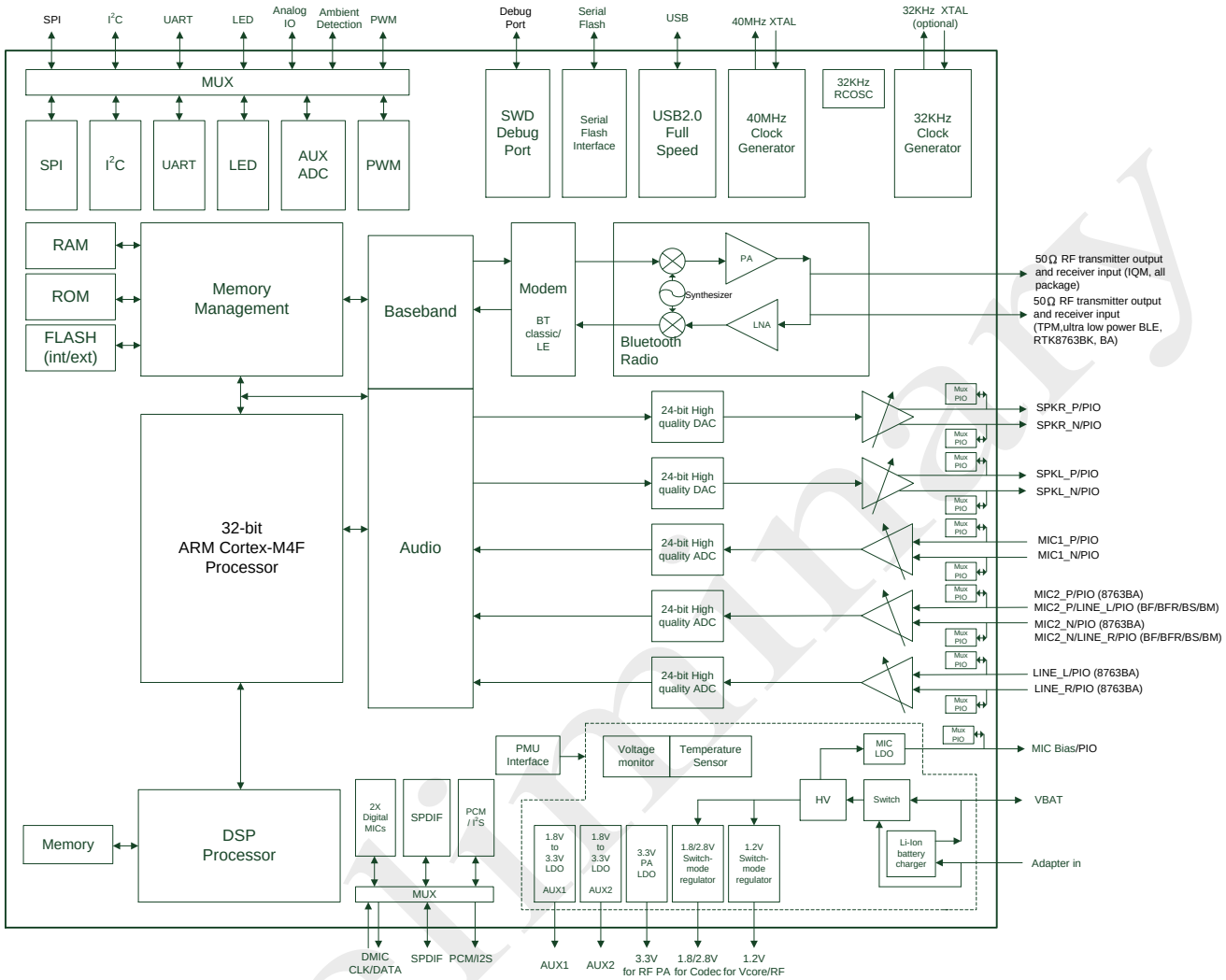

Figure 1. Block Diagram

5. Power Tree

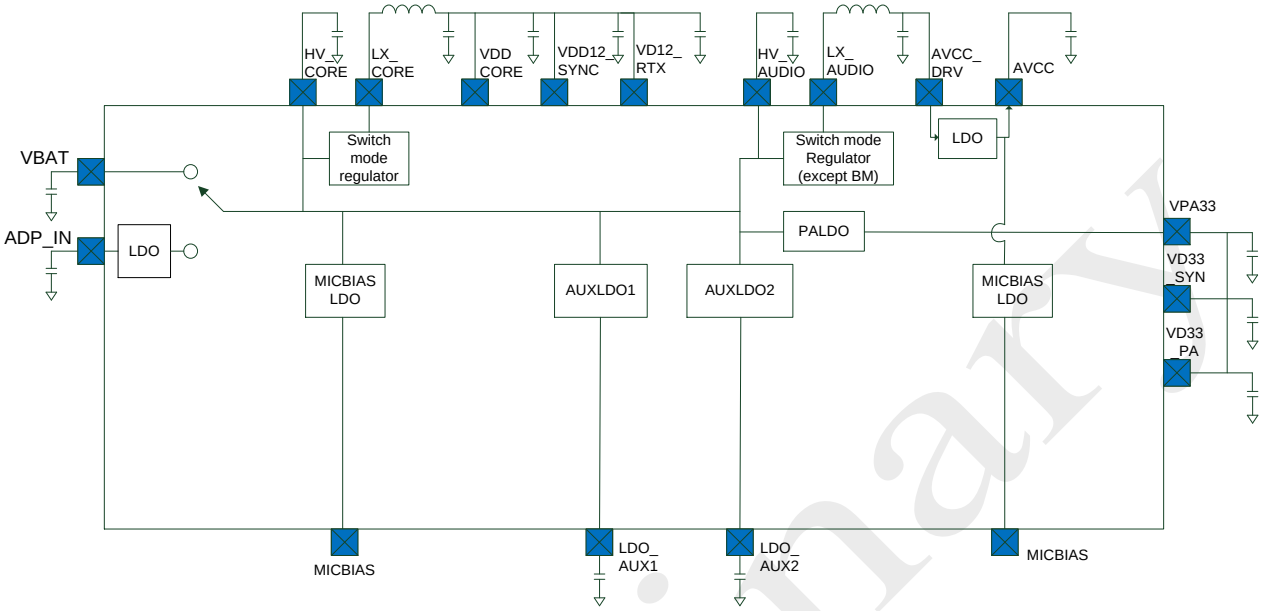

Figure 2. Power Tree-1

6. Pin Assignments

6.1. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 4). The version is shown in the location marked 'V'.

Figure 3. Package Identification

6.2. PIN OUT (TOP View) RTL8763BM QFN40

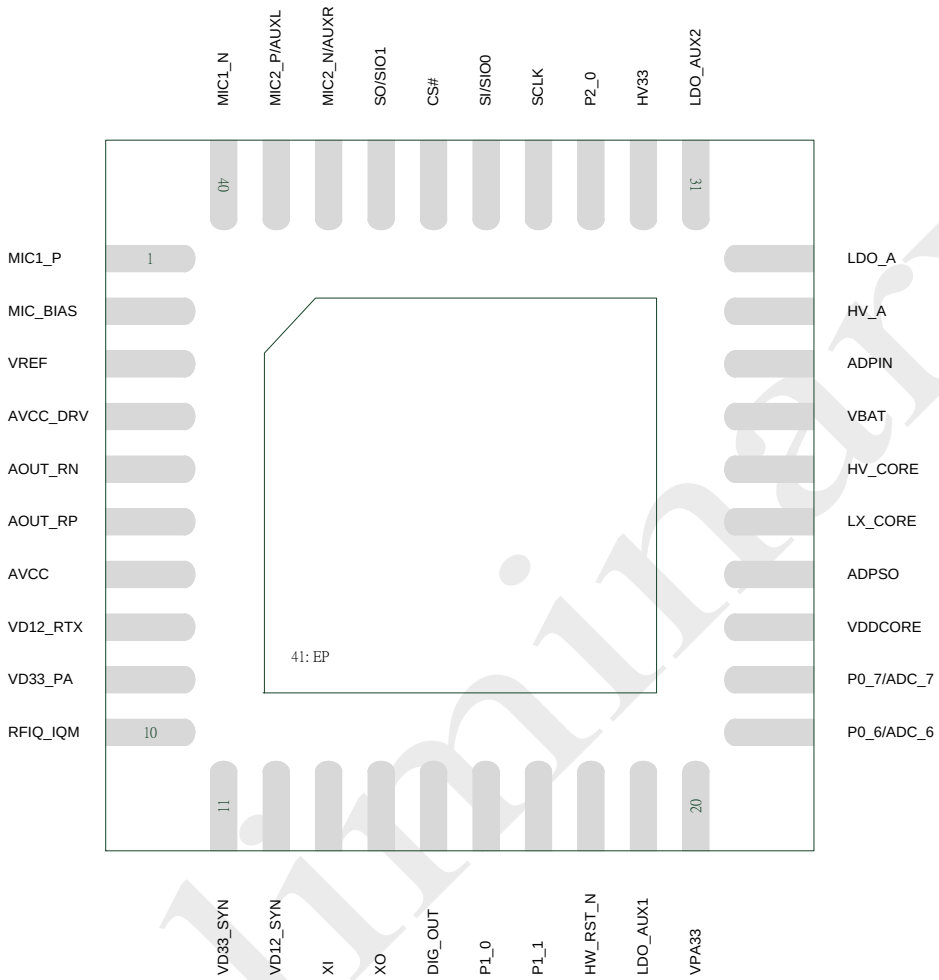

Figure 4. PIN OUT (TOP View) RTL8763BM QFN40

6.3. PIN OUT (TOP View) RTL8763BF/BFR QFN40

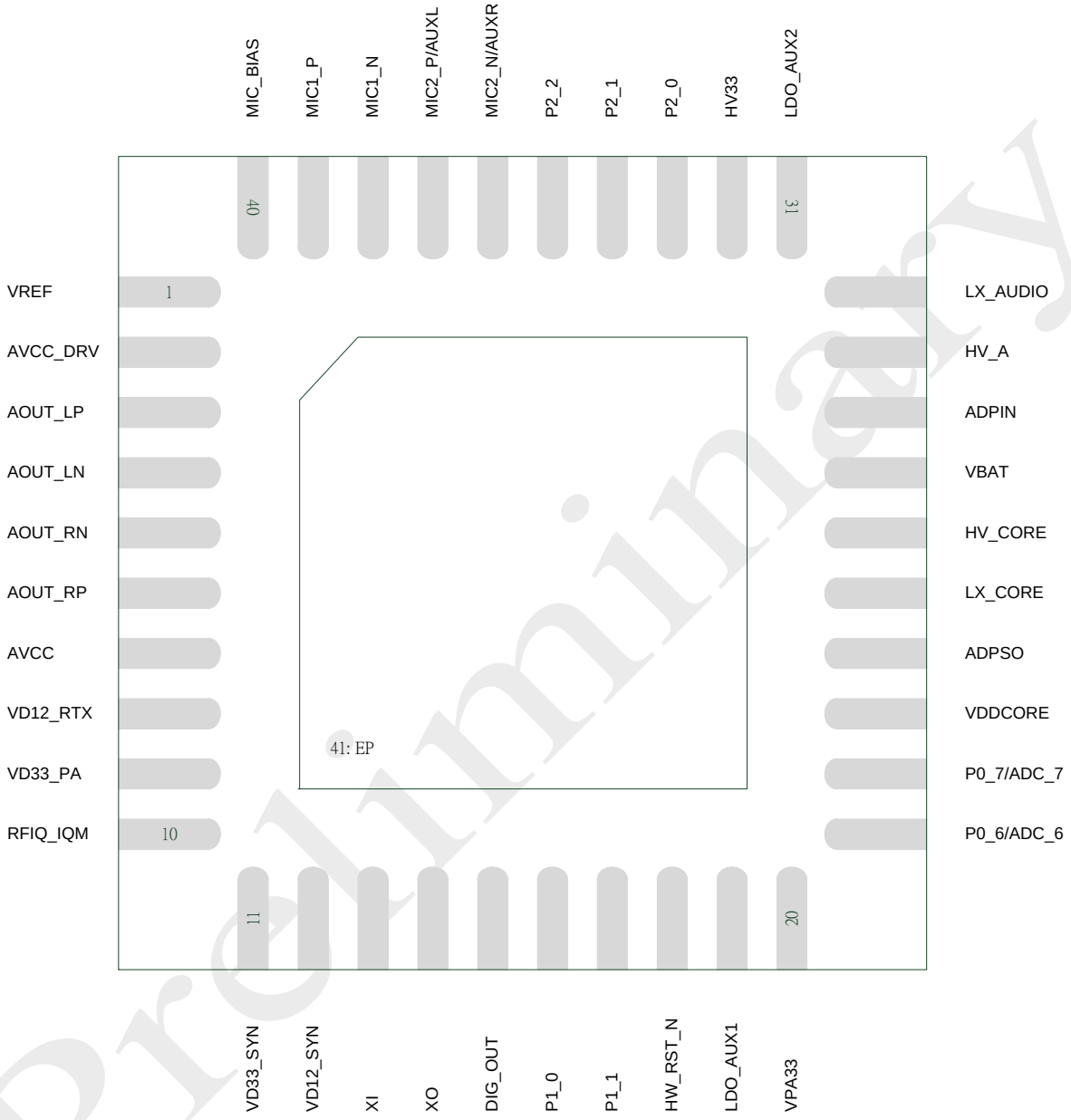

Figure 5. PIN OUT (TOP View) RTL8763BF/BFR QFN40

6.4. PIN OUT (TOP View) RTL8763BS QFN48

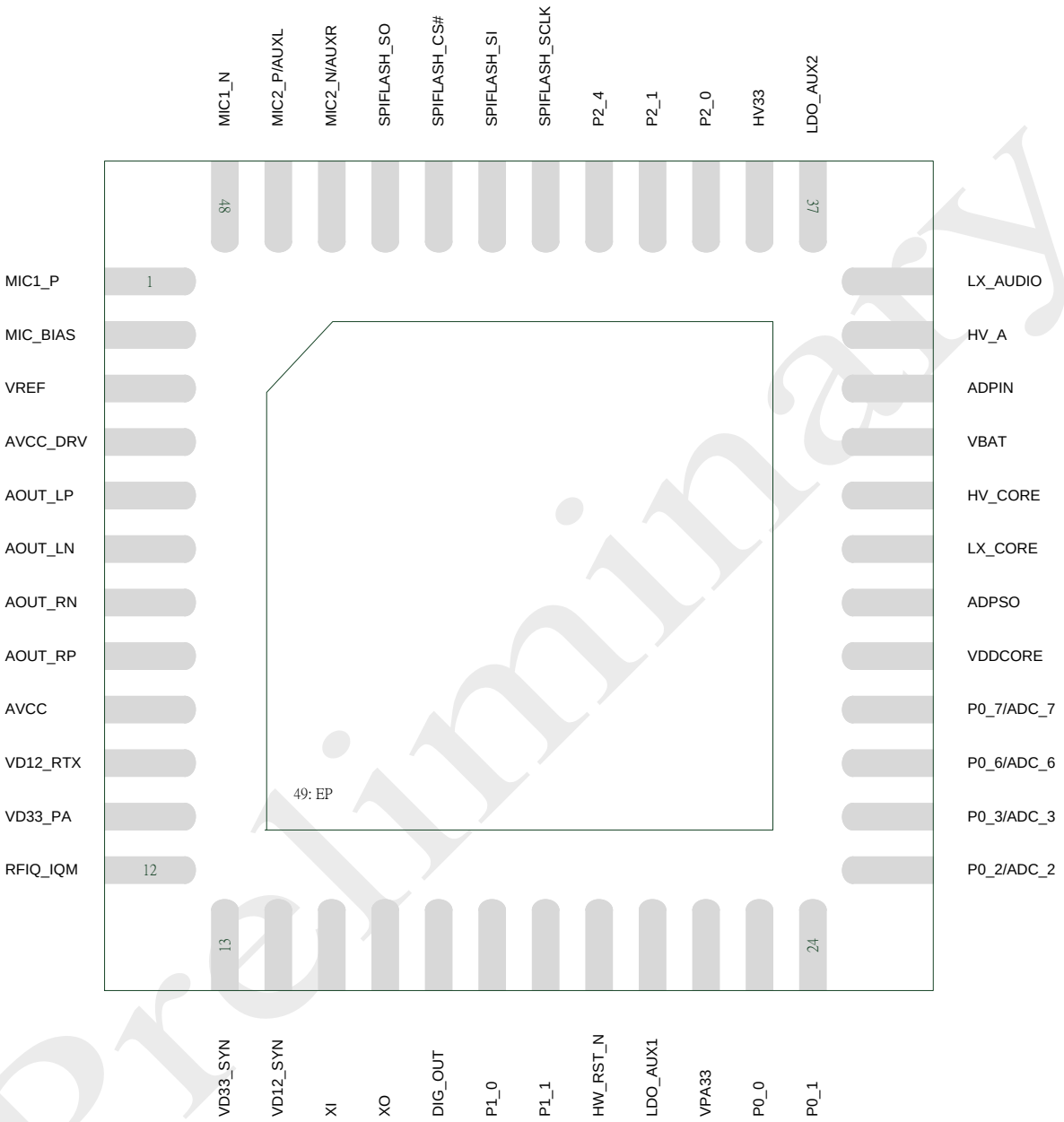

Figure 6. PIN OUT (TOP View) RTL8763BS QFN48

6.5. PIN OUT (TOP View) RTL8763BA QFN68

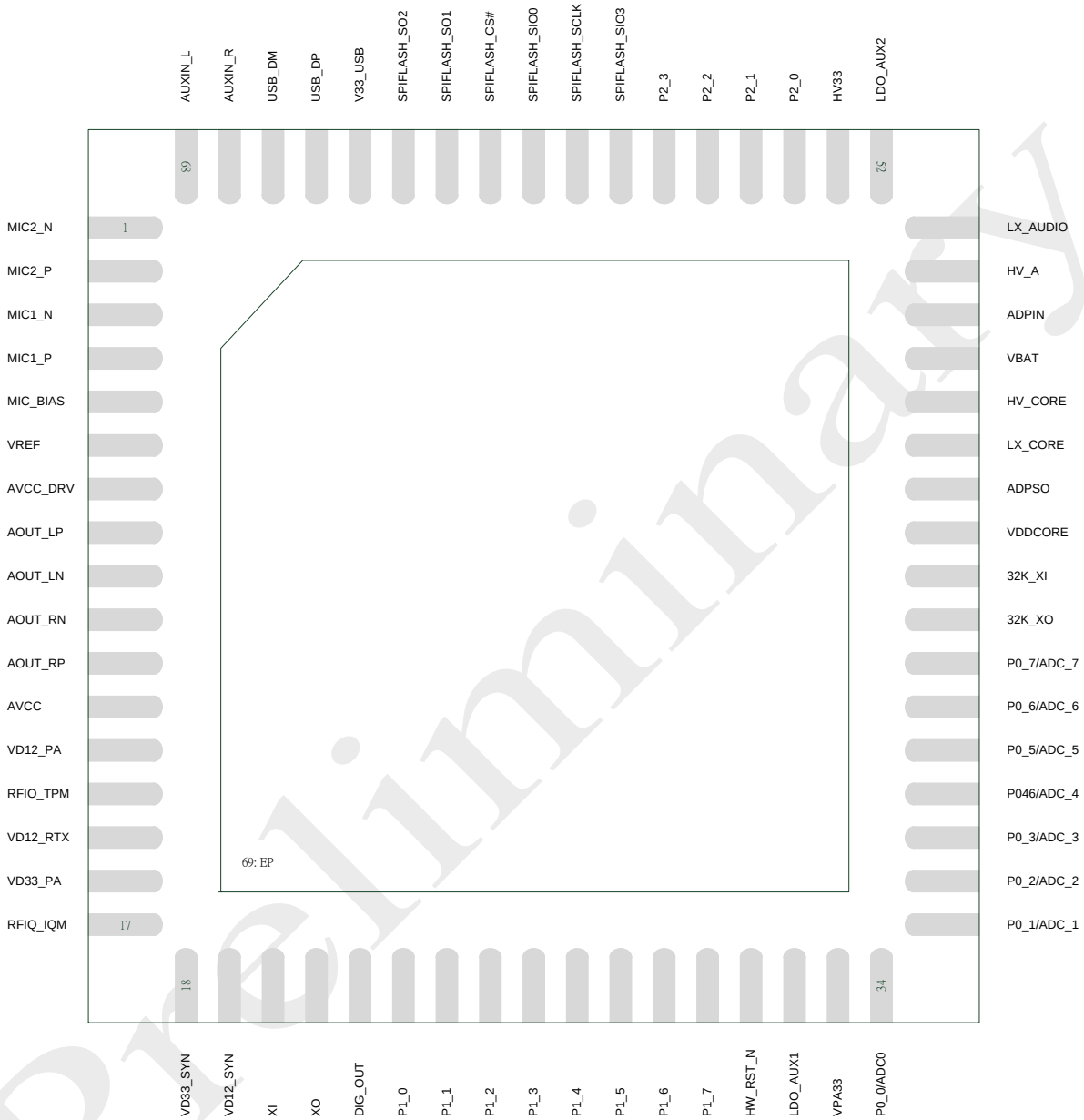

Figure 7. PIN OUT (TOP View) RTL8763BA QFN68

7. Pin Descriptions

7.1. RF Interface

Table 1. RF Interface

Pin Name	Pad Type	RTL 8763BM	RTL 8763BF/ BFR	RTL 8763BS	RTL 8763BA	Description
RFIO_IQM	RF	10	10	12	17	Bluetooth radio 50Ω transmitter output and receiver input (dual mode)
RFIO_TPM	RF	-	-	-	14	Bluetooth radio 50Ω transmitter output and receiver input (BLE)

7.2. Crystal Oscillator

Table 2. Crystal Oscillator

Pin Name	Pad Type	RTL 8763BM	RTL 8763BF/ BFR	RTL 8763BS	RTL 8763BA	Description
XI	A	13	13	15	20	Crystal input
XO	A	14	14	16	21	Crystal output

A: Analog

7.3. General Purpose I/Os

Table 3. General Purpose I/Os

Pin Name	Pad Type	RTL 8763BM	RTL 8763BF/ BFR	RTL 8763BS	RTL 8763BA	Description
P0_0/ADC_0	I/O I/O A	-	-	23	34	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P0_1/ADC_1	I/O I/O A	-	-	24	35	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P0_2/ADC_2	I/O I/O A	-	-	25	36	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P0_3/ADC_3	I/O I/O A	-	-	26	37	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain

Pin Name	Pad Type	RTL 8763BM	RTL 8763BF/ BFR	RTL 8763BS	RTL 8763BA	Description
P0_4/ADC_4	I/O I/O A	-	-	-	38	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable
P0_5/ADC_5	I/O I/O A	-	-	-	39	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P0_6/ADC_6	I/O I/O A	21	21	27	40	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P0_7/ADC_7	I/O I/O A	22	22	28	41	Programmable GPIO. Can be programmed as ADC input pin Pull high/low input configurable Belongs to LDO_AUX1 domain
P1_0	I/O	16	16	18	23	Programmable GPI O Pull high/low input configurable Belongs to LDO_AUX1 domain
P1_1	I/O	17	17	19	24	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain
P1_2	I/O	-	-	-	25	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain
P1_3	I/O	-	-	-	26	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain
P1_4	I/O	-	-	-	27	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain
P1_5	I/O	-	-	-	28	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain
P1_6	I/O	-	-	-	29	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain
P1_7	I/O	-	-	-	30	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX1 domain
P2_0	I/O	33	33	39	54	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain HCI mode selection H: APP mode L: HCI mode

Pin Name	Pad Type	RTL 8763BM	RTL 8763BF/ BFR	RTL 8763BS	RTL 8763BA	Description
P2_1	I/O	-	34	40	55	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain
P2_2	I/O	-	35	-	56	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain
P2_3	I/O	-	-	-	57	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain
P2_4	I/O	-		41	-	Programmable GPIO Pull high/low input configurable Belongs to LDO_AUX2 domain

I/O: Bidirectional digital pad

I/O PU: Bidirectional digital pad with pull high resistor inside when input mode

I/O PD: Bidirectional digital pad with pull low resistor inside when input mode

I/O A: Bidirectional digital pad and programmable ADC

7.4. Audio Codec

Table 4. Audio Codec

Pin Name	Pad Type	RTL 8763BM	RTL 8763BF/ BFR	RTL 8763BS	RTL 8763BA	Description
MIC1_N	AH	40	38	48	3	MIC1 input negative pad. Used as main MIC in dual MIC application. Programmable digital I/O, refer to MUX table, belongs to AVCC domain
MIC1_P	AH	1	39	1	4	MIC1 input positive pad. Used as main MIC in dual MIC application. Programmable digital I/O, refer to MUX table, belongs to AVCC domain
MIC2_N	AH	-	36(*)	46(*)	1	MIC2 input negative pad. Used as 2nd MIC in dual MIC application. Programmable digital I/O, refer to MUX table (*) AUX input right channel pad. Programmable digital I/O, refer to MUX table, belongs to AVCC domain

MIC2_P	AH	-	37(**)	47(**)	2	MIC2 input positive pad. Used as 2nd MIC in dual MIC application. Programmable digital I/O, refer to MUX table (**) AUX input left channel pad. Programmable digital I/O, refer to MUX table, belongs to AVCC domain
SPKR_N	AH	5	5	7	10	Right channel speaker output negative Programmable digital I/O, refer to MUX table, belongs to AVCC_DRV domain
SPKR_P	AH	6	6	8	11	Right channel speaker output positive Programmable digital I/O, refer to MUX table, belongs to AVCC_DRV domain
SPKL_N	AH	-	4	6	9	Left channel speaker output negative Programmable digital I/O, refer to MUX table, belongs to AVCC_DRV domain
SPKL_P	AH	-	3	5	8	Left channel speaker output positive Programmable digital I/O, refer to MUX table, belongs to AVCC_DRV domain
MICBIAS	PO	2	40	2	5	Microphone bias output Programmable digital I/O, refer to MUX table, belongs to AVCC domain
VREF	PO	3	1	3	6	Codec bandgap reference output, add a 1µF cap as close as possible, belongs to AVCC domain
AUXIN_R	AH	-	-	-	67	AUX input right channel pad. Programmable digital I/O, refer to MUX table, belongs to AVCC domain
AUXIN_L	AH	-	-	-	68	AUX input left channel pad. Programmable digital I/O, refer to MUX table, belongs to AVCC domain

AH: Analog and digital hybrid programmable

PO: Power output

7.5. Power Management

Table 5. Power Management

Pin Name	Pad Type	RTL 8763BM	RTL 8763BF/ BFR	RTL 8763BS	RTL 8763BA	Description
VBAT	PIO	27	27	33	48	Battery input when battery only Battery charge output when in charger mode with adapter in
ADP_IN	PI	28	28	34	49	Adapter input for battery charge
HV_CORE	PO	26	26	32	47	Switch output for switch mode regulator, add a 4.7µF cap as close as possible
LX_CORE	PO	25	25	31	46	Switch mode regulator output, connect to a 2.2µH inductor as close as possible
VDDCORE	PI	23	23	29	44	Switch mode regulator sense input and digital core power input

HV_AUDIO	PO	-	29	35	50	Switch output for switch mode regulator, add a 4.7µF cap as close as possible
LX_AUDIO	PO	-	30	36	51	Switch mode regulator output, connect to a 2.2µH inductor as close as possible
HV_A	PO	29	-	-	-	Switch output for LDO, add a 1µF cap as close as possible
LDO_A	PO	30	-	-	-	LDO mode regulator output, add a 1µF as close as possible.
AVCC	PO	7	7	9	12	Switch mode regulator sense input and power input for codec digital circuitry, 1.8V or 2.8V
AVCC_DRV	PI	4	2	4	7	Power input for codec drive stage, 1.8V or 2.8V
VD33_PA	PI	9	9	11	16	3.3V power input for RF PA
VD33_SYN	PI	11	11	13	18	3.3V power input for RF synthesizer
VPA33	PO	20	20	22	33	3.3V linear regulator output
VD12_SYN	PI	12	12	14	19	1.2V power input for RF synthesizer
VD12_RTX	PI	8	8	10	15	1.2V power input for RF circuitry
LDO_AUX1	PO	19	19	21	32	Programmable linear regulator output for I/O
LDO_AUX2	PO	31	31	37	52	Programmable linear regulator output for I/O
V33_USB	PO	-	-	-	64	Power output, add 1µF cap
ADPSO	PO	24	24	30	45	Power output, add 1µF cap
DIG_OUT	PO	15	15	17	22	Power output, add 1µF cap
HV33	PO	32	32	38	53	Power output, add 1µF cap
GND_EP	GND	EP	EP	EP	EP	Exposed pad with ground connections

PO: Power Output

PI: Power Input

PIO: Power Input and Output

7.6. SPI FLASH Memory Interface

Table 6. SPI FLASH Memory Interface

Pin Name	Pad Type	RTL 8763BM	RTL 8763BF/ BFR	RTL 8763BS	RTL 8763BA	Description
SPIFLASH_ SCLK	O	34	-	42	59	Serial flash clock output
SPIFLASH_ CS#	I/O	36	-	44	61	Serial flash chip select, low active

SPIFLASH_SI/ SIO0	I/O	35	-	43	60	Serial flash data output for 1-bit mode, connect to SI pin of external FLASH memory Serial flash data output for 4-bit mode, connect to SIO0 pin of external FLASH memory
SPIFLASH_SO/ SIO1	I/O	37	-	45	62	Serial flash data input for 1-bit mode, connect to SO pin of external FLASH memory Serial flash data output for 4-bit mode, connect to SIO1 pin of external FLASH memory
SPIFLASH_ WP#/SIO2	I/O	-	-	-	63	Serial flash data output for 4-bit mode, connect to SIO2 pin of external FLASH memory
SPIFLASH_ HOLD#/SIO3	I/O	-	-	-	58	Serial flash data output for 4-bit mode, connect to SIO3 pin of external FLASH memory

O: Digital output

I: Digital input

7.7. System

Table 7. System

Pin Name	Pad Type	RTL 8763BM	RTL 8763BF/ BFR	RTL 8763BS	RTL 8763BA	Description
HW_RST#	I_PU	18	18	20	31	System reset input with internal pull high, low active with at least 5ms low to trigger system reset
USB_DP	AI/O	-	-	-	65	USB signal positive
USB_DN	AI/O	-	-	-	66	USB signal negative

I_PU: Input with internal pull high inside

8. Ordering Information

Table 10. Ordering Information

Part Number	Package	Status
RTL8763BM	QFN-40, 5mm x 5mm Outline; 'Green' Package	MP
RTL8763BF	QFN-40, 5mm x 5mm Outline; 'Green' Package	MP
RTL8763BFR	QFN-40, 5mm x 5mm Outline; 'Green' Package	MP
RTL8763BS	QFN-48, 6mm x 6mm Outline; 'Green' Package	MP
RTL8763BA	QFN-68, 8mm x 8mm Outline; 'Green' Package	MP

Note: See page 7 for package identification information.

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Realtek RTL8763B
Bluetooth RF Test Tool
RTLBTAPP
User Manual

Draft v0.2

2017/08/8

Revision History

Date	Version	
2017/07/11	Draft v0.1	Initial
2017/08/08	Draft v0.1	Add BLE DTM Test

Catalog

Figure List

1. Overview

This document is used to introduce RF test tool “RTLBTAPP” for Realtek Bluetooth chip RTL8763B series. Customers should comply with the steps and requirements under this document. Contact Realtek Bluetooth FAE if any problem arises in RF test flow.

2. Files

MP tool package is provided to customers in binary format:

RTLBTAPP.exe	MP executable file
RtlBluetoothMP.dll	MP dll library

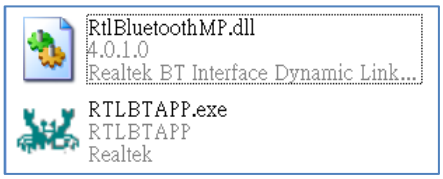


Figure 1 File List

Double click “RTLBTAPP.exe” to open this tool. However, please use “Run Administrator” to open it in Vista/Windows7 or higher.

3. Hardware environment

Before use this tool, PC should direct connected UART port. The connection between Bluetooth and HOST chip must be cut off.

4. Open RTLBTAPP

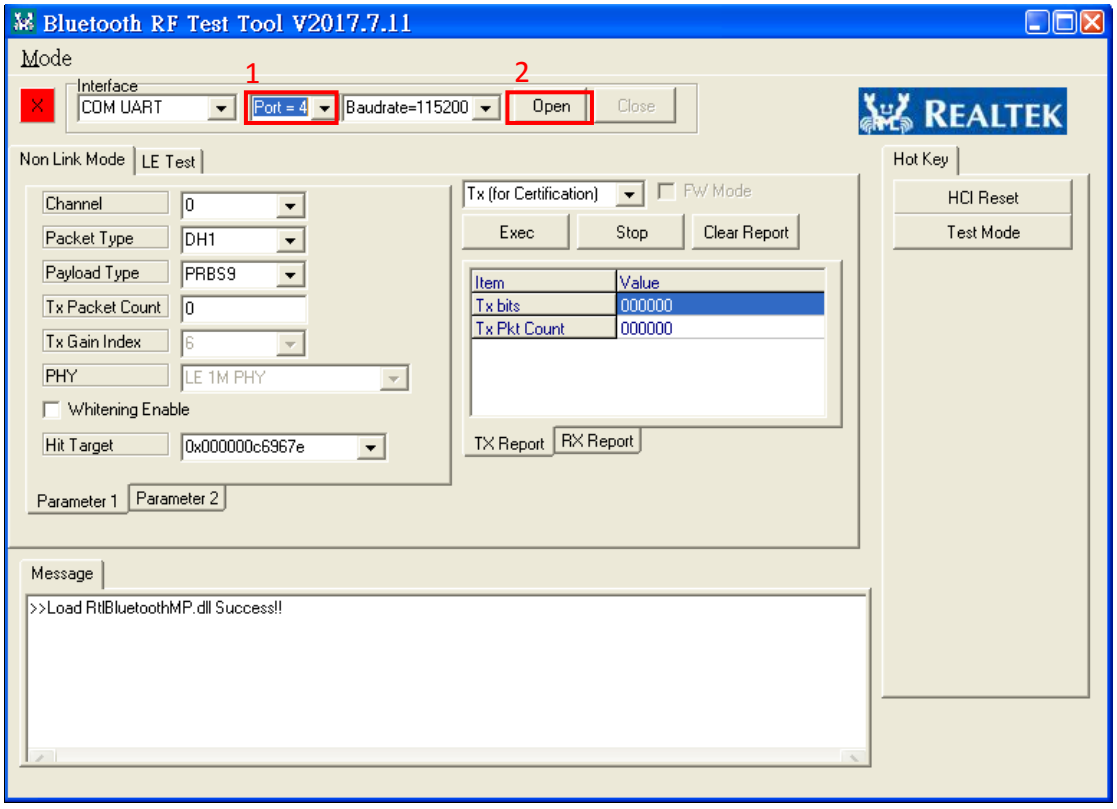


Figure 2 Open BTLBTAPP

Step 1: Select correct interface.

- UART:

If the module interface is UART, please select "UART" and check COM port number in Device Manager.

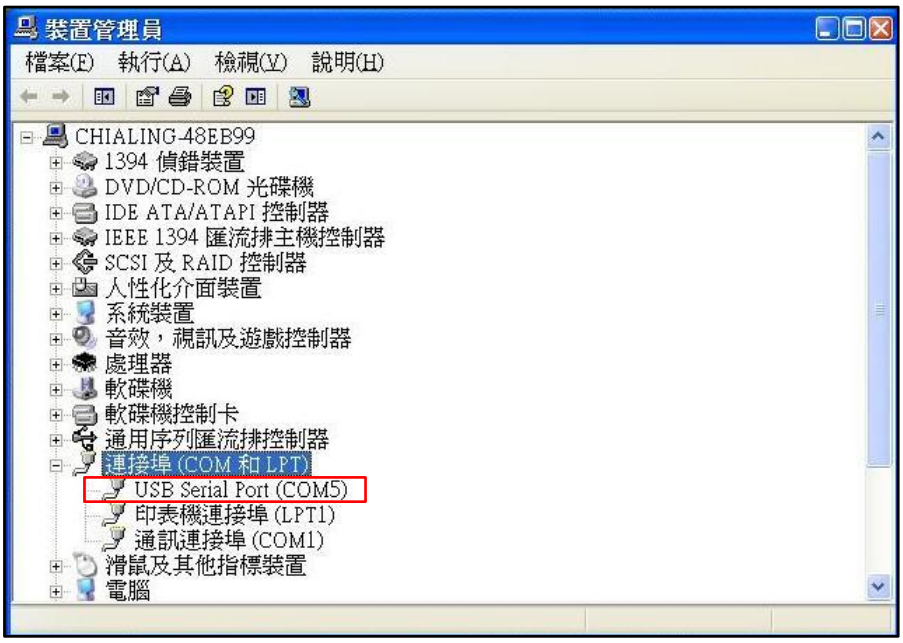


Figure 3 Check COM port number

Step 2: Click "Open".

After clicking "Open" button, the up left corner changes to green means it is successful to open BT Device.

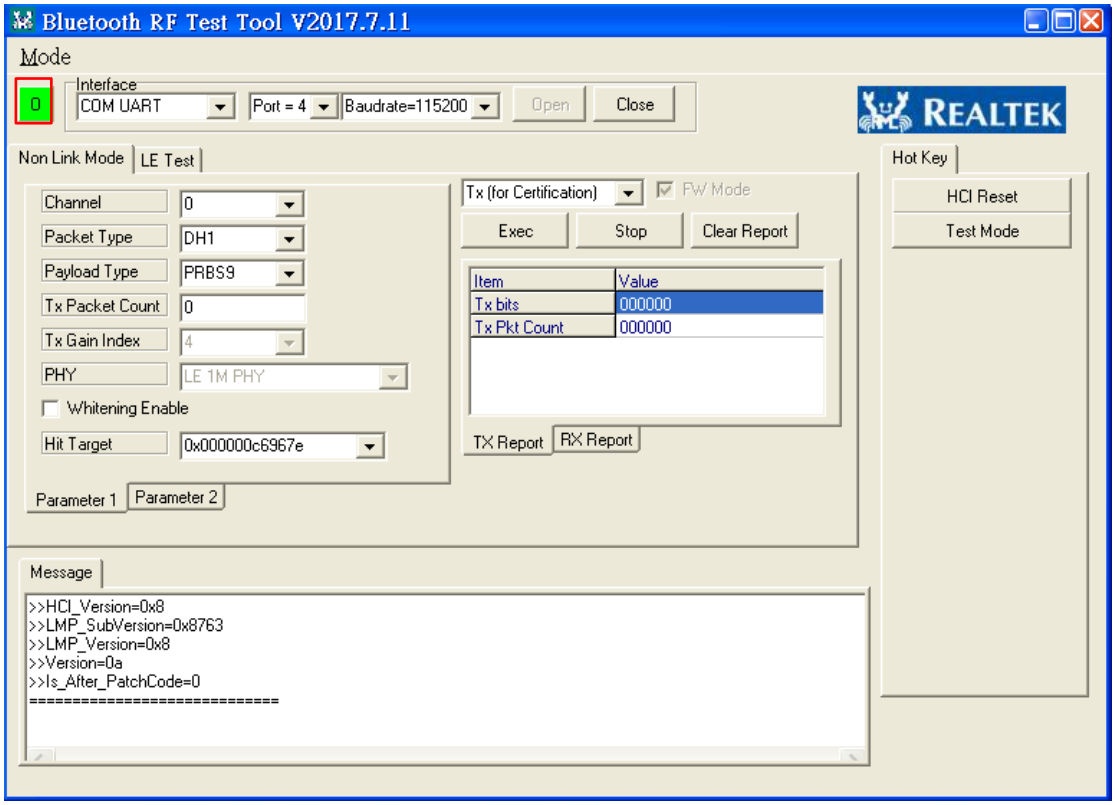


Figure 4 Device opens successfully

5. DUT (Link) Test Mode

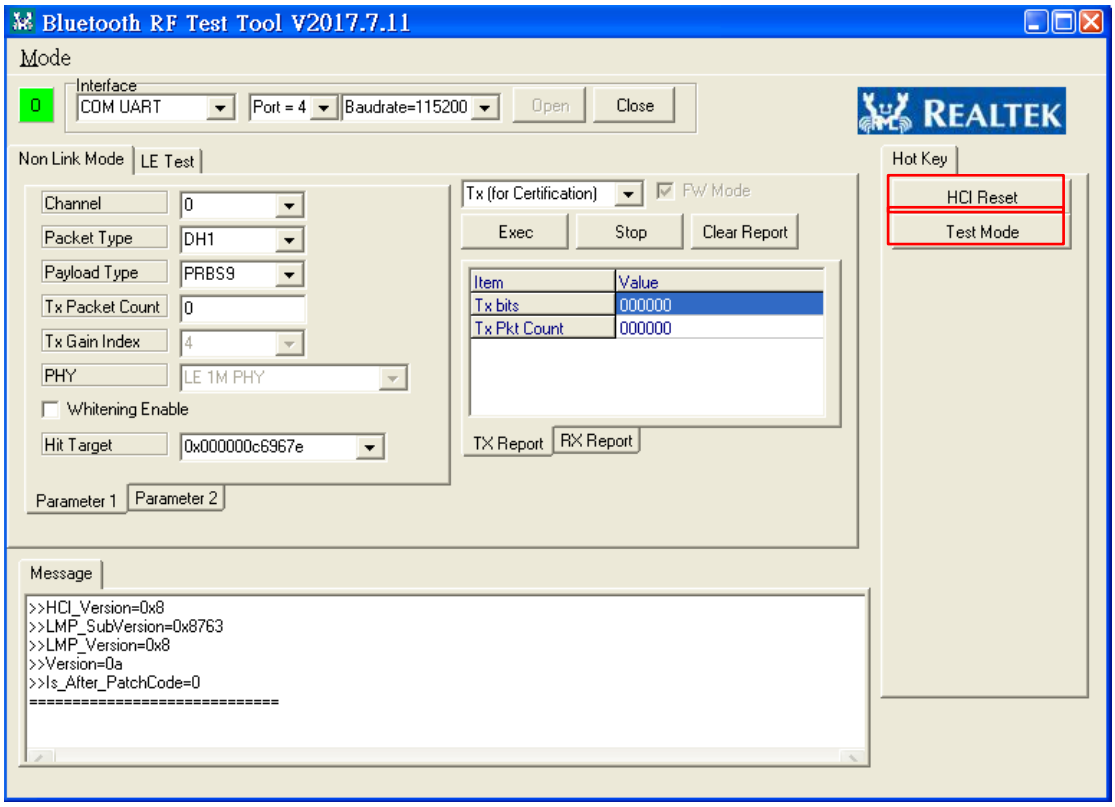


Figure 5 Enter link test mode

Enter link test mode, please follow the below operations.

- **Step 1:** Click “HCI Reset” button to reset.
- **Step 2:** Click “Test Mode” button to enter DUT Test Mode (link test mode).
- **Step 3:** After testing, click “HCI Reset” button to exit DUT Test Mode

6. LE DUT TX/RX Test(MP)

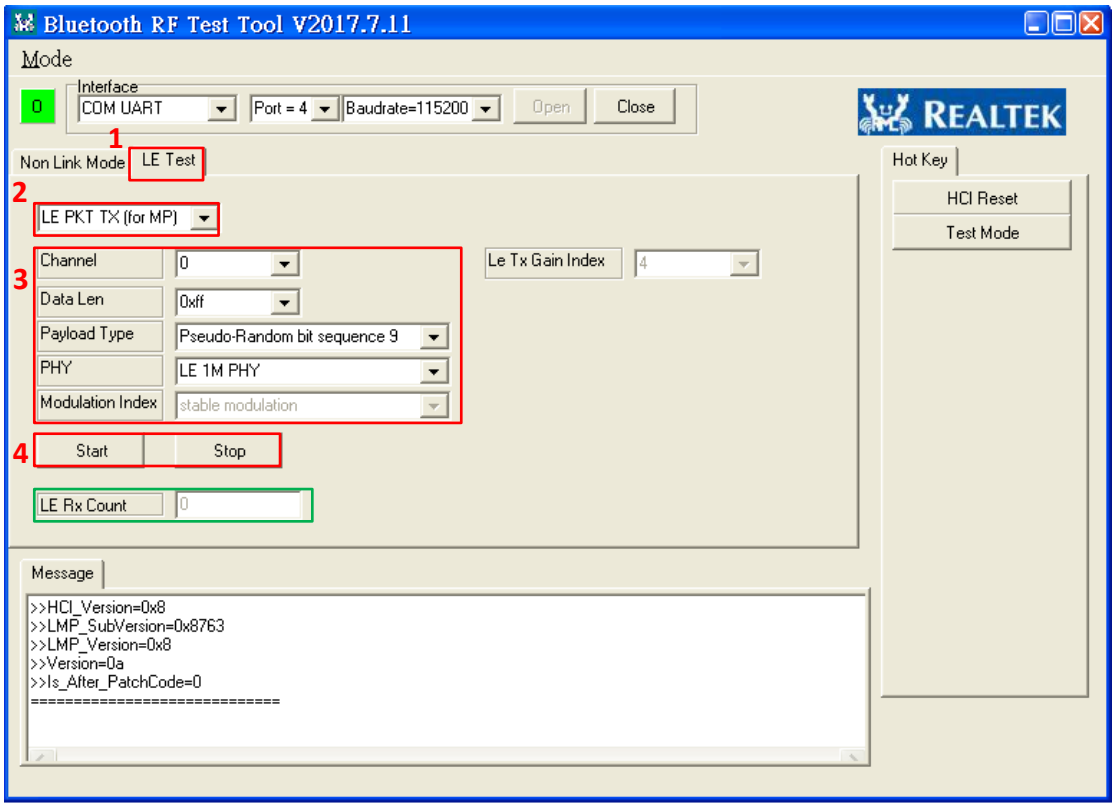


Figure 6 LE Test

- **Step 1:** Choose “LE Test”.
- **Step 2:** Choose “LE PKT TX” or “LE PKT RX”
- **Step 3:** Choose LE Test Parameters :
  - (a) Channel :0~39.
  - (b) Data length:0~0xFF
  - (c) PayType: PRBS9, 1111_0000, 1010, PRBS15, ALL1, ALL0, 0000_1111, 0101
  - (d) PHY: LE 1M PHY, LE 2M PHY, LE Coded PHY with S=8, LE Coded PHY with S=2
- **Step 4:** Click “Start” button and start to test. After testing, click “Stop” button.

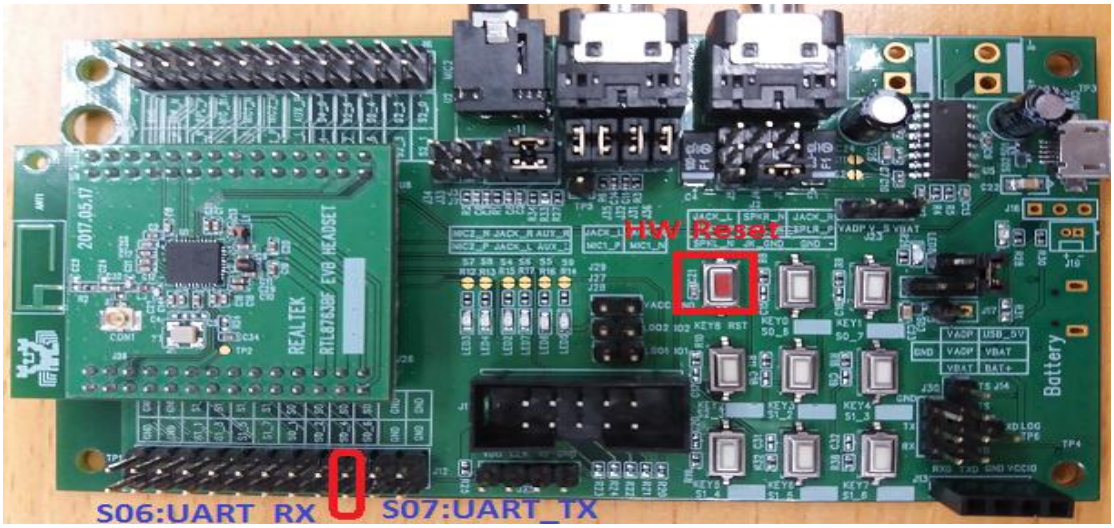
The green rectangle shows received LE Rx Packets in LE PKT RX mode.

7. BLE Direct Test Mode

This section describes the direct test mode mechanisms for testing Bluetooth Low Energy devices and explains how the direct test mode connection is established.

This Direct Test Mode MODE requires a direct connection to the Bluetooth measurement instrument.The Realtek Bluetooth Device uses the HCI UARTt interface to connect to the Bluetooth measurement instrument.

Realtek defines the uart pin as shown in the table below:

PIN Name	Interface
S06	UART RX
S07	UART TX
EVB	 **Figure 7 Reference EVB board define** Note: Reference EVB board define as(This version may change)

- **If if Bluetooth measurement instrument interface is hci uart or 2 wire:**

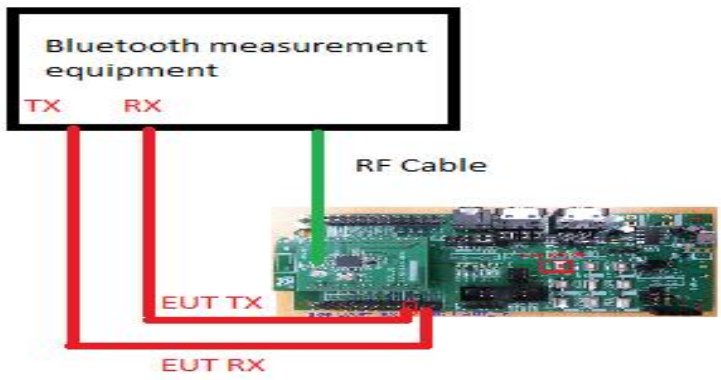


Figure 8 Connect to instrument by uart interface

- **if Bluetooth measurement instrument interface is RS232, Level shift is required also .**

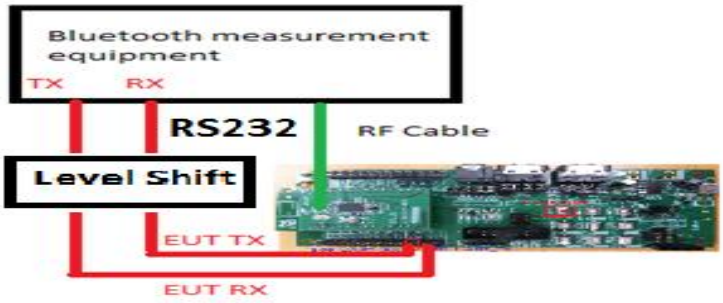


Figure 9 Connect to instrument for RS232 interface

- **if Bluetooth measurement instrument interface has support USB converter UART board, such as FTDI USB converter board.**

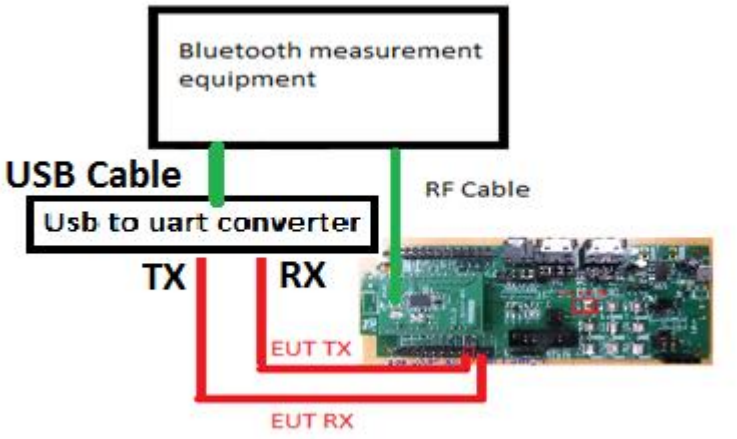


Figure 10 Connect to instrument for usb to uart converter boar

- **Configuration test environment step by step :**

1. Connect an RF cable between the antenna connector on the EUT and Bluetooth measurement equipment.
2. Connect the HCI UART(RS232) TX to UART RX of Bluetooth measurement equipment (level shift or usb converter board).
3. Connect the HCI UART(RS232) RX to UART TX of Bluetooth measurement equipment (level shift or usb converter board).
4. Connect GND between the EUT and Bluetooth measurement equipment or connect USB Cable to Tester.
5. Push HW Reset pin and to begin test..

8. Appendix

FCC Statement:

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Label Instructions

The outside of final products that contains this module device must display a label

referring to the enclosed module. This exterior label can use wording such as the

following**: "Contains Transmitter Module FCC ID: TX2-RTL8763BA"** or "**Contains FCC ID:**

TX2-RTL8763BA." Any similar wording that expresses the same meaning may be used.

Additionally, there must be the following sentence on the device, unless it is too small to carry it:

"This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation."

This device is intended only for OEM integrators under the following conditions:

(1) The antenna must be installed such that 20cm is maintained between the antenna and users, and

(2) This device and its antenna must not be co-located with any other transmitters except in accordance with FCC multi-transmitter product procedures. Referring to the multi-transmitter policy, multiple-transmitter(s) and module(s) can be operated simultaneously with C2P.

User's manual of the end product:

In the user's manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC RF exposure guidelines for an uncontrolled environment can be satisfied. The end user has to be also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's manual authority to operate this equipment.

IC Statement

This device complies with Industry Canada license-exempt RSS standard(s).

Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le present appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisee aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioelectrique subi, meme si le brouillage est susceptible d'en compromettre le fonctionnement.

If the final product is to be sold in Canada, then this exterior label should use wording such as the following: “Contains Transmitter Module IC: 6317A-RTL8763BA”

Taiwan requlatory information(NCC)

低功率電波輻射性電機管理辦法

第十二條　經型式認證合格之低功率射頻電機，非經許可，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。

第十四條　低功率射頻電機之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。

前項合法通信，指依電信法規定作業之無線電通信。

低功率射頻電機須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。