승 인 원

◈ 제 품 명: BWR-Y89359 SMA
◈ 품 번: M3012001296
◈ 적용모델: D-AUDIO2.0V/PIO3.0
◈ 적용차종: DL3외
◈ 고 객 명: 현대 모비스
◈ 버 전: Rev 1.6

상기 제품에 대해 승인 합니다.

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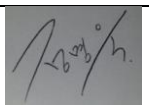
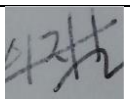
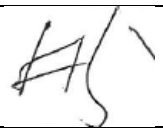
고객승인			
㈜eSSys	담 당	검 토	승 인
			

Revision History

Revision	Date	Contents of Revision	Author
1.0	2017.11.16	Preliminary	MW.J
1.1	2018.03.06	7.1 Module Dimension 쉴드캔 도면 변경	Lee. J. H
		7.3 Barcode Label Specification Update	
		7.4 Product Picture Update	
		10.1 Packing Information Update	
		10.3 Ordering Inforamtion Update	
		10.4 BT PATCH RAM / WIFI NVRAM File Information Update	
1.2	2018.11.08	7.1 Module Dimension change.	Lee.J.H
		7.4 Product Picture Update.	
		10.4.3 Module Version Selection Table add.	
1.3	2018.11.26	4.4 I2S Interface Update	Lee. J.H
		7.4 Product Picture Update.	
		Module Name Change. BWR-B89359SMA -> BWR-Y89359SMA	
1.4	2018.01.07	10.4.2 WiFi NVRAM File Information change. SW 배포일 최신 날짜로 변경	Lee. J.H
1.5	2019.01.21	4.2.3 SDIO Bus Timing Specifictaion in SDR Modes -> device input timing change	Lee. J.H
1.6	2019.03.22	7.1 Module Dimension Update.	Lee. J.H
		7.4 Product Picture Update.	

Table of Contents

1.General Description

1.1 General Features

- Module type:
  - 48 pin SMD Type
- Compact dimension: 22.5 x 20 x 2.5mm Max
- Host Interfaces: SDIO (Ver.3.0) for Wi-Fi and UART for Bluetooth
- RoHS compliant
- Supply Voltage:
  - VDD: 3.3V
  - SDIO_VBUS: 1.8V or 3.3V
- Operating temperature range: -40℃~+85℃
- Programmable dynamic power management
- Supports 1410 bytes of user-accessible OTP, of which 256 bytes are allocated for BT and 1150 bytes are allocated for WLAN for storing board parameters.
- Security:
  - WPA, WAPI STA, and WPA2 (Personal) support for powerful encryption and authentication
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
- Worldwide regulatory support
- Global products supported with worldwide homologated design.
- This module uses shield cans of C7521 material.
- This module has deployed part which are AEC-Q100 qualified.

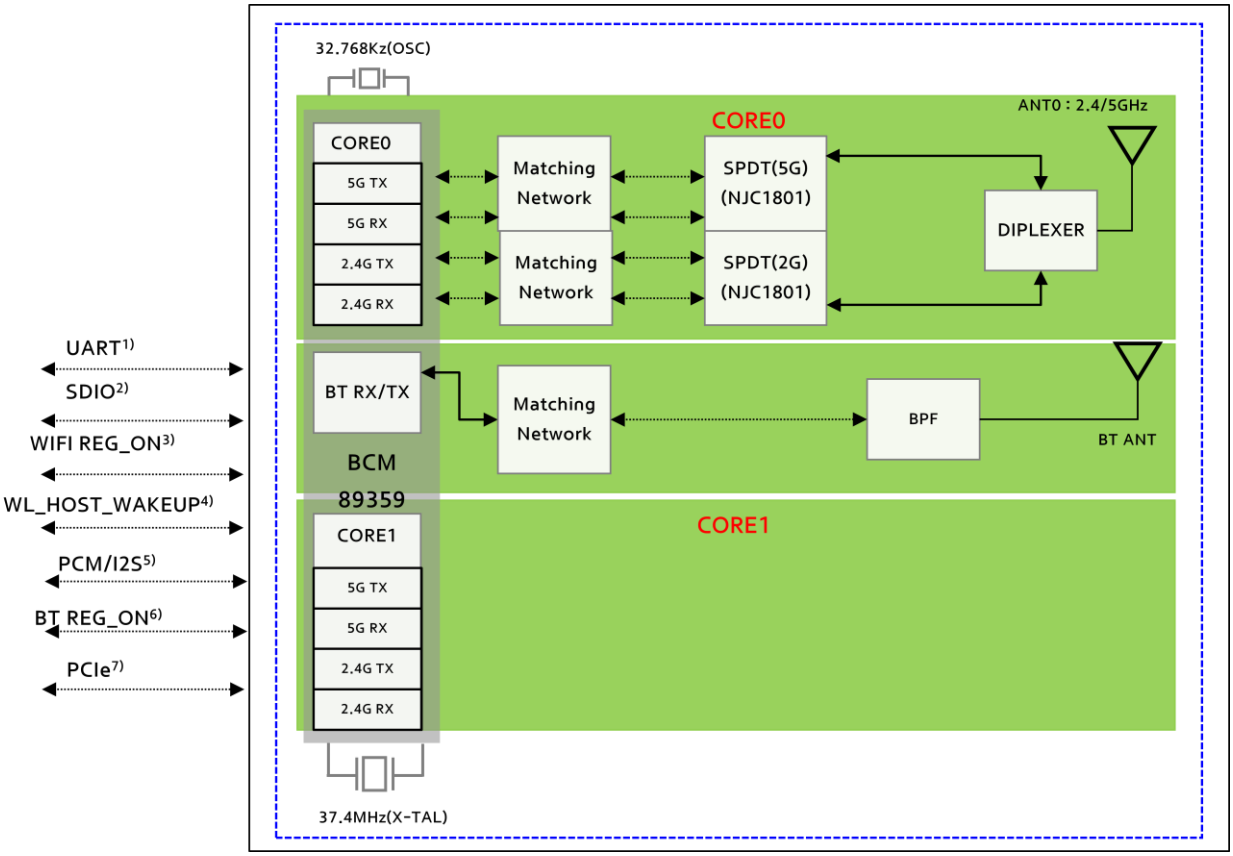
1.2 IEEE 802.11x Key Features

- IEEE 802.11ac compliant.
- Dual-stream spatial multiplexing up to 867 Mbps data rate.
- Supports 20, 40 and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- Tx and Rx low-density parity check (LDPC) support for improved range and power efficiency.
- Supports IEEE 802.11ac/n beamforming.
- Supports real simultaneous dual-band (RSDB).
- Supports standard SDIO v3.0 (up to SDR104 mode at 208MHz, 4-bit and 1-bit) host interfaces.
- Backward compatible with SDIO v2.0 host interfaces.

1.3 Bluetooth Key Features

- Complies with Bluetooth Core Specification Version 4.2 with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO) for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support:
  - Host controller interface (HCI) using a USB or High-speed UART interface.
  - PCM for audio data.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.

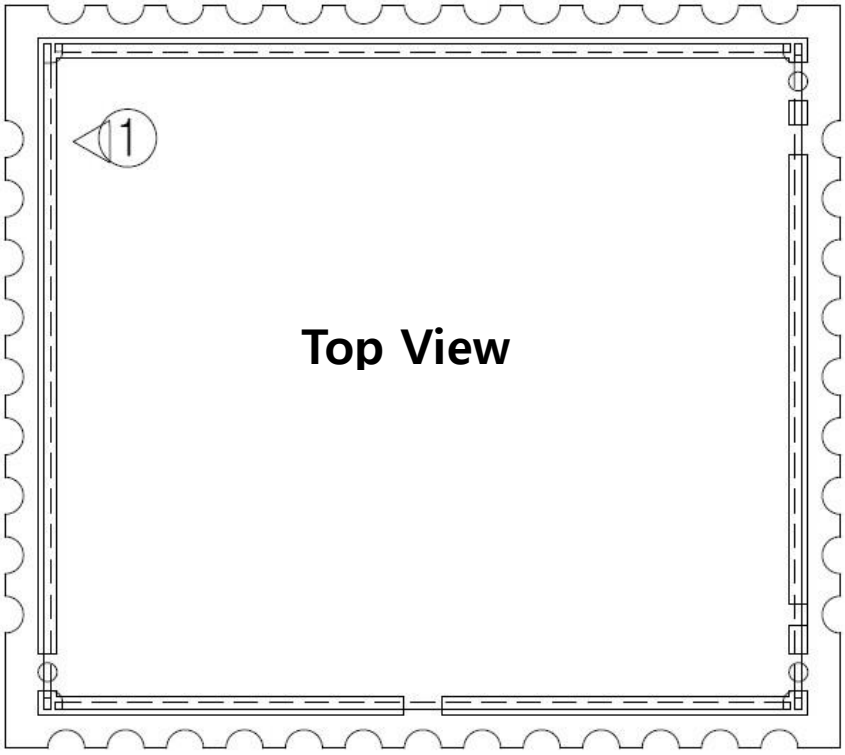
1.4 Block Diagram



1) Host Interface for Bluetooth: 4 Pins (BT_UART_TXD, BT_UART_RXD, BT_UART_CTS, BT_UART_RTS)
2) Audio Interface for Bluetooth: 4 Pins (BT_PCM_CLK, BT_PCM_SYNC, BT_PCM_IN, BT_PCM_OUT)
3) Host Interface for Wi-Fi: 6Pins (SDIO_CMD, SDIO_CLK, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, SDIO_DATA3)
4) Bluetooth/Wi-Fi On/Off and Reset: 2Pins (BT_REG_ON for Bluetooth, WIFI_REG_ON for Wi-Fi)
5) Controlled by Module to wake-up Host. (Optional)
6) External LPO 32.768KHz Clock. (Optional)
7) Host Interface for WIFI : PCIe /SDIO 선택 적용

2.Pin Assignments and Descriptions

2.1 Pin Assignments



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
PCIE_CLK_P	PCIE_CLK_N	PCIE_TD_N	PCIE_TD_P	SDIO_CLK	SDIO_CMD	SDIO_DATA3	SDIO_DATA2	SDIO_DATA1	SDIO_DATA0	SECI_IN	SECI_OUT	VBAT	VBAT	VIO_SDIO	BT_ANT	WL_REG_ON	BT_REG_ON	BT_PCM_CLK	BT_PCM_SYNC	BT_PCM_IN	BT_PCM_OUT	WL_ANT_CORE0	GND
25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
LPO	GND	VER_VOLTAGE	WL_HOST_WAKE_UP	GND	GND	WL_ANT_CORE1	SDIO_PAD	BT_UART_RTS_N	BT_UART_CTS_N	BT_UART_RXD	BT_UART_TXD	VIO	SDIO_DIS	PCIE_EN	PCIE_PME_L	PCIE_PERST_N	PCIE_CLKREQ	PCIE_RD_P	PCIE_RD_N	GND	GND`	GND	GND

2.2 Pin Descriptions

Pin #	Pin Name	Type	Descriptions
1	PCIE_CLK_P	I	PCIE Differential Clock inputs positive. 100MHz differential.
2	PCIE_CLK_N	I	PCIE Differential Clock inputs negative. 100MHz differential.
3	PCIE_TD_N	O	Transmitter differential pair(x1 lane). Negative.
4	PCIE_TD_P	O	Transmitter differential pair(x1 lane). Positive.
5	SDIO_CLK	I	SDIO clock input.
6	SDIO_CMD	I/O	SDIO command line.
7	SDIO_DATA3	I/O	SDIO data line 3.
8	SDIO_DATA2	I/O	SDIO data line 2.
9	SDIO_DATA1	I/O	SDIO data line 1.
10	SDIO_DATA0	I/O	SDIO data line 0.
11	SECI_IN	I	Coexistence Input.
12	SECI_OUT	O	Coexistence Output.
13	VBAT	PWR	Power supply 3.3V.
14	VBAT	PWR	Power supply 3.3V.
15	VIO_SDIO	PWR	Positive supply for SDIO 1.8V.
16	BT_ANT	RF	Pad for 2.4G Bluetooth ANT PORT
17	WL_REG_ON	I	PMU to power up or power down the internal BCM89359 regulators used by the WLAN section.
18	BT_REG_ON	I	PMU to power up or power down the internal BCM89359 regulators used by the Bluetooth section.
19	BT_PCM_CLK	I/O	PCM clock; can be master(output) or slave(input).
20	BT_PCM_SYNC	I/O	PCM sync ; can be master(output) or slave(input).
21	BT_PCM_IN	I	PCM data input.
22	BT_PCM_OUT	O	PCM data output.
23	WL_ANT_CORE0	RF	Pad for 2.4G/5G dual WLAN ANT PORT 0
24	GND	GND	Ground
25	LPO	I	Select the internal LPO or External LPO(Optional). - 32.768Khz clock. - Default internal LPO
26	GND	GND	Ground
27	VER_VOLTAGE	O	Connect to ADC port in host for module chipset identification. - 0 ~ 3.3V
28	WL_HOST_WAKE_UP	O	WLAN Host wake up.
29	GND	GND	Ground
30	GND	GND	Ground
31	WL_ANT_CORE1	RF	Pad for 2.4G/5G dual WLAN ANT PORT 1
32	SDIO_PAD	I	SDIO interface voltage control Pad

			- HIGH : 1.8V - LOW : 3.3V
33	BT_UART_RTS_N	O	UART clear-to end. Active-low clear-to-send signal for the HCI UART interface.
34	BT_UART_CTS_N	I	UART request-to-send. Active-low request-to-send signal for the HCI UART interface.
35	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
36	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.
37	VIO	PWR	Power supply 3.3V.
38	SDIO_DIS	I/O	SDIO_ ENABLE CONTROL PAD - HIGH : SDIO disable - LOW : SDIO enable
39	PCIE_EN	I/O	PCIE_ ENABLE CONTROL PAD - HIGH : PCIE enable - LOW : PCIE disable
40	PCIE_PME_L	OD	PCI power management event output.
41	PCIE_PERST_N	I	PCIe System Reset.
42	PCIE_CLKREQ	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.
43	PCIE_RD_P	I	Receiver differential pair(x1 lane). Positive
44	PCIE_RD_N	I	Receiver differential pair(x1 lane). Negative
45	GND	GND	Ground
46	GND	GND	Ground
47	GND	GND	Ground
48	GND	GND	Ground

2.3 Host Interface Selection

PCIe_EN(PIN39)	*SDIO_DIS(PIN38)*	*SDIO_PAD(PIN32)*	*Mode*
HIGH	HIGH	HIGH	**PCIe**
HIGH	HIGH	LOW	**PCIe + SPROM**
LOW	LOW	HIGH	**1.8V SDIO**
LOW	LOW	LOW	**3.3V SDIO**
HIGH	LOW	HIGH	**PCIe + SDIO(1.8V)**
HIGH	LOW	LOW	**PCIe + SDIO(3.3V)**

3.Power Management and On/Off Sequence

3.1 PowerSupply Topology

Two VDD(Typ 3.3V) and a single VIO_SDIO(1.8 ~3.3V) and a single VIO(Typ 3.3V), can be used with all additional voltages being provided by the regulators in the BWR-Y89359-SMA.

Two control signals, BT_REG_ON and WL_REG_ON are used to power-up the regulators and take the respective section out of reset. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted.

3.2 WLAN Power Management

BWR-Y89359-SMA includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the BWR-Y89359-SMA into various power management states. The power management unit enables and disables internal regulators. Power up sequences are fully programmable. Free running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used whenever possible.

The BWR-Y89359-SMA WLAN power states are described as follows:

- **Active mode**– All WLAN blocks are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and clock speeds are dynamically adjusted by the PMU sequencer.
- **Deep-sleep mode** –Most of the chip including both analog and digital domains and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain. Upon a wake-up event triggered by the PMU timers, an external interrupt or a host resume through the SDIO bus.
- **Power-down mode**–The BWR-Y89359-SMA is effectively powered off by shutting down all internal regulators.

3.3 Power-Off Shutdown

The BWR-Y89359-SMA provides low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. This allows the BWR-Y89359-SDA to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, provided VDDIO remains applied to eh BWR-Y89359-SMA, all outputs are tri-stated, and most inputs signals are disabled.

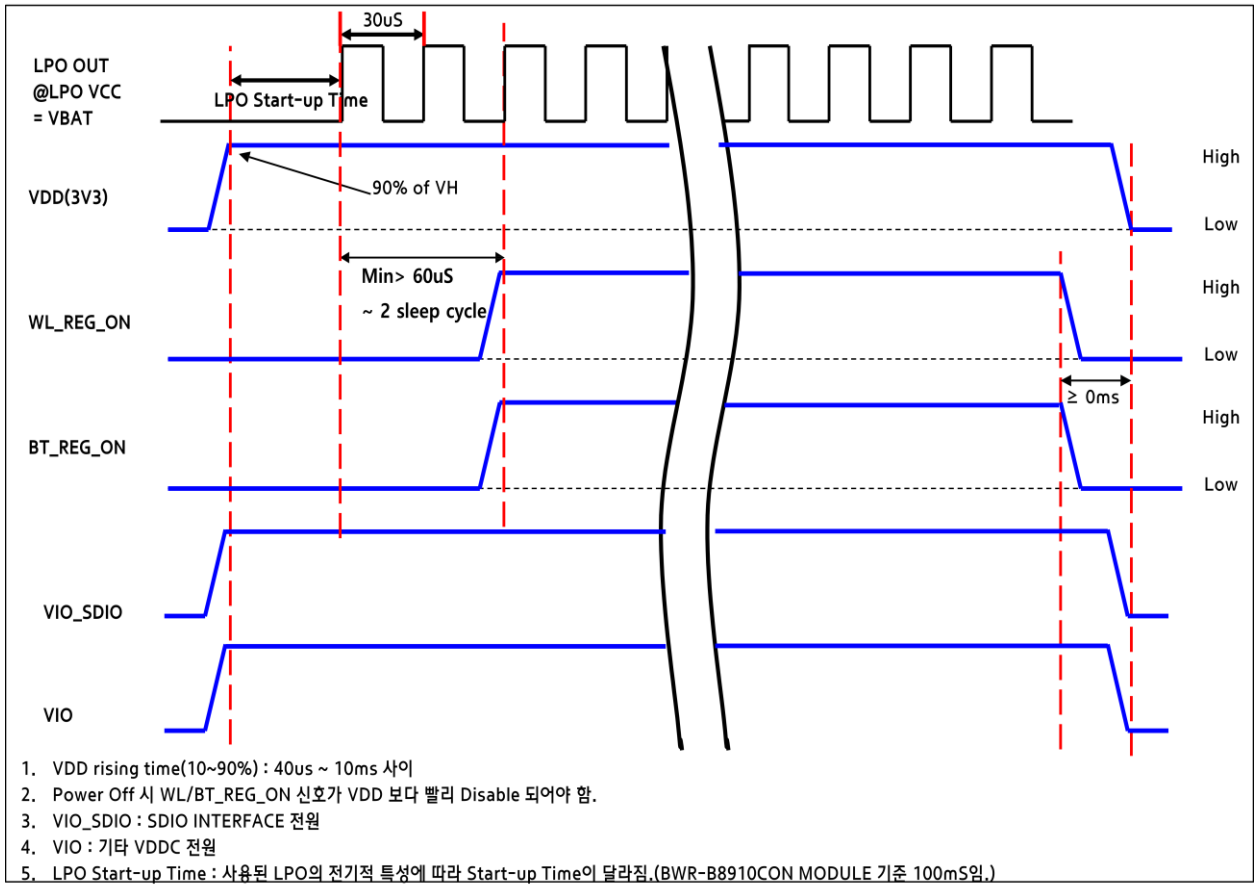
When the BWR-Y89359-SDA is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

3.4 Power-Up/Power-Down/Reset Circuits

The BWR-Y89359-SDA has two signals that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences.

Signal	*Description*
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal BCM_89359 regulators. - HIGH, the regulators are enabled and the WLAN section is out of reset. - LOW, the WLAN section is in reset. - BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal BCM89359 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

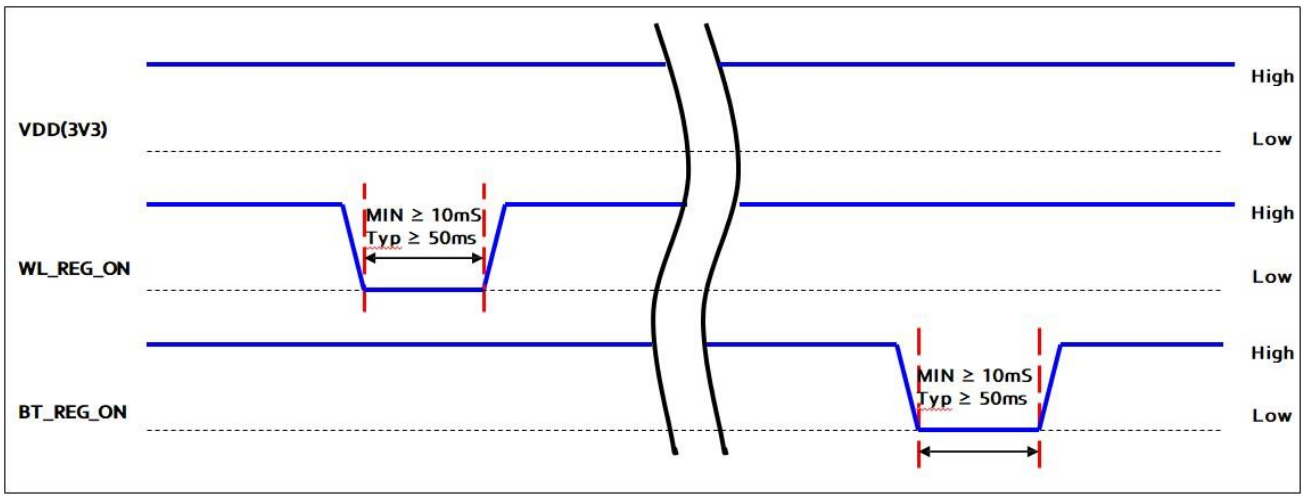
3.5 Power-Up/Down Sequence and Timing



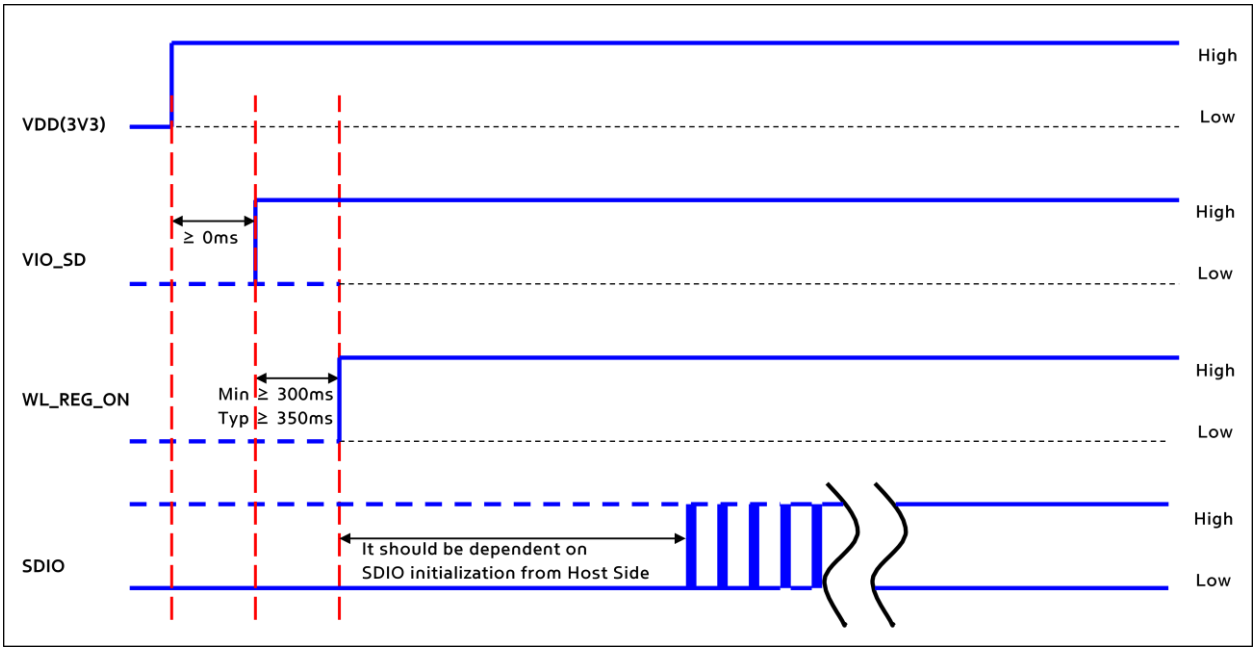
1. VDD rising time(10~90%) : 40us ~ 10ms 사이
2. Power Off 시 WL/BT_REG_ON 신호가 VDD 보다 빨리 Disable 되어야 함.
3. VIO_SDIO : SDIO INTERFACE 전원
4. VIO : 기타 VDDC 전원
5. LPO Start-up Time : 사용된 LPO의 전기적 특성에 따라 Start-up Time이 달라짐.(BWR-B8910CON MODULE 기준 100mS임.)

3.6 External Reset Sequence

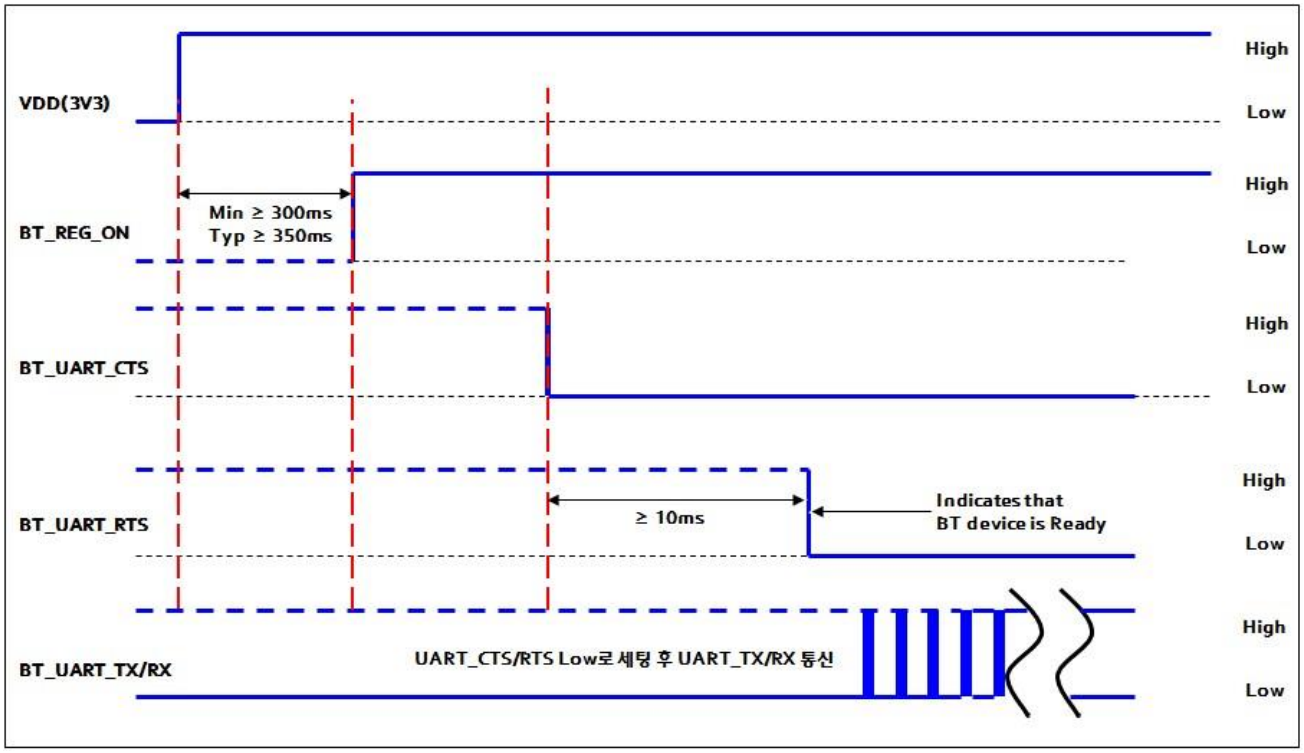
In case of external reset in the middle of operation, the BT_REG_ON for Bluetooth reset or WL_REG_ON for WLAN reset shall be LOW more than 10ms to execute proper reset action.



3.7 SDIO Start up Signaling Sequence



3.8 UART Start up Signaling Sequence



4. HardwareInterfaces

4.1 UART Interface– Bluetooth Host Interfaces

BWR-Y89359-SMA has a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an **automatic baud rate detection** capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-bytes receive FIFO and a 1040-bytes transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB(in BCM89359) interface through either DMA or the CPU. The UART supports the Bluetooth 4.2 UART HCI specification: H4, a custom Extended H4 and H5. **The default baud rate is 115.2Kbaud.**

The UART supports the 3-wire H5 UART transport as described in the Bluetooth specification ("Three-wire UART Transport Layer"). Compared to H4, the H5 UART transport reduce the number of signal lines required by eliminating the CTS and RTS signals.

The BWR-Y89359-SDA UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

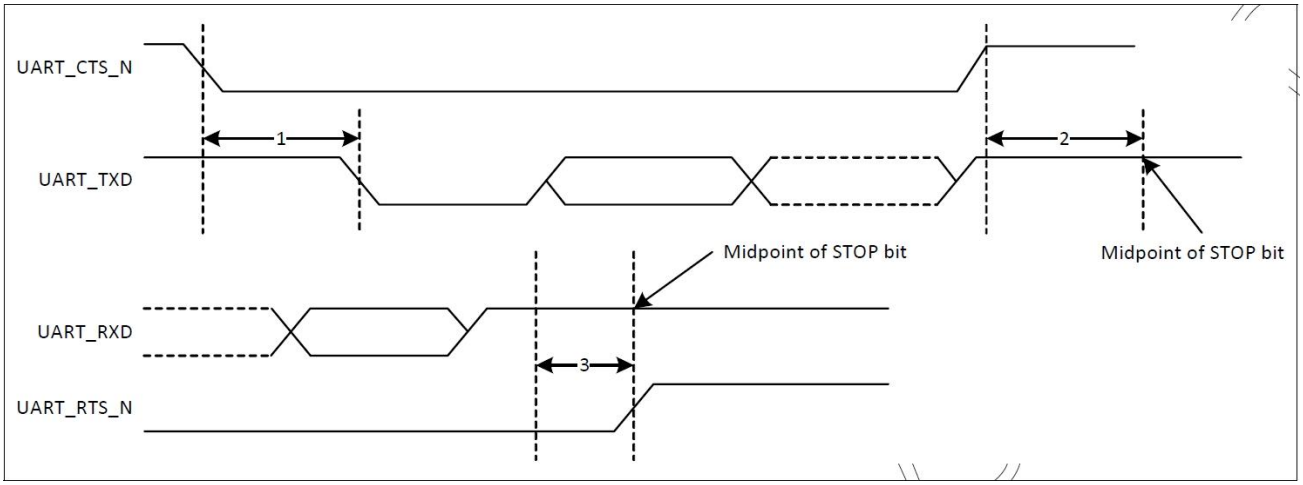
Normally, the UART baud rate is set by a configuration record downloaded after device reset or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. **The BWR-Y89359-SDA UART operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.**

❖ ***Example of Common Baud Rates***

Desired Rate	*Actual Rate*	*Error (%)*
4,000,000	4,000,000	0.00
3,692,000	3,692,308	0.01
3,000,000	3,000,000	0.00
2,000,000	2,000,000	0.00
1,500,000	1,500,000	0.00
1,444,444	1,454,544	0.70
921,600	923,077	0.16
460,800	461,538	0.16

230,400	230,796	0.17
115,200	115,385	0.16
57,600	57,692	0.16
38,400	38,400	0.00
28,800	28,846	0.16
19,200	19,200	0.00
14,400	14,423	0.16
9,600	9,600	0.00

❖ ***UART Timing***



Ref No.	*Characteristics*	*Min*	*Typ*	*Max*	*Unit*
1	Delay time, UART_CTS_N low to UART_TXD valid	-	-	1.5	Bit period
2	Setup time, UART_CTS_N high before midpoint of stop bit	-	-	0.5	Bit period
3	Delay time, midpoint of stop bit to UART_RTS_N high	-	-	0.5	Bit period

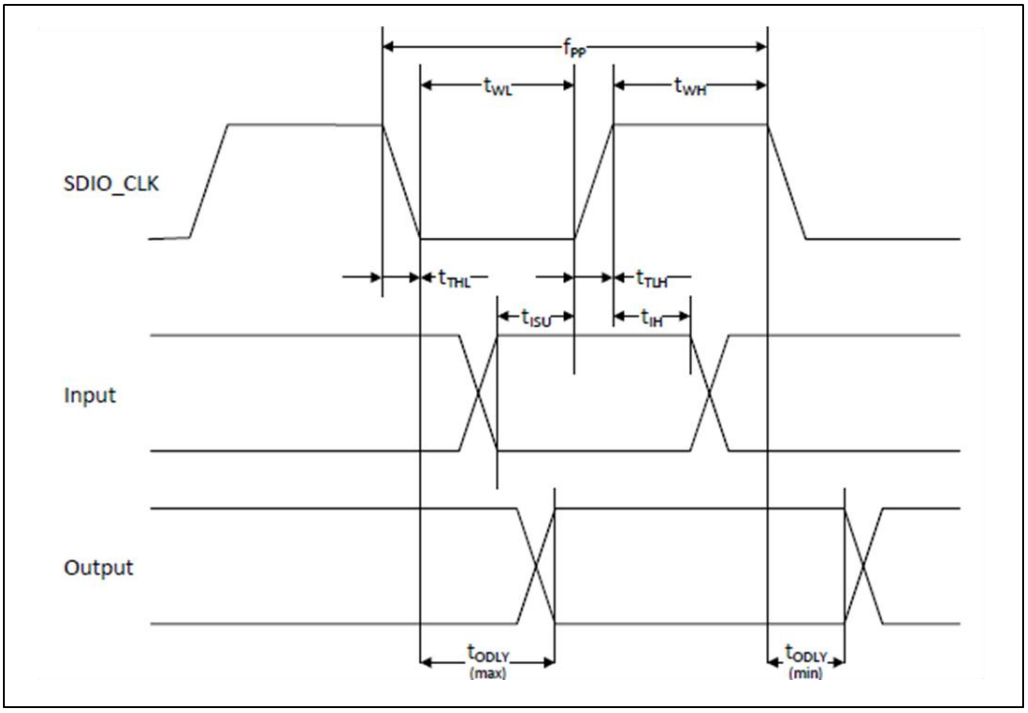
4.2 SDIO v3.0 – WLAN Host Interfaces

BWR-Y89359-SMA WLAN section provide support for SDIO version 3.0, including the new UHS-I mode:

- DS: Default speed (DS) up to 25MHz, including 1-and 4-bit modes (3.3V signaling).
- SDR12: SDR up to 25MHz (1.8V signaling).
- SDR25: SDR up to 50MHz (1.8V signaling).
- SDR50: SDR up to 100MHz (1.8V signaling).
- SDR104: SDR up to 208MHz (1.8V signaling).
- DDR50: DDR up to 50MHz (1.8V signaling).
  - ➢ **Note:** The BWR-Y89359-SDA is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided.

4.2.1 SDIO Default Mode Timing

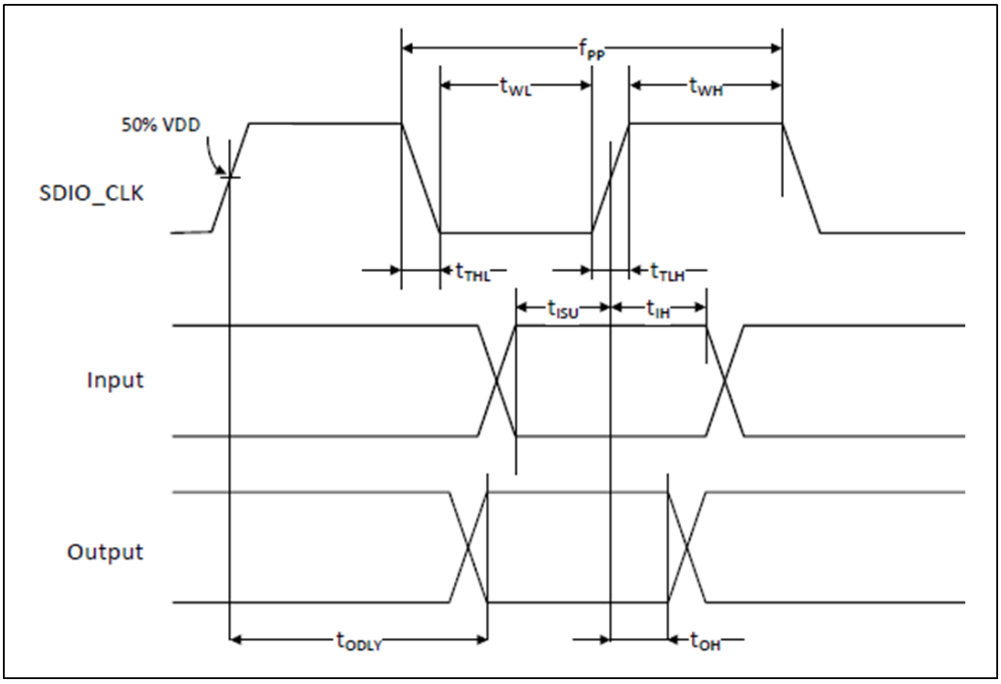


SDIO Bus Timing[a] Parameters (Default Mode)	*Symbol*	*Value*			
		Min.	*Typ.*	*Max.*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	-	25	MHz
Frequency – Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data

b. Min.(Vih) = 0.7xVDDIO_SD and max.(Vil) = 0.2xVDDIO_SD.

4.2.2 SDIO High-Speed Mode Timing



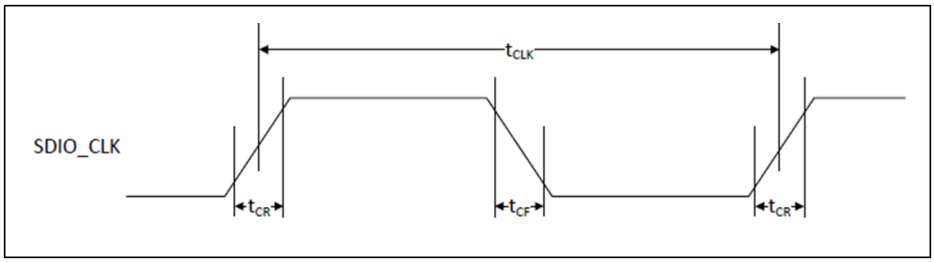
SDIO Bus Timing[a] Parameters (High-Speed Mode)	*Symbol*	*Value*			
		Min.	*Typ.*	*Max.*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	-	50	MHz
Frequency – Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data

b. Min.(Vih) = 0.7xVDDIO_SD and max.(Vil) = 0.2xVDDIO_SD.

4.2.3 SDIO Bus Timing Specification in SDR Modes

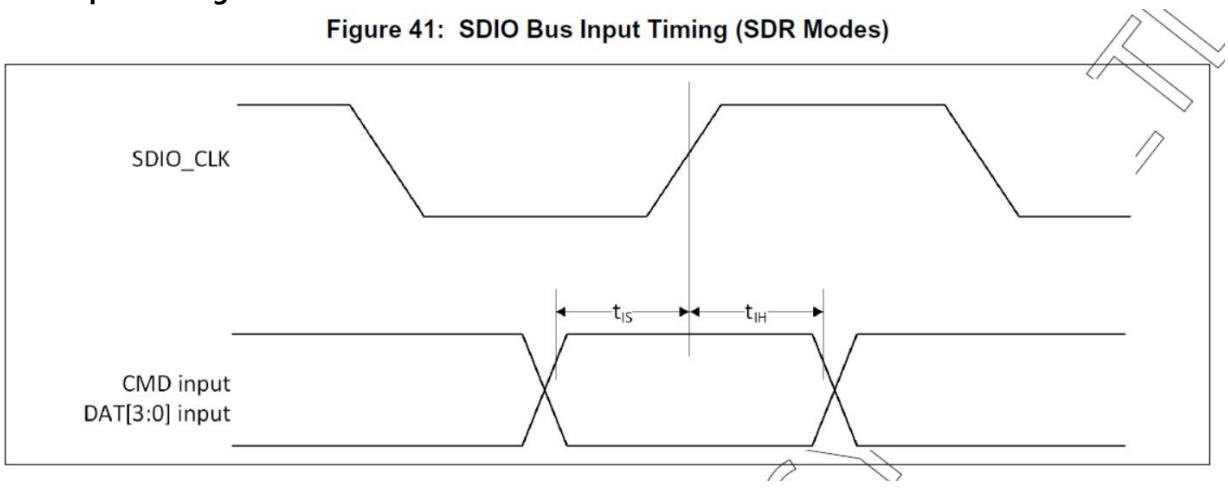
- Clock Timing



Parameter	Symbol	Min.	Max.	Unit	Comments
-	t_{CLK}	40	-	ns	SDR12 mode
		20	-	ns	SDR25 mode
		10	-	ns	SDR50 mode
		4.8	-	ns	SDR104 mode
	t_{CR}, t_{CF}	-	0.2 x t_{CLK}	ns	t_{CR}, t_{CF}< 2.00ns (max) @ 100MHz, C_{CARD} = 10pF) t_{CR}, t_{CF}< 0.96ns (max) @ 208MHz, C_{CARD} = 10pF)
Clock duty cycle	-	30	70	%	-

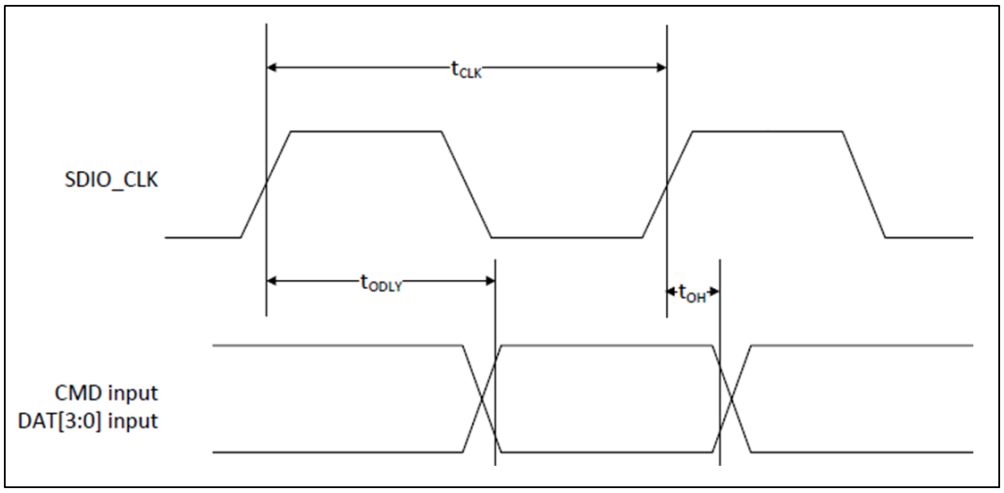
- Device Input Timing

Figure 41: SDIO Bus Input Timing (SDR Modes)



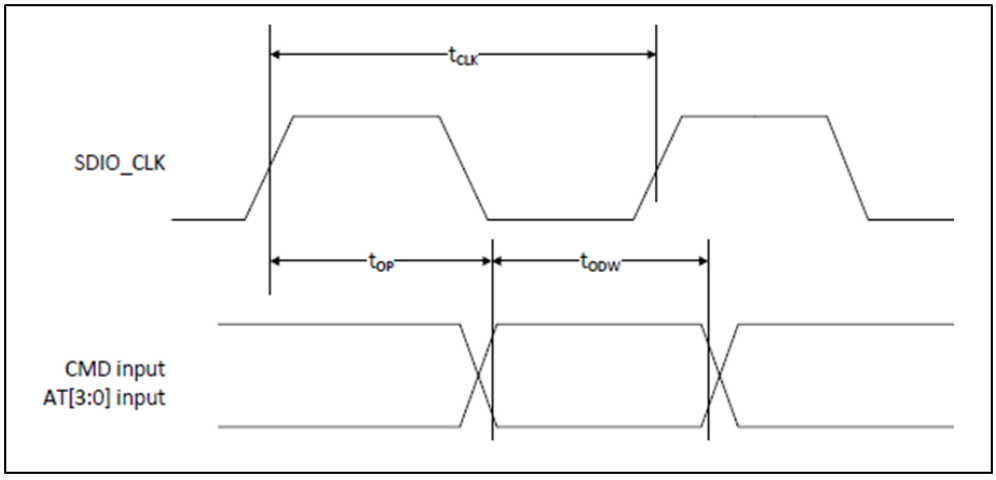
Symbol	Min.	Max.	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	-	ns	C_{CARD} = 10pF, VCT = 0.975V
t_{IH}	0.8	-	ns	C_{CARD} = 5pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.0	-	ns	C_{CARD} = 10pF, VCT = 0.975V
t_{IH}	0.8	-	ns	C_{CARD} = 5pF, VCT = 0.975V

- Device Output Timing (SDR Modes up to 100MHz)



Symbol	*Min.*	*Max.*	*Unit*	*Comments*
t_{ODLY}	-	7.5	ns	t_{CLK} ≥ 10ns C_L = 30pF using driver type B for SDR50
t_{ODLY}	-	14.0	ns	t_{CLK} ≥ 20ns C_L = 40pF using driver SDR12, SDR25
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min) C_L = 15pF

- Device Output Timing (SDR Modes up to 100MHz to 208 MHz)

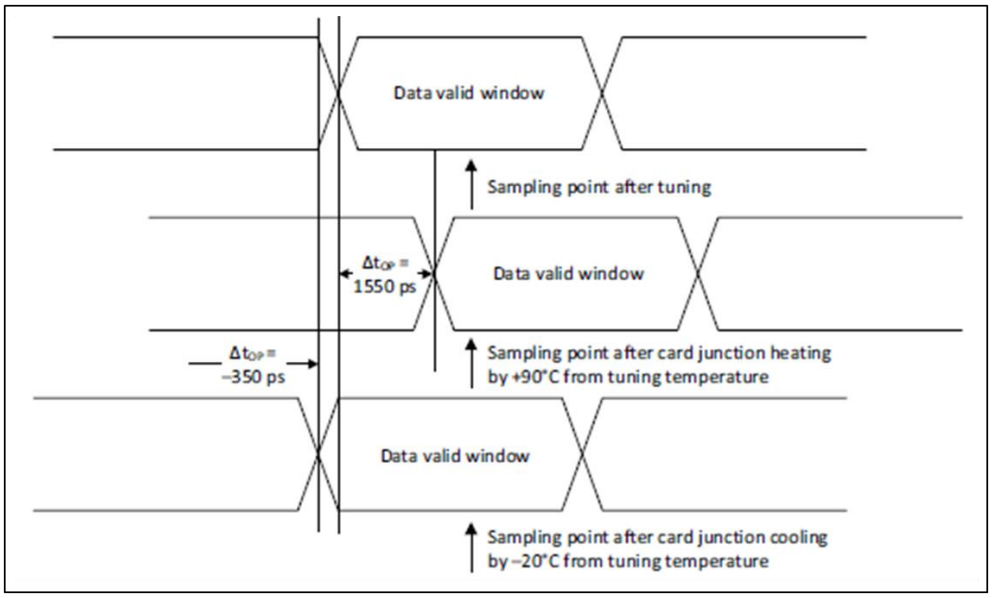


Symbol	*Min.*	*Max.*	*Unit*	*Comments*
t_{OP}	-	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.6	-	UI	t_{ODW}=2.88ns @208 MHz

Δt_{OP} = +1550ps for junction temperature of Δt_{OP}= 90 degrees during operation

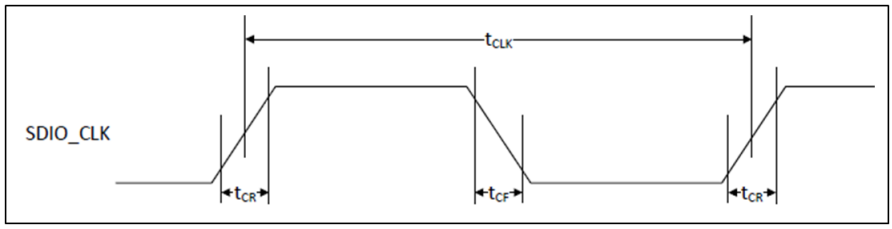
Δt_{OP} =-350 ps for junction temperature of Δt_{OP}= -20 degrees during operation

Δt_{OP} = +2600 ps for junction temperature of Δt_{OP}= -20 to +125 degrees during operation



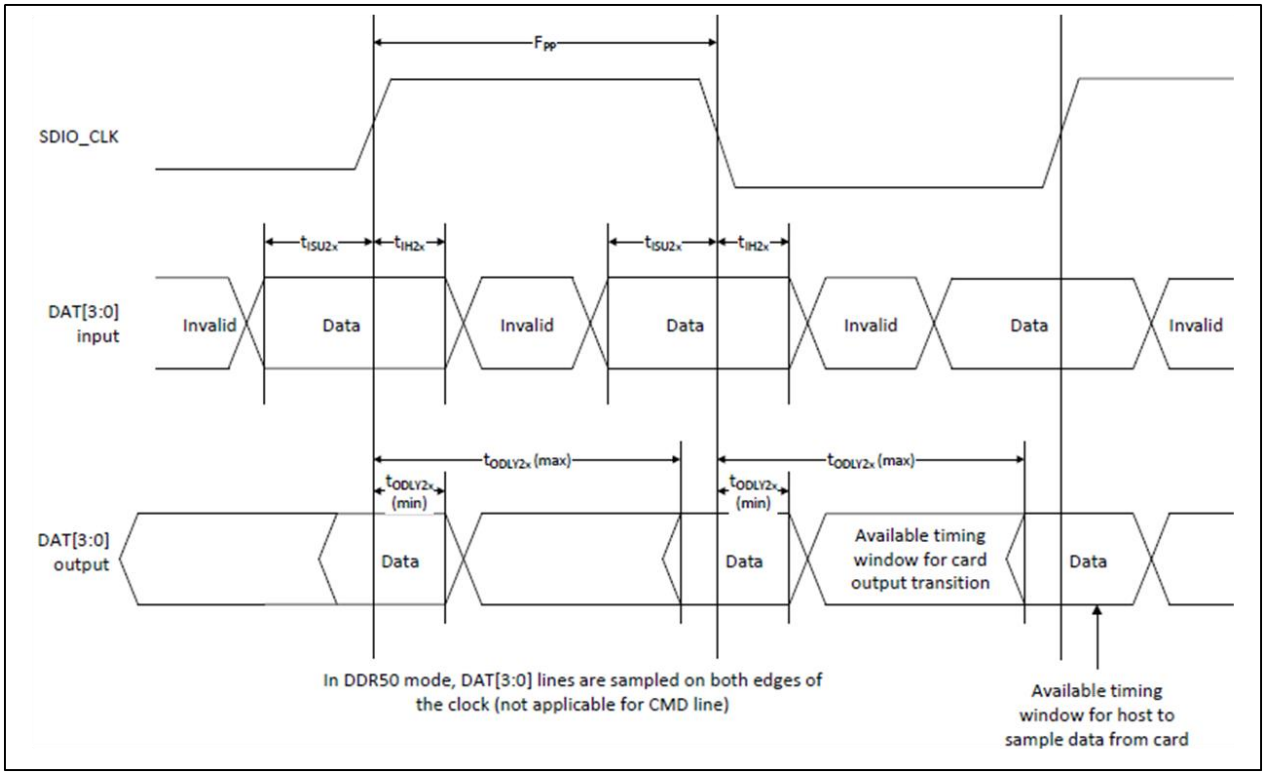
[Δt_{OP}Consideration for Variable Data Window (SDR 104 Mode)]

4.2.4 SDIO Bus Timing Specification in DDR50 Mode



Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Comments*
-	t_{CLK}	20	-	ns	DDR50 mode
-	t_{CR}, t_{CF}	-	0.2 x t_{CLK}	ns	t_{CR}, t_{CF}< 4.00ns (max) @ 100MHz, C_{CARD} = 10pF)
Clock duty cycle	-	45	55	%	-

- Data Timing, DDR50 Mode



Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Comments*
Input CMD					
Input setup time	t_{ISU}	6	-	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD} < 10pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	-	13.7	ns	C_{CARD} < 30pF (1 Card)
Output hold time	t_{OH}	1.5	-	ns	C_{CARD} < 15pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	-	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{CARD} < 10pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	-	7.5	ns	C_{CARD} < 25pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	-	ns	C_{CARD} < 15pF (1 Card)

4.3 PCM Interface

BWR-Y89359-SMA support a PCM interface that can connect to linear PCM Codec devices in master or slave mode. in master mode, the BWR-Y89359-SDA generates the PCM_DCLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BWR-Y89359-SMA.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

4.3.1 Slot Mapping

The BWR-Y89359-SMA supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8 and 16 respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tri-states its output on unused slots to allow other devices to share the PCM interface signals. The data output driver tri-states its output after the falling edge of the PCM clock during the last bit of the slot.

4.3.2 Frame Synchronization

The BWR-Y89359-SMA supports both short- and long-frame synchronization in both master and slave modes. in short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

4.3.3 Data Formatting

The BWR-Y89359-SMA may be configured to generate and accept several different data formats. For conventional narrowband speech, the BWR-Y89359-SMA uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM frame. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit or a programmed value on the output. The default format is 1-bit 2's complement data, left justified and clocked MSB first.

4.3.4 Wideband Speech Support

When the host encodes Wideband Speech (WBS) packets in transparent mode.the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate, The BWR-Y89359-SDA also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, Linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

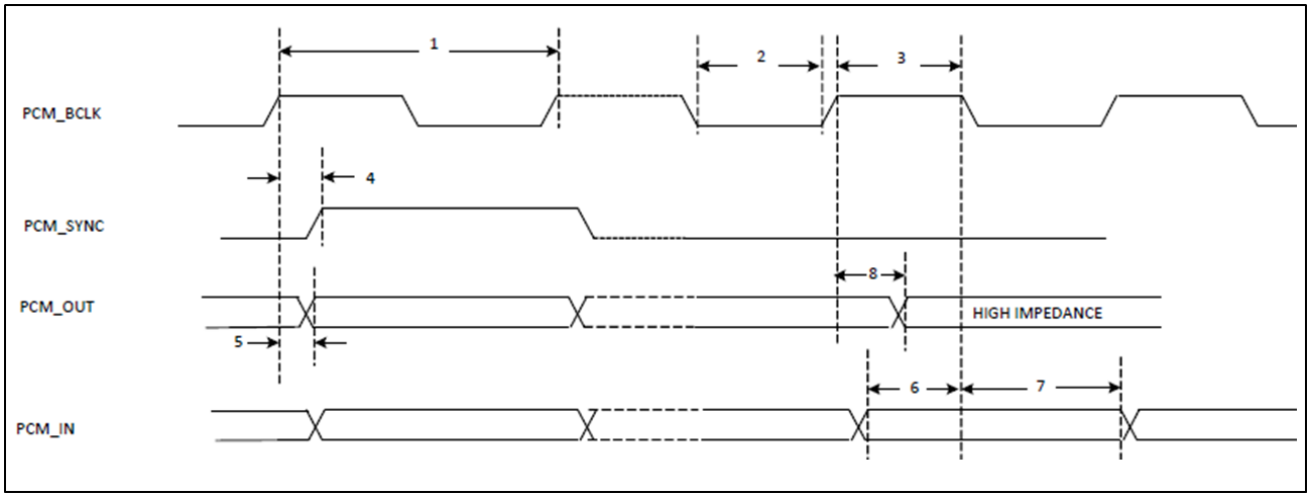
4.3.5 Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host

to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

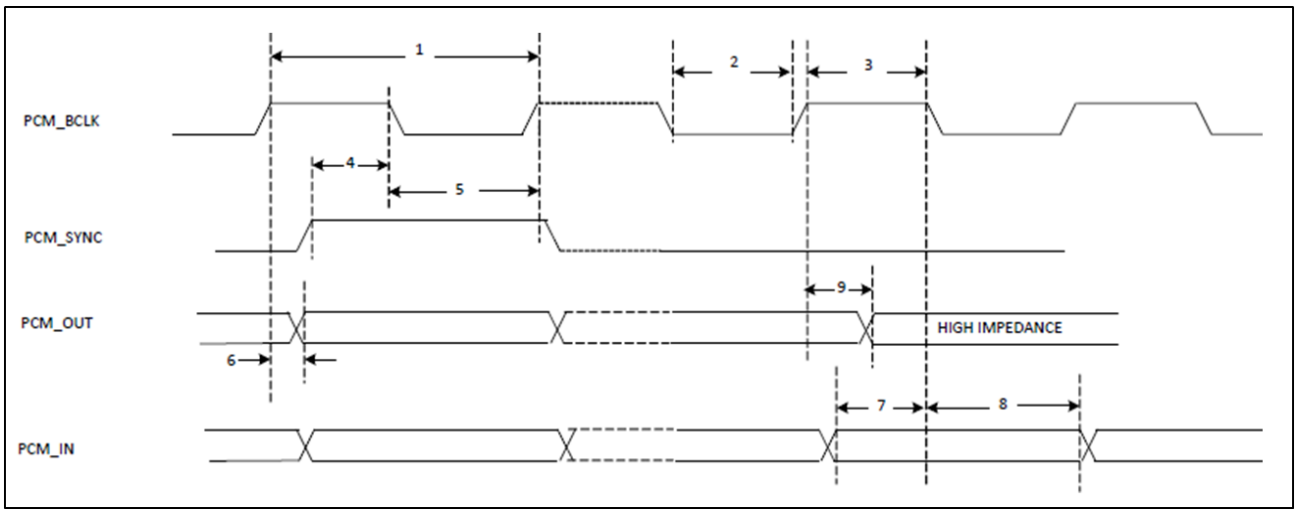
4.3.6 PCM Interface Timing

- Short Frame Snyc, Master Mode



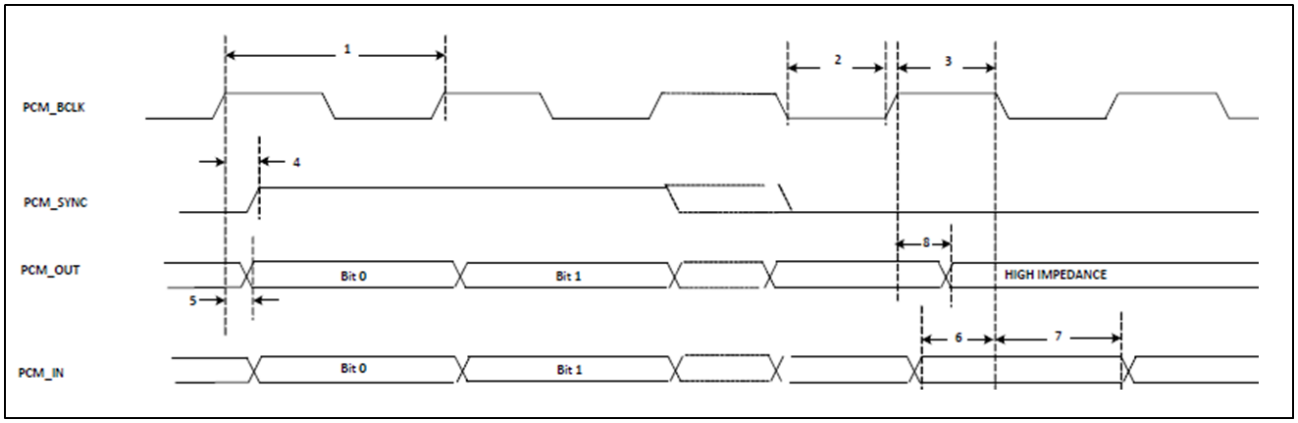
Ref No.	*Characteristics*	*Min.*	*Typ.*	*Max.*	*Unit*
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

- Short Frame Snyc, Slave Mode



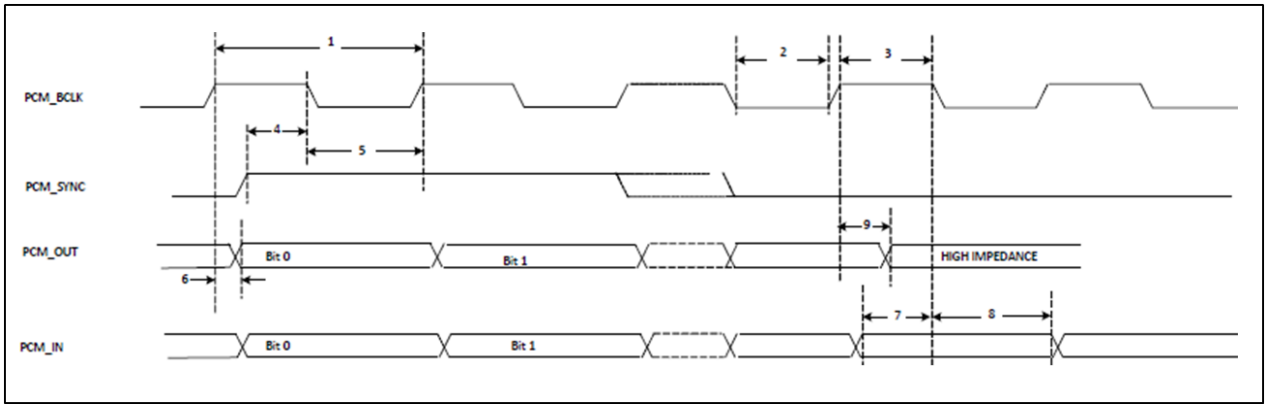
Ref No.	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

- Long Frame Sync, Master Mode



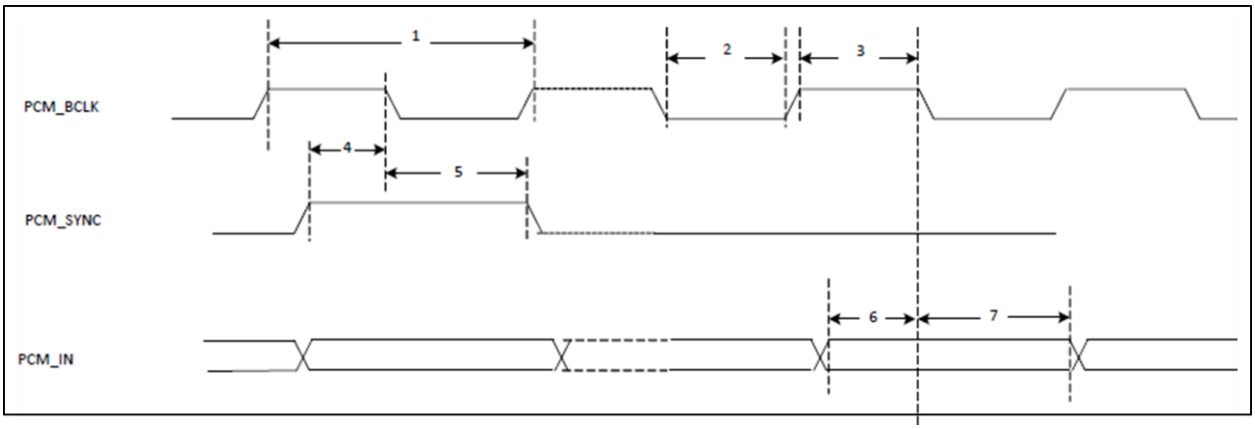
Ref No.	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

- Long Frame Sync, Slave Mode



Ref No.	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

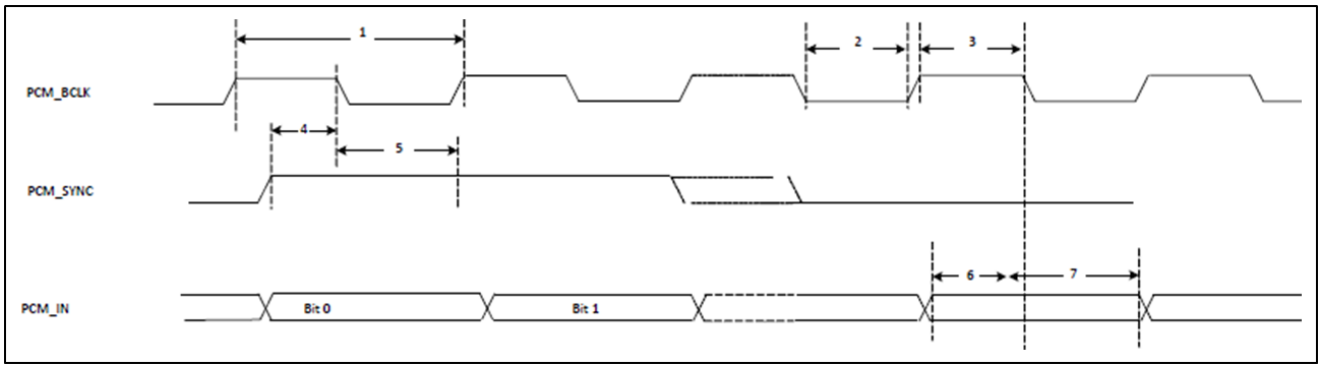
- Short Frame Sync, Burst Mode



Ref No.	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock LOW	20.8	-	-	ns
3	PCM bit clock HIGH	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns

5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

- Long Frame Sync, Burst Mode



Ref No.	*Characteristics*	*Min.*	*Typ.*	*Max.*	*Unit*
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock LOW	20.8	-	-	ns
3	PCM bit clock HIGH	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

4.4 I2S Interface

The BWR-Y89359-SMA supports I^2S digital audio port for Bluetooth audio. The I^2S signals are :

- I^2S clock : BT_I2S_CLK
- I^2S Word Select : BT_I2S_WS
- I^2S Data Out : BT_I2S_DO
- I^2S Data In : BT_I2S_DI

BT_I2S_CLK and BT_I2S_WS beome ooutputs in master mode and inputs in slave mode, whereas BT_I2S_DO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I^2S bus, in accord with the I^2S specification. The MSB of each data word is transmitted one bit clock cycle after the BT_I2S_WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when BT_I2S_WS is low,and right-channel data is transmitted when BT_I2S_WS is high.

Data bits sent by the BWR-Y89359-SMA are synchronized, with the falling edge of BT_I2S_CLK and should be sampled by the receiver on the rising edge of BT_I2S_CLK.

The clock rate in master mode is either of the following :

48kHz x 32 bits per frame = 1.536MHz

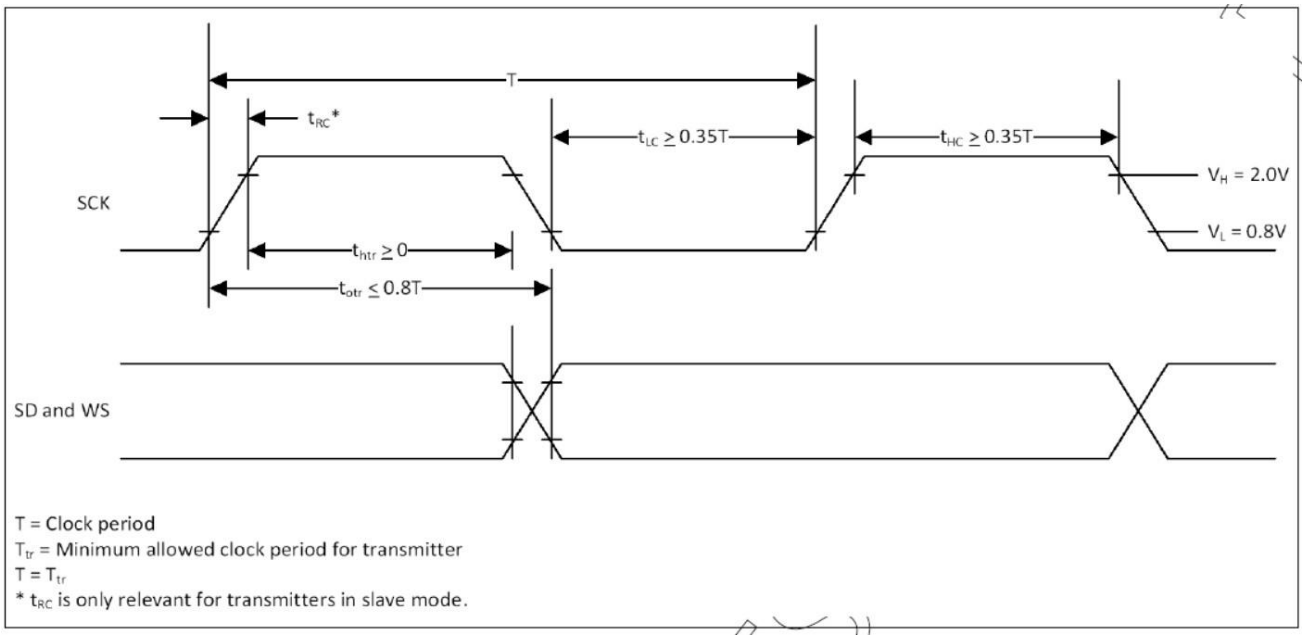
48kHz x 50 bits per frame = 2.400MHz

The master clock is generated from the input reference clock using a N/M clock divider.

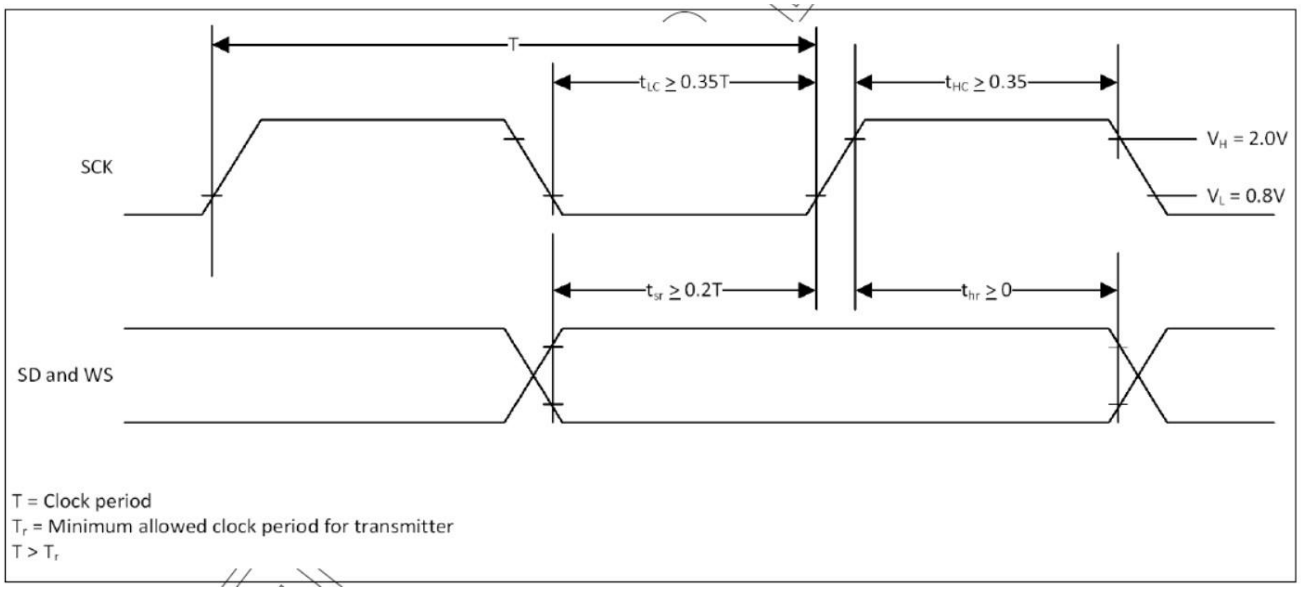
In the slave mode, any clock rate is supported to a maximum of 3.072MHz.

4.4.1 I²S Timing

- I²S Transmitter Timing



- I²S Receiver Timing



- Timing for I²S Transmitters and Receivers

	Transmitter				Receiver				
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Notes
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	d
Transmitter									
Delay t_{dtr}	–	–	–	$0.8T$	–	–	–	–	e
Hold time t_{htr}	0	–	–	–	–	–	–	–	d
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	f
Hold time t_{hr}	–	–	–	–	–	0	–	–	f

a. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.

b. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.

c. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.

d. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than 0.15 T_{tr}.

e. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.

f. The data setup and hold time must not be less than the specified receiver setup and hold time.

5. DC Characteristics

5.1 Absolute Maximum Ratings

- **Caution!** The absolute maximum ratings indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Rating	*Symbol*	*Value*	*Unit*
DC supply voltage for VDD (main source)	VDD	-0.5 to +6.0	V
DC supply voltage for SDIO interface	VIO	-0.5 to 3.9	V
Maximum undershoot voltage for I/O[a]	$V_{undershoot}$	-0.5	V
Maximum overshoot voltage for I/O[a]	$V_{overshoot}$	VDD+0.5	V
Maximum junction temperature	T_j	125	℃

a. Duration not to exceed 25% of the duty cycle.

5.2 Environmental Ratings

Characteristic	*Value*	*Units*	*Conditions/Comments*
Ambient Temperature(T_A)	-40 to +85	℃	Functional operation[a]
Storage Temperature	-40 to +125	℃	-
Operating Temperature	-40 to +80	℃	
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

5.3 Recommended Operating Conditions and DC Characteristics

System operating conditions of the wifi module	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
DC supply voltage for VDD (System operating conditions of the wifi module)	VDD	3.1	3.3	3.5	V
VDD ripple voltage tolerance (Rippledoesnot exceed theconditionof3.15V ~ 3.5V)	Vp-p	-	-	0.2	V
DC supply Voltage for VIO_SD (System operating conditions of the wifi module)	VIO_SD	1.7	1.8	1.9	V
VIO_SD ripple voltage tolerance (Rippledoesnot exceed theconditionof1.73V ~ 1.87V)	Vp-p	-	-	0.1	V
SDIO interface I/O Pins (VDDIO_SD = 1.8V)					
Input high voltage	VIH	1.27	-	-	V
Input low voltage	VIL	-	-	0.58	V
Output high voltage@2mA	VOH	1.4	-	-	V
Output low voltage@2mA	VOL	-	-	0.45	V

Other Digital I/O Pins (VDDIO = 3.3V)					
Input high voltage	VIH	2.0	-	-	V
Input low voltage	VIL	-	-	0.8	V
Output high voltage@2mA	VOH	VDDIO-0.4	-	-	V
Output low Voltage@2mA	VOL	-	-	0.4	V

5.4 CurrentConsumption

Simultaneous operating conditions of BT and Wifi	*Max. Current*	*Unit*
Max. Current Consumption @ VDD	820	mA
Max. Current Consumption @ VIO_SD	40	mA

Wifi only operating conditions	*Max. Current*	*Unit*
Max. Current Consumption @ VDD	700	mA
Max. Current Consumption @ VIO_SD	40	mA

BT only operating conditions	*Max. Current*	*Unit*
Max. Current Consumption @ VDD	100	mA
Max. Current Consumption @ VIO_SD	40	mA

6. RF Specifications

6.1 Bluetooth RF Specifications

Items	Contents			
Bluetooth specification(power class)	Version 4.2 Class2			
Channelfrequency (spacing)	2402 to 2480MHz(1MHz)			
Current Consumption	**Min.**	**Typ.**	**Max.**	**unit**
(a)Tx=Rx=DH5 (fully occupied)	-	-	100	mA
(b)Tx=Rx=2DH5 (fully occupied)	-	-	100	mA
(c)Tx=Rx=3DH5 (fully occupied)	-	-	100	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
OutputPower	0	-	+4	dBm
Frequency range	2400	-	2483.5	MHz
20dBbandwidth	-		1	MHz
AdjacentChannelPower				
(a) [M-N] =2	-	-	-20	dBm
(b) [M-N]≥3	-	-	-40	dBm
Modulation characteristics				
(a) Modulation Δf1avg	140	-	175	kHz
(b) ModulationΔf2max	115		-	kHz
(c) ModulationΔf2avg/Δf1avg	80	-	-	%
Initial Carrier Frequency Tolerance	-65		65	KHz
Carrier Frequency Drift				
(a) 1slot	-25	-	+25	kHz
(b) 3slot/ 5slot	-40	-	+40	kHz
(c) Maximumdrift rate	-20	-	+20	kHz/50us
EDR Relative Power	-4	-	+1	dB
EDR Carrier Frequency Stability and ModulationAccuracy				
(a)ωi	-75	-	+75	kHz
(b)ωi+ωo	-75	-	+75	kHz
(c)ωo	-10	-	+10	kHz
(d)RMSDEVM (DQPSK)	-	-	20	%
(e)PeakDEVM (DQPSK)	-	-	35	%
(f)99%DEVM (DQPSK)	-	-	30	%
(g)RMSDEVM (8DPSK)	-	-	13	%
(h)PeakDEVM (8DPSK)	-	-	25	%

(i) 99%DEVM(8DPSK)	-	-	20	%
SpuriousEmissions (BW=100kHz)				
(a) 10MHz≦f<2387MHz	-	-	-36	dBm
(b) 2387MHz≦f<2400MHz	-	-	-30	dBm
(c) 2483.5MHz<f≦2496.5MHz	-	-	-47	dBm
(d) 2496.5MHz<f≦8GHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**unit**
Sensitivity (BER≤0.1%)	-	-	-81	dBm
C/IPerformance (BER≤0.1%) *2				
(a) co-channel	-	-	11	dB
(b)1MHz	-	-	0	dB
(c)2MHz	-	-	-30	dB
(d)3MHz	-	-	-40	dB
(e)image (+4MHz)	-	-	-9	dB
(f)image +/- 1MHz	-	-	-20	dB
MaximumInputLevel(BER≤0.1%)	-20	-	-	dBm
EDR Sensitivity (BER≤0.007%)				
(a) 8DPSK	-	-	-77	dBm

6.2 WLAN RF Specifications

6.2.1 RF Characteristics for IEEE802.11b – 2.4GHz

*** Condition: 25℃, VDD = 3.3V, 11Mbps mode**

Items	**Contents**			
Specification	IEEE802.11b-2.4GHz			
Mode	DSSS/ CCK			
Channel frequency (spacing)	2412 to 2472MHz(5MHz)			
Data rate	1,2,5.5,11Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**unit**
(a)Tx mode (Continuous)	-	-	700	mA
(b) Rx mode	-	-	100	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**unit**
Power Levels	8	10	12	dBm
Spectrum Mask				
(a) 1st side lobes	-	-	-30	dBr
(b) 2nd side lobes	-	-	-50	dBr
Power-on/off ramp	-	-	2.0	usec

RF Carrier Suppression	15		-	dB
Modulation Accuracy	-	-	35	%
Spurious Emissions (BW=100kHz)				
(a) 10MHz≤f<2387MHz	-	-	-36	dBm
(b) 2387MHz≤f<2400MHz	-	-	-30	dBm
(c) 2483.5MHz<f≤2496.5MHz	-	-	-47	dBm
(d) 2496.5MHz<f≤8GHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (FER< 8%)	-	-	-84	dBm
Maximum Input Level (FER < 8%)	-10	-	-	dBm
Adjacent Channel Rejection (FER< 8%)	35	-	-	dB

6.2.2 RF Characteristics for IEEE802.11g – 2.4GHz

*** Condition: 25℃, VDD = 3.3V, 54Mbps mode**

Items	**Contents**			
Specification	IEEE802.11g-2.4GHz			
Mode	OFDM			
Channelfrequency (spacing)	2412 to 2472MHz(5MHz)			
Data rate	6,9,12,18, 24,36,48,54Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**unit**
(a)Tx mode (Continuous)	-	-	700	mA
(b) Rx mode	-	-	100	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**unit**
Power Levels	8	10	12	dBm
SpectrumMask				
(a) atfc +/- 11MHz	-	-	-20	dBr
(b) atfc +/- 20MHz	-	-	-28	dBr
(c) at fc≥+/-30MHz	-	-	-40	dBr
Constellation Error	-	-	-28	dB
SpuriousEmissions (BW=100kHz)				
(a) 10MHz≦f<2387MHz	-	-	-36	dBm
(b) 2387MHz≦f<2400MHz	-	-	-30	dBm
(c) 2483.5MHz<f≦2496.5MHz	-	-	-47	dBm
(d) 2496.5MHz<f≦8GHz	-	-	-47	dBm

Receiver	Min.	Typ.	Max.	unit
MinimumInputLevel(PER ≤ 10%)	-	-	-71	dBm
MaximumInputLevel(PER≤ 10%)	-20	-	-	dBm
AdjacentChannelRejection(FER≤ 10%)	-1	-	-	dB

6.2.3 RF Characteristics for IEEE802.11n– 2.4GHz

*** Condition: 25℃, VDD = 3.3V, 65Mbps (MCS7 - HT 20MHz) mode**

Items	Contents			
Specification	IEEE802.11n-2.4GHz			
Mode	OFDM			
Channel frequency (spacing)	2412 to 2472MHz(5MHz)			
Data rate	6.5,13,19.5,26,39,52,58.5,65Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**unit**
(a) Tx mode (Continuous)	-	-	700	mA
(b) Rx mode	-	-	100	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**unit**
Power Levels	8	10	12	dBm
Spectrum Mask				
(a) at fc +/- 11MHz	-	-	-20	dBr
(b) at fc +/- 20MHz	-	-	-28	dBr
(c) at fc > +/-30MHz	-	-	-45	dBr
Constellation Error	-	-	-28	dB
Spurious Emissions (BW=100kHz)				
(a) 10MHz≤f<2387MHz	-	-	-36	dBm
(b) 2387MHz≤f<2400MHz	-	-	-30	dBm
(c) 2483.5MHz<f≤2496.5MHz	-	-	-47	dBm
(d) 2496.5MHz<f≤8GHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**unit**
Minimum Input Level (PER < 10%)	-	-	-69	dBm
Adjacent Channel Rejection (FER< 10%)	-1	-	-	dB

6.2.4 RF Characteristics for IEEE802.11a – 5GHz

*** Condition: 25℃, VDD = 3.3V, 54Mbps mode**

Items	Contents

Specification	IEEE802.11a-5GHz			
Mode	OFDM			
Channelfrequency (spacing)	5180 - 5825MHz			
Data rate	6,9,12,18, 24,36,48,54Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a)Tx mode (Continuous)	-	-	700	mA
(b) Rx mode	-	-	110	mA
Transmitter	Min.	Typ.	Max.	**Unit**
Power Levels	8	10	12	dBm
SpectrumMask				
(a) atfc +/- 11MHz	-	-	-20	dBr
(b) atfc +/- 20MHz	-	-	-28	dBr
(c) at fc>+/-30MHz	-	-	-40	dBr
Constellation Error	-	-	-28	dB
SpuriousEmissions (BW=100kHz)				
(a) 10MHz≦f<2387MHz	-	-	-36	dBm
(b) 2387MHz≦f<2400MHz	-	-	-30	dBm
(c) 2483.5MHz<f≦2496.5MHz	-	-	-47	dBm
(d) 2496.5MHz<f≦8GHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
MinimumInputLevel(PER ≤ 10%)	-	-	-71	dBm
AdjacentChannelRejection (FER≤ 10%)	-1	-	-	dB

6.2.5 RF Characteristics for IEEE802.11n(HT 20MHz)– 5GHz

*** Condition: 25℃, VDD = 3.3V, 65Mbps (MCS7-HT20MHz)**

Items	**Contents**			
Specification	IEEE802.11n-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5180 - 5825MHz			
Data rate	6.5,13,19.5,26,39,52,58.5,65Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode (Continuous)	-	-	700	mA
(b) Rx mode	-	-	110	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**

Power Levels	8	10	12	dBm
Spectrum Mask				
(a) at fc +/- 11MHz	-	-	-20	dBr
(b) at fc +/- 20MHz	-	-	-28	dBr
(c) at fc > +/-30MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-28	dB
Spurious Emissions (BW=100kHz)				
(a) 10MHz≤f<2387MHz	-	-	-36	dBm
(b) 2387MHz≤f<2400MHz	-	-	-30	dBm
(c) 2483.5MHz<f≤2496.5MHz	-	-	-47	dBm
(d) 2496.5MHz<f≤8GHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER < 10%)	-	-	-65	dBm
Adjacent Channel Rejection (FER< 10%)	-1	-	-	dB

6.2.6 RF Characteristics for IEEE802.11n(HT 40MHz) – 5GHz

*** Condition: 25℃, VDD = 3.3V, 135Mbps (MCS7-HT40MHz)**

Items	**Contents**			
Specification	IEEE802.11n-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5180 - 5825MHz			
Data rate	13.5,27,40.5,54,81,108,121.5,135Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode (Continuous)	-	-	700	mA
(b) Rx mode	-	-	130	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	6	8	10	dBm
Spectrum Mask				
(a) at fc +/- 21MHz	-	-	-20	dBr
(b) at fc +/- 40MHz	-	-	-28	dBr
(c) at fc > +/-60MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-28	dB
Spurious Emissions (BW=100kHz)				
(a) 10MHz≤f<2387MHz	-	-	-36	dBm
(b) 2387MHz≤f<2400MHz	-	-	-30	dBm

(c) 2483.5MHz<f≤2496.5MHz	-	-	-47	dBm
(d) 2496.5MHz<f≤8GHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER < 10%)	-	-	-60	dBm
Adjacent Channel Rejection (FER< 10%)	-1	-	-	dB

6.2.7 RF Characteristics for IEEE802.11ac(HT 40MHz) – 5GHz

*** Condition: 25℃, VDD = 3.3V, 180Mbps (MCS9-HT40MHz)**

Items	**Contents**			
Specification	IEEE802.11ac-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5180 - 5825MHz			
Data rate	13.5,27,40.5,54,81,108,121.5,135,162,180Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode (Continuous)	-	-	700	mA
(b) Rx mode	-	-	130	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	6	8	10	dBm
Spectrum Mask				
(a) at fc +/- 21MHz	-	-	-20	dBr
(b) at fc +/- 40MHz	-	-	-28	dBr
(c) at fc > +/-60MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-32	dB
Spurious Emissions (BW=100kHz)				
(a) 10MHz≤f<2387MHz	-	-	-36	dBm
(b) 2387MHz≤f<2400MHz	-	-	-30	dBm
(c) 2483.5MHz<f≤2496.5MHz	-	-	-47	dBm
(d) 2496.5MHz<f≤8GHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER < 10%)	-	-	-53	dBm
Adjacent Channel Rejection (FER< 10%)	-1	-	-	dB

6.2.8 RF Characteristics for IEEE802.11ac(HT 80MHz) – 5GHz

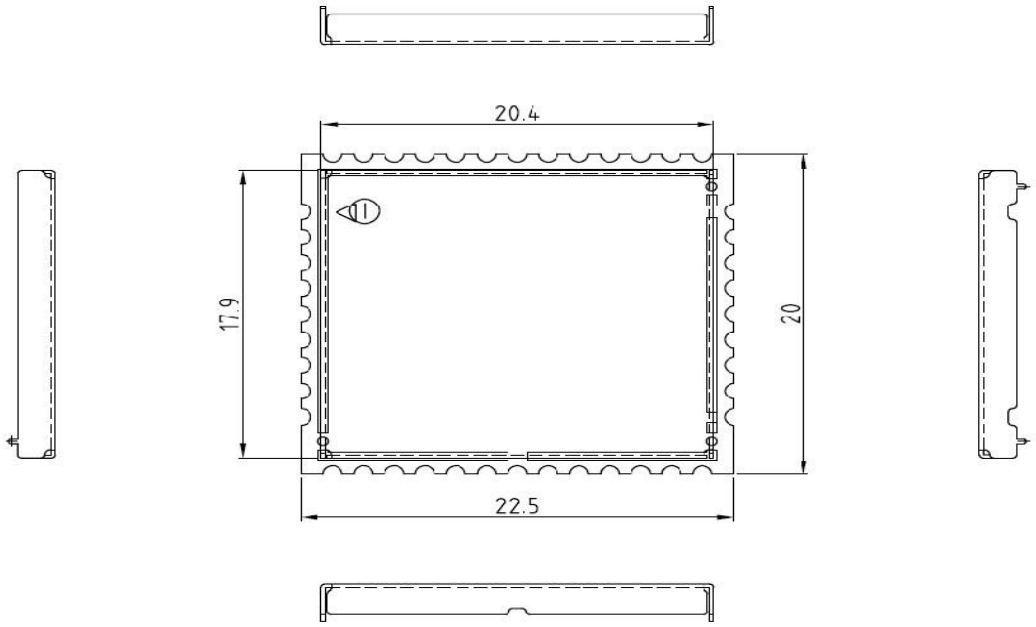
*** Condition: 25℃, VDD = 3.3V, 390Mbps (MCS9-HT80MHz)**

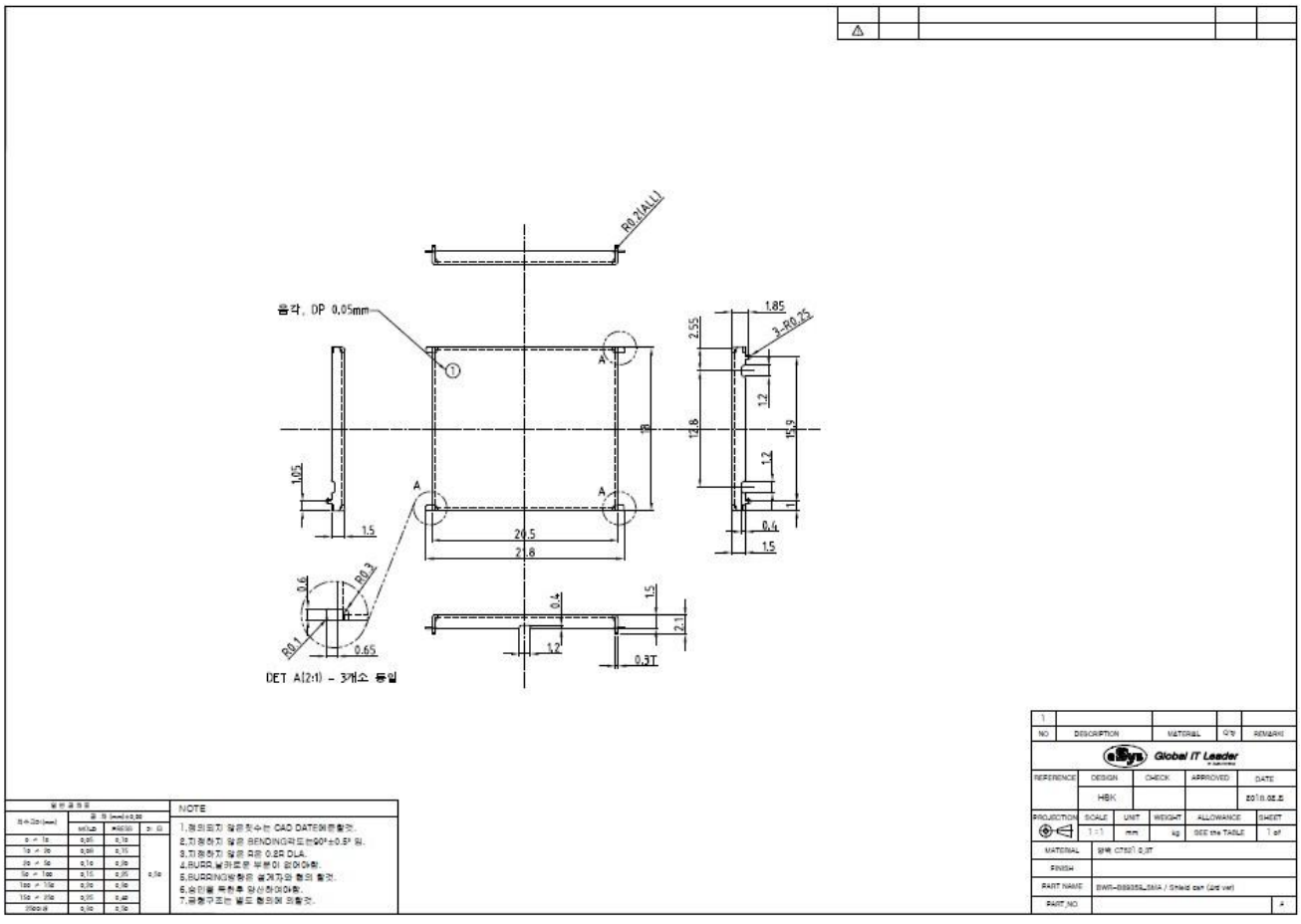
Items	**Contents**
Specification	IEEE802.11ac-5GHz

Mode	OFDM			
Channel frequency (spacing)	5180 - 5825MHz			
Data rate	29.3,58.5,87.8,117,175.5,234,263.3,292.5,351,390Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode (Continuous)	-	-	700	mA
(b) Rx mode	-	-	160	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	4.5	6.5	8.5	dBm
Spectrum Mask				
(a) at fc +/- 41MHz	-	-	-20	dBr
(b) at fc +/- 80MHz	-	-	-28	dBr
(c) at fc > +/-120MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-32	dB
Spurious Emissions (BW=100kHz)				
(a) 10MHz≤f<2387MHz	-	-	-36	dBm
(b) 2387MHz≤f<2400MHz	-	-	-30	dBm
(c) 2483.5MHz<f≤2496.5MHz	-	-	-47	dBm
(d) 2496.5MHz<f≤8GHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER < 10%)	-	-	-57	dBm
Adjacent Channel Rejection (FER< 10%)	-1	-	-	dB

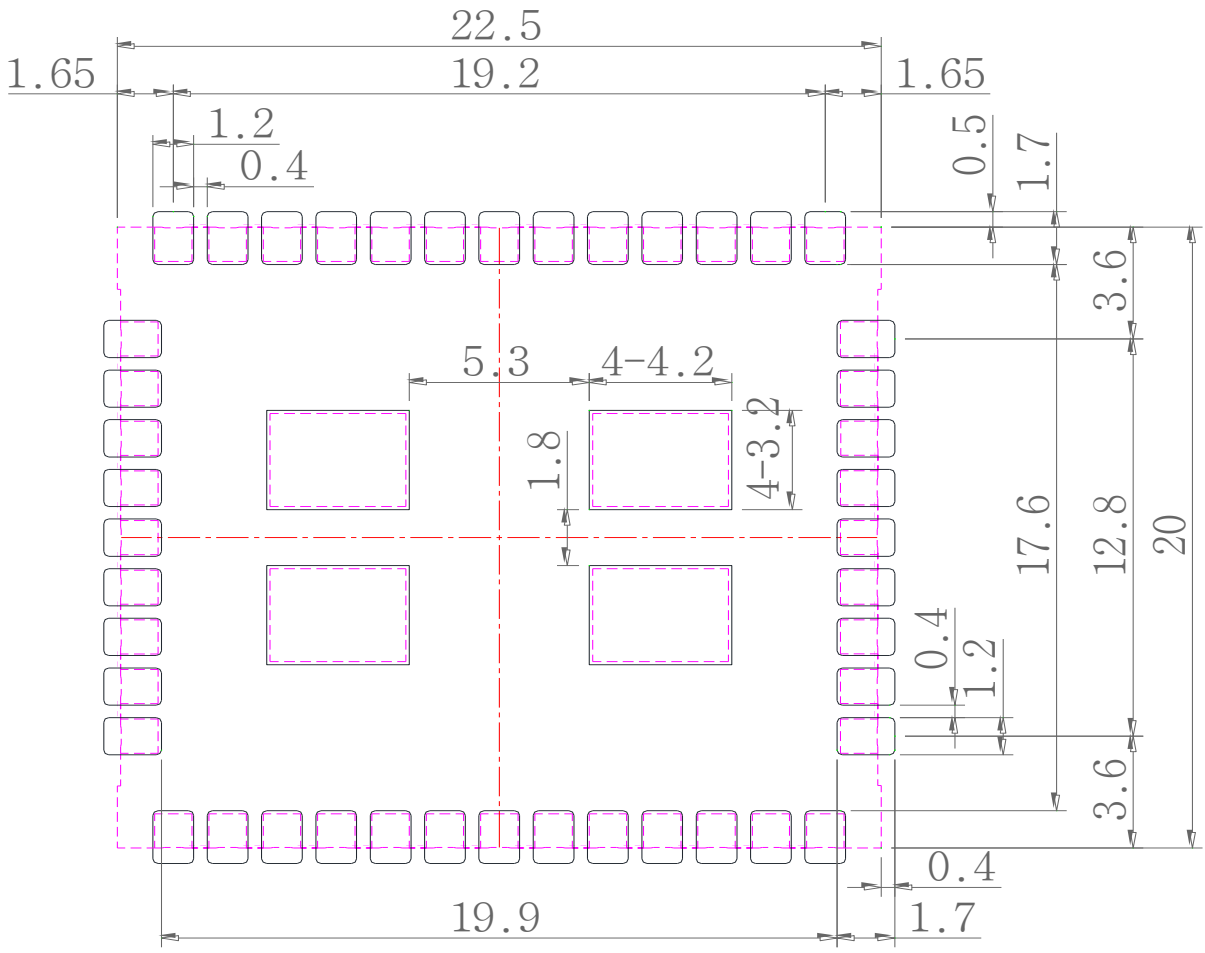
7.Mechanical Specification

7.1 Module Dimension

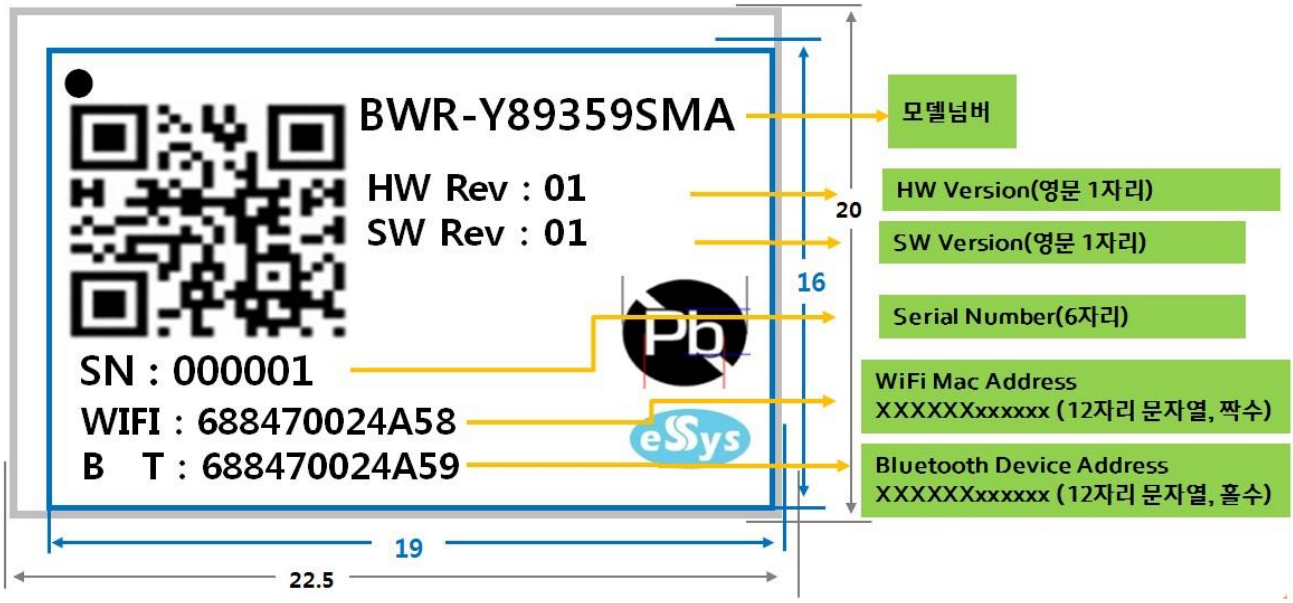




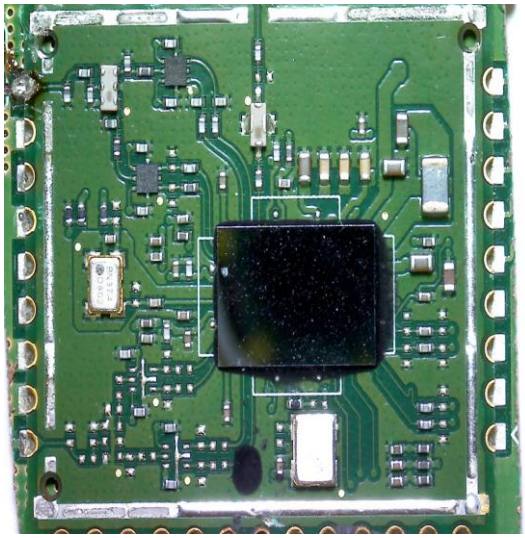
7.2 Recommended Land Pattern



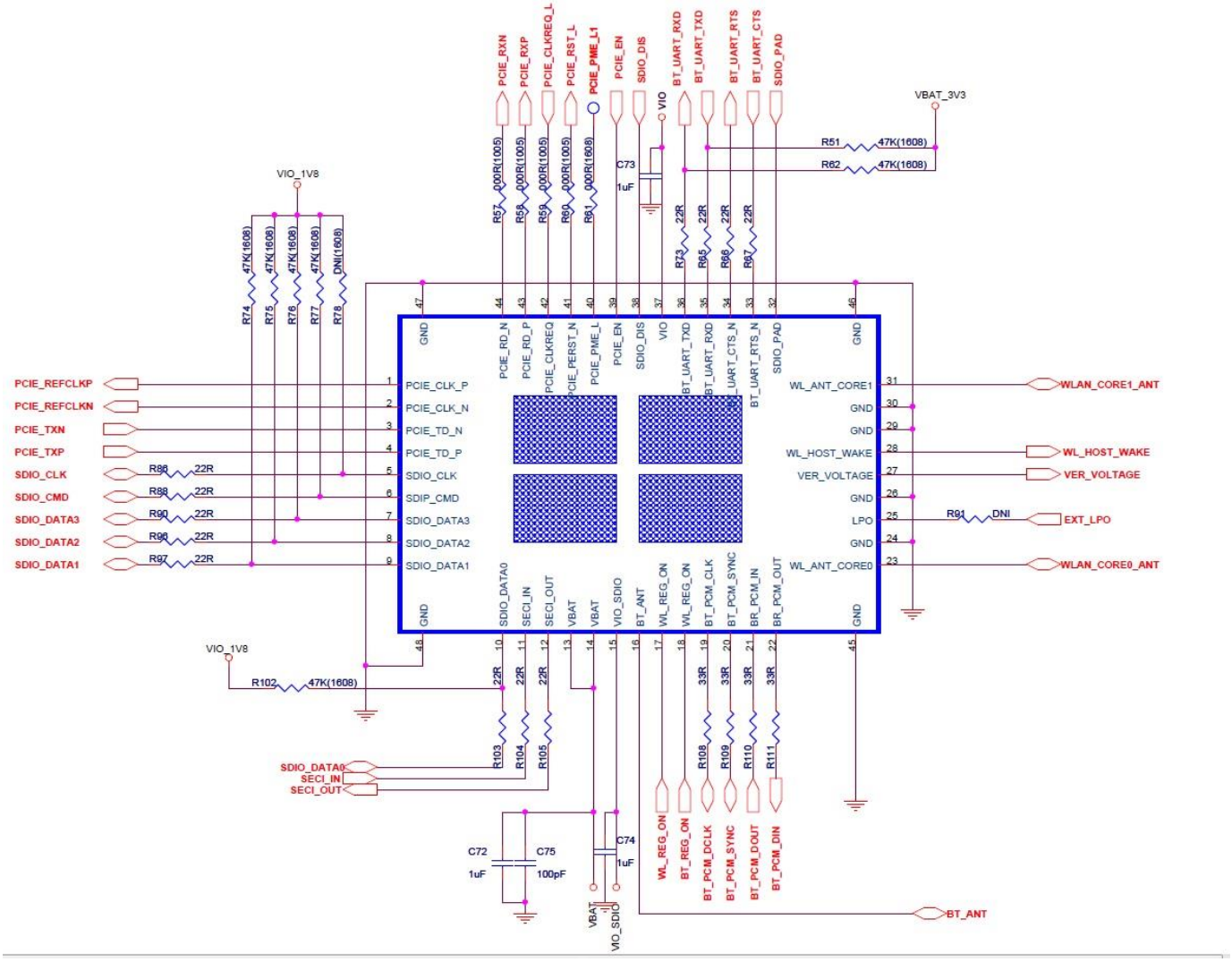
7.3 Barcode Label Specification



7.4 Product Picture

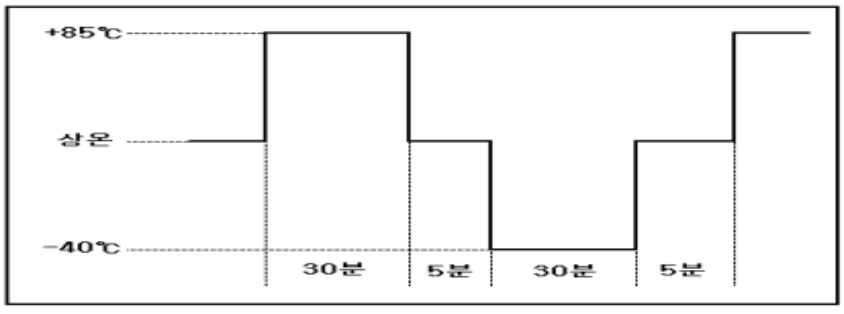


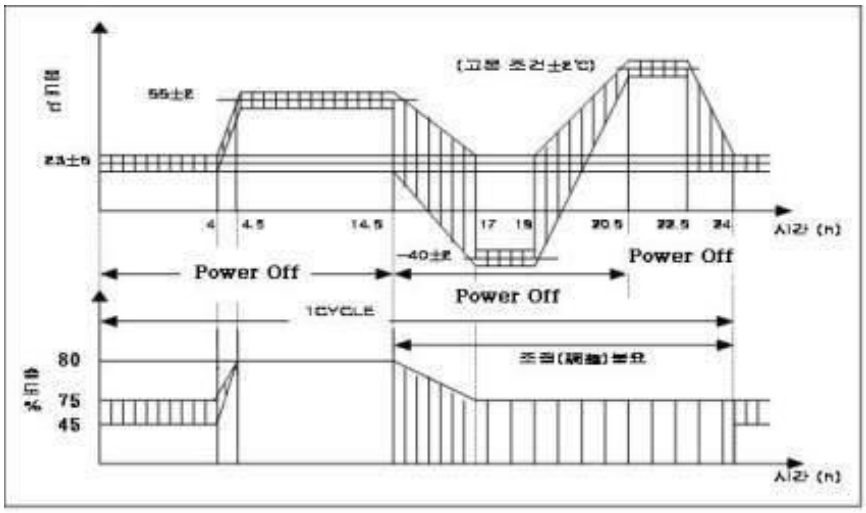
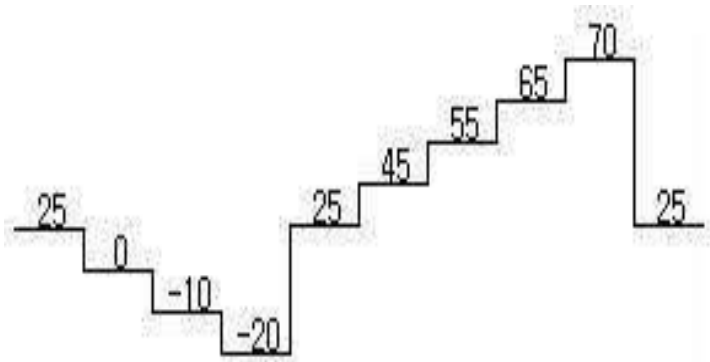
8.Application Schematic



9.Reliability Test

9.1 Reliability Test Configuration

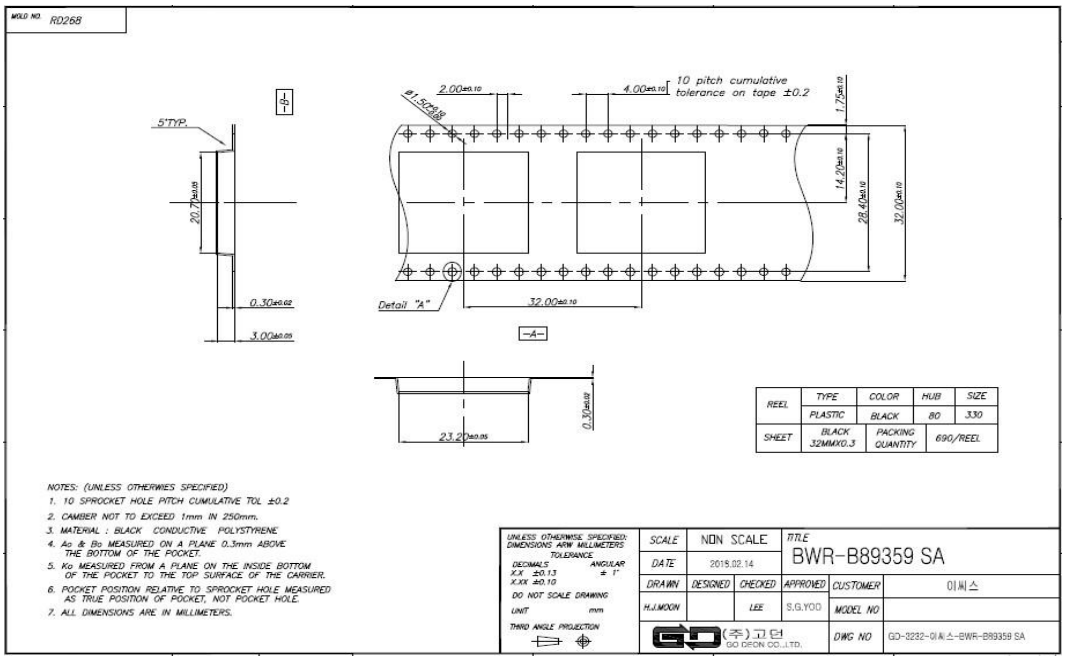
항목	판정 기준	만족여부
고온 저장	85℃ 168시간 방치 -> 2시간 상온 방치 -> 성능 테스트 후 SPEC 대비 판정	
저온 저장	-40℃ 168시간 방치 -> 2시간 상온 방치 -> 성능 테스트 후 SPEC 대비 판정	
고온 동작	70℃ 100시간 동작 -> 2시간 상온 방치 -> 성능 테스트 후 SPEC 대비 판정	
저온 동작	-20℃ 100시간 동작 -> 2시간 상온 방치 -> 성능 테스트 후 SPEC 대비 판정	
내습 동작	60℃, 80%, 48시간 동작 -> 2시간 이상 상온 방치 -> 성능 테스트 후 SPEC 대비 판정	
낙하	높이 1m에서 Random하게 10회 낙하 -> 성능 테스트 후 SPEC 대비 판정	
충격	가속도 50m/sec, 충격 시간 11msec, 각 면당 10회 실시 후 SPEC 대비 판정	
진동	주파수(10 ~ 55Hz), 가속도 4G, 3방향(X,Y,Z) 6시간 진행 후 SPEC 대비 판정	
내습 동작	60℃, 80%, 48시간 동작 -> 2시간 이상 상온 방치 -> 성능 테스트 후 SPEC 대비 판정	
열충격	시험 패턴은 그림을 따를 것 - 기본 시험 : 500 Cycle 시행 - 비전원 상태에서 시행 후 성능 SPEC에 준하여 TEST 실시 	

고온내구	85℃ 500시간 동작 -> 성능 테스트 후 SPEC 대비 판정	
상온내구	상온상습(25±5℃, 60±20%) 1500시간 작동 -> 성능 테스트 후 SPEC 대비 판정	
온 습도 싸이클 시험	고온 조건은 70℃이며, 그림의 패턴을 3Cycle 실시한다. 시험 완료되면 상온 2시간 방치 후 측정하여 SPEC 대비 판정. 	
온도 특성 시험	그림의 각 온도에서 비전원인가로 1시간 방치 후 온도 유지 상태에서 성능 TEST 실시 	

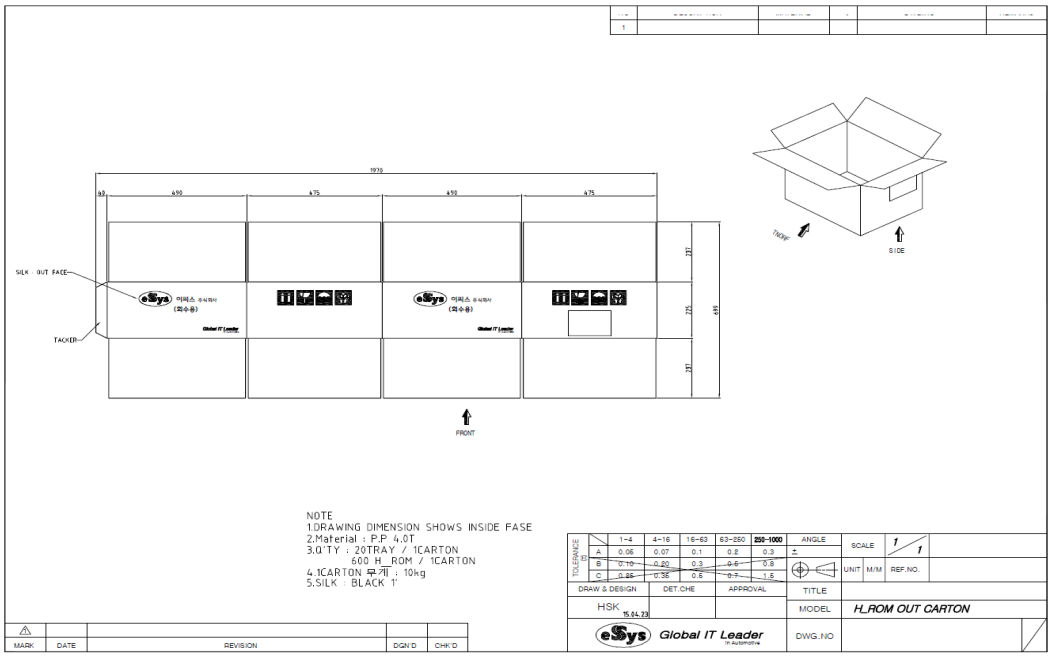
10.Delivery Information

10.1 Packing Information

■ **Reel Information**



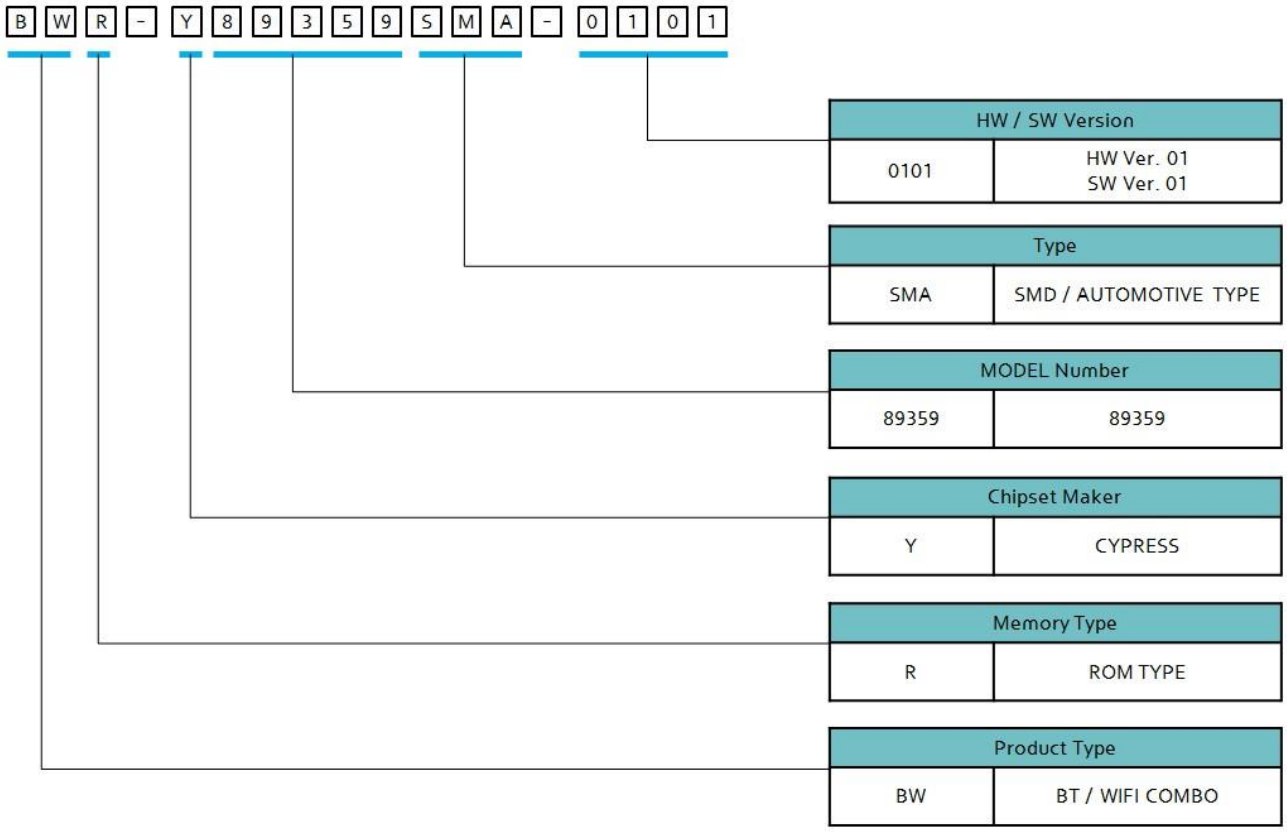
■ **Box Information**



10.2 RoHS Compliance

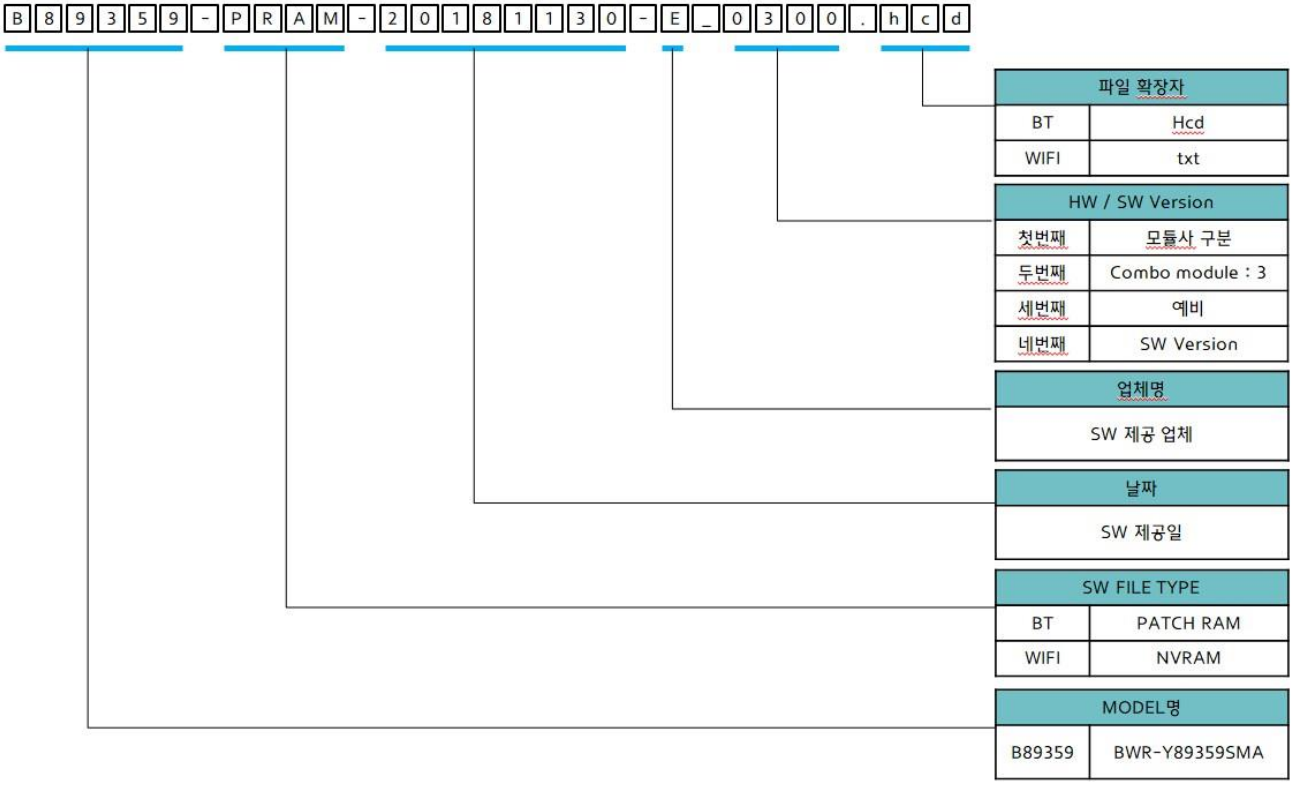
BWR-Y89359-SDAmodule meets the requirements of directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS)

10.3 Ordering Information

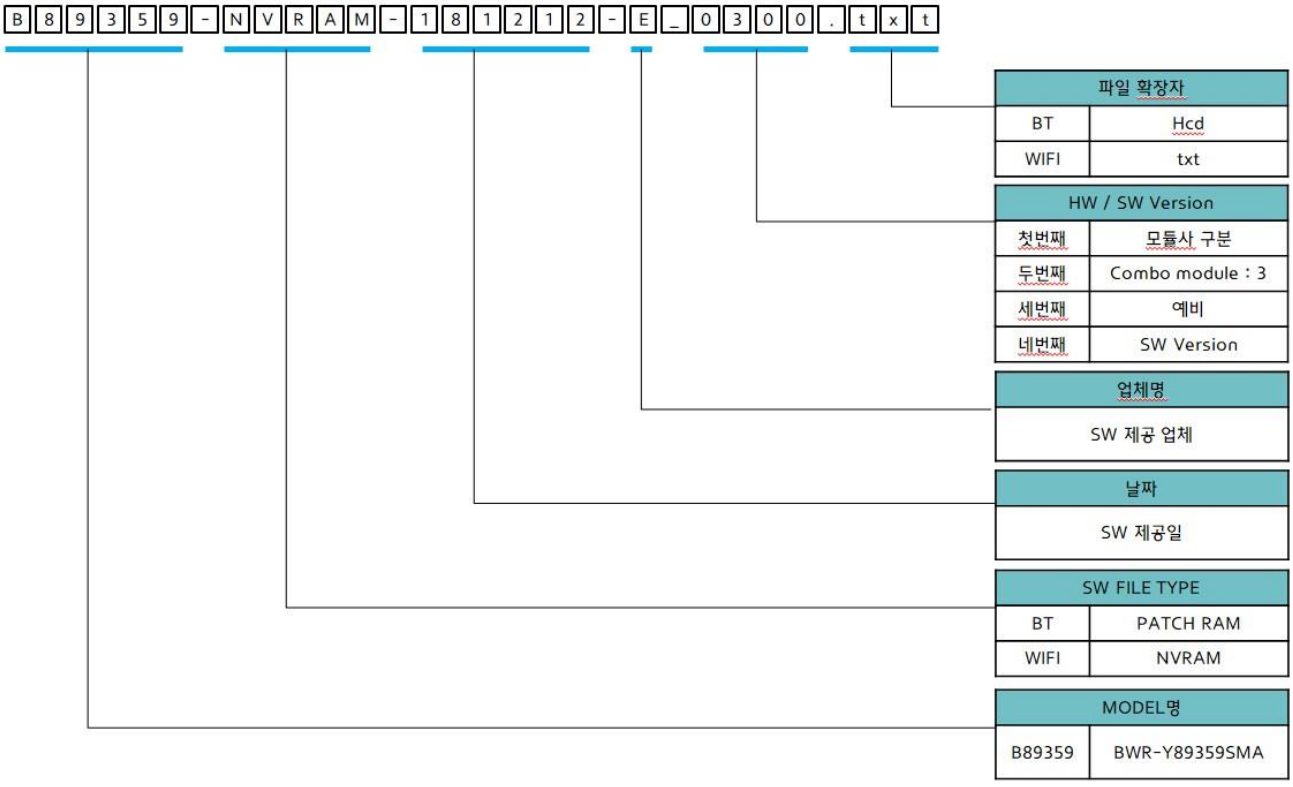


10.4 BT PATCH RAM & WiFi NVRAM File Information

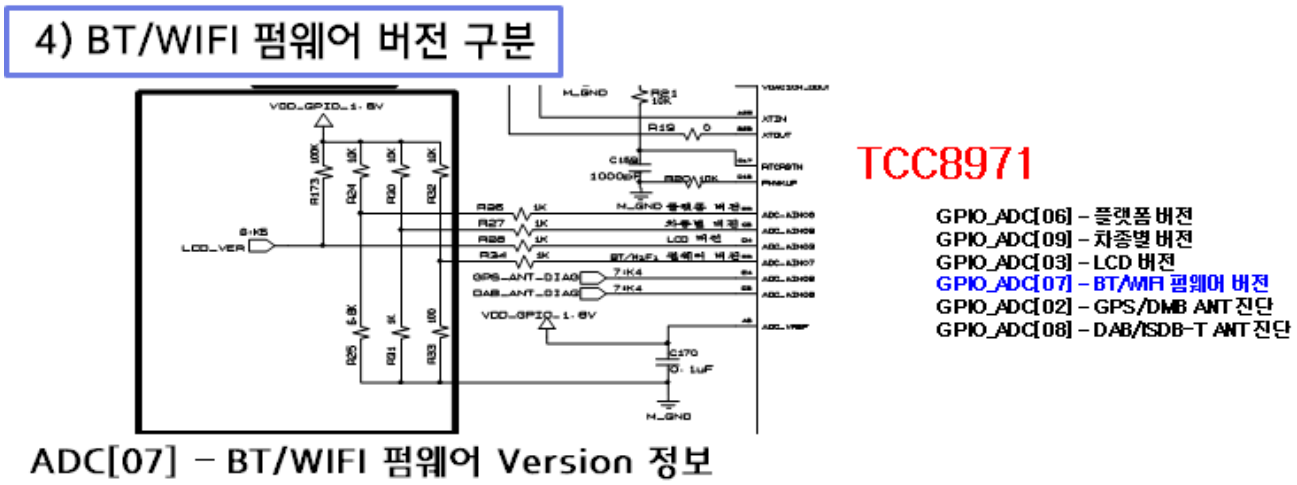
10.4.1 Bluetooth PATCH RAM File Information



10.4.2 WiFi NVRAM File Information



10.4.3 Module Version Selection Table



R33	GPIO_ADC[07] VOLTAGE	Version	비 고	모듈품번
910	0.15V (0.~0.2V)	001	LGIT 콤보 모듈	- M3012001272 - M3012001308 (NVRAM 공용 모듈)
2.2K	0.32V (0.2~0.4V)	002	Reserved	
3.9K	0.51V (0.4~0.6V)	003	Reserved	
6.8K	0.73V (0.6~0.8V)	004	Reserved	
10K	0.9V (0.8~1.0V)	005	이씨스 콤보 모듈	M3012001296
16K	1.11V (1.0~1.2V)	006	Reserved	
27K	1.13V (1.2~1.4V)	007	Reserved	
47K	1.48V (1.4~1.6V)	008	Reserved	
150K	1.69V (1.6~1.8V)	009	Reserved	

11.APPENDIX

11.1 DOCUMENT REFERENCES

Documents	*Description*
DS109-RDS	BCM89359 Preliminary Datasheet
JESD22-A114	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
IPC / JEDEC J-STD-020	Moisture / Reflow Sensitivity Classification for Non-hermitic Solid State Surface Mount Devices