

**Appendix 5.**

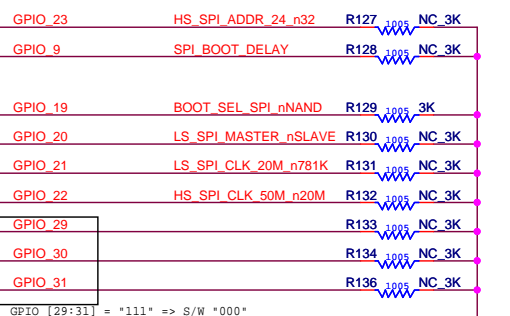
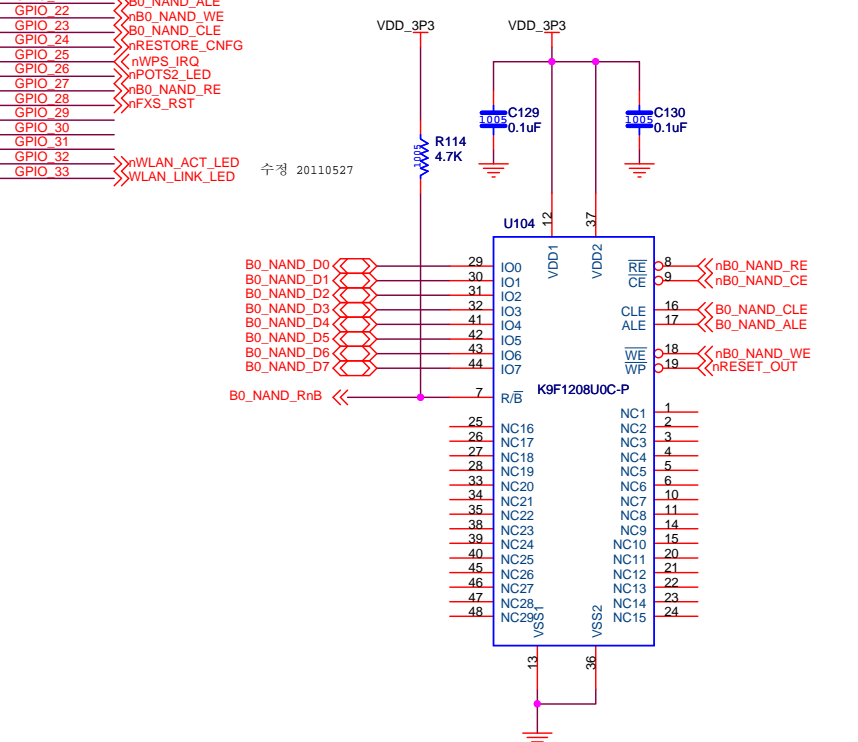
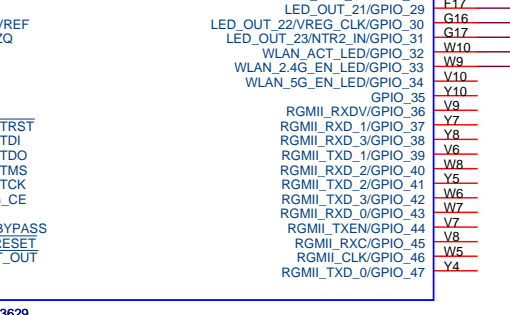
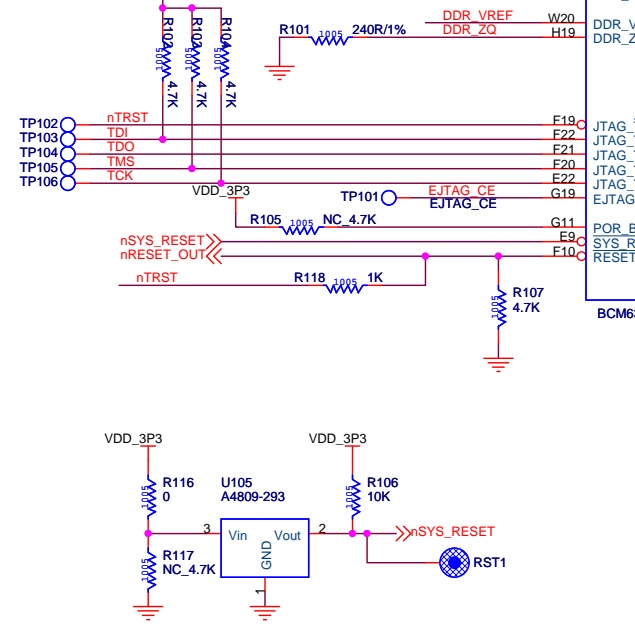
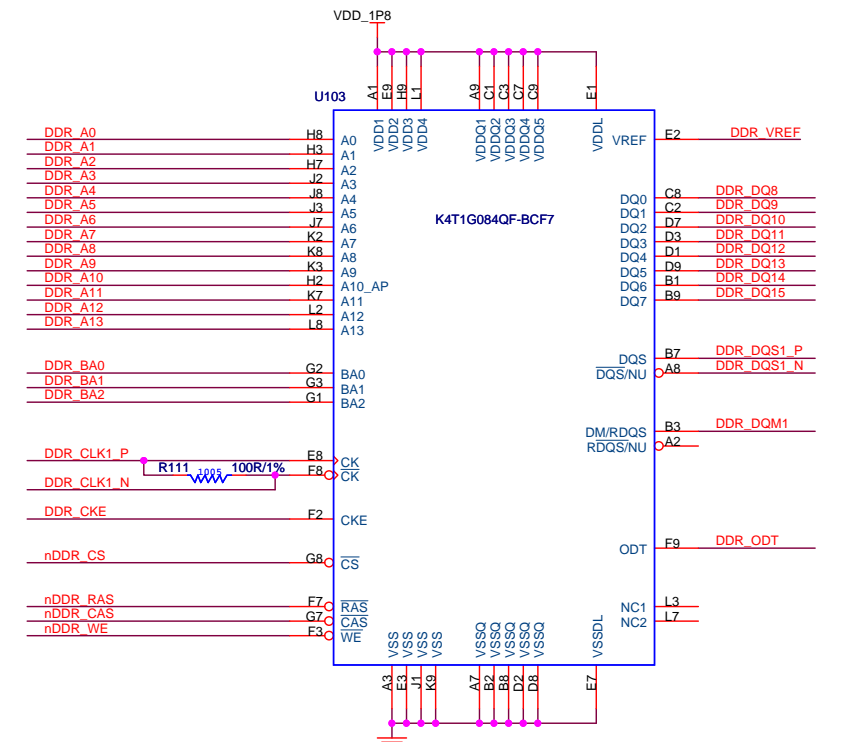
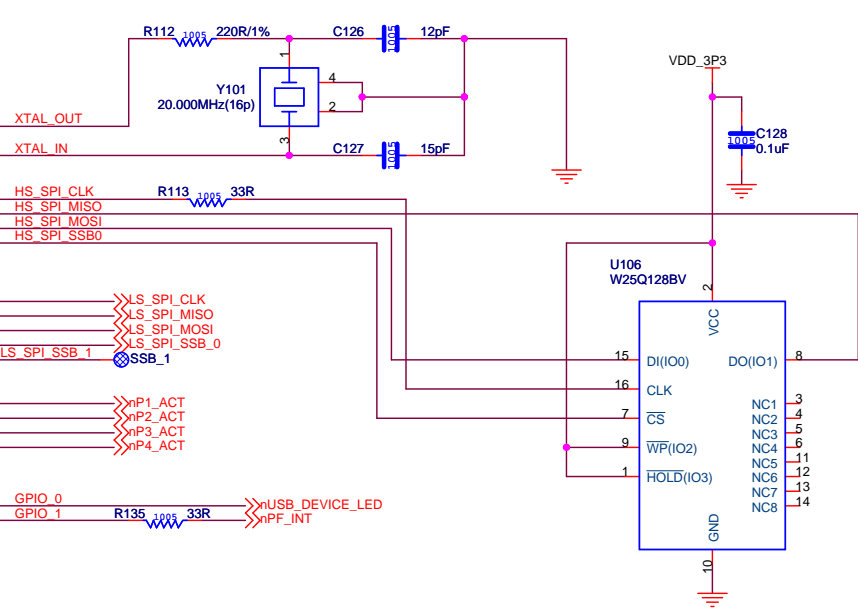
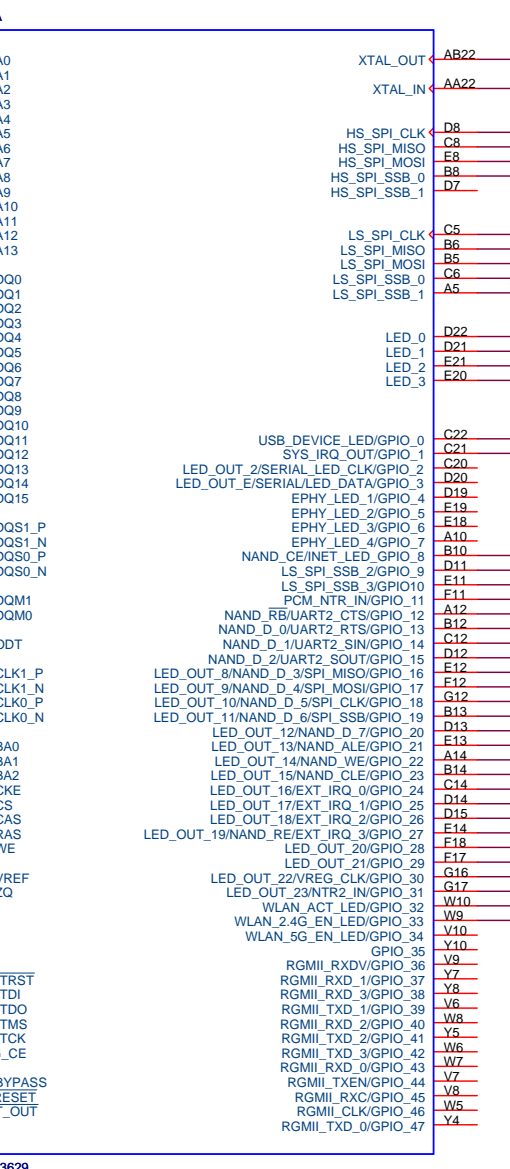
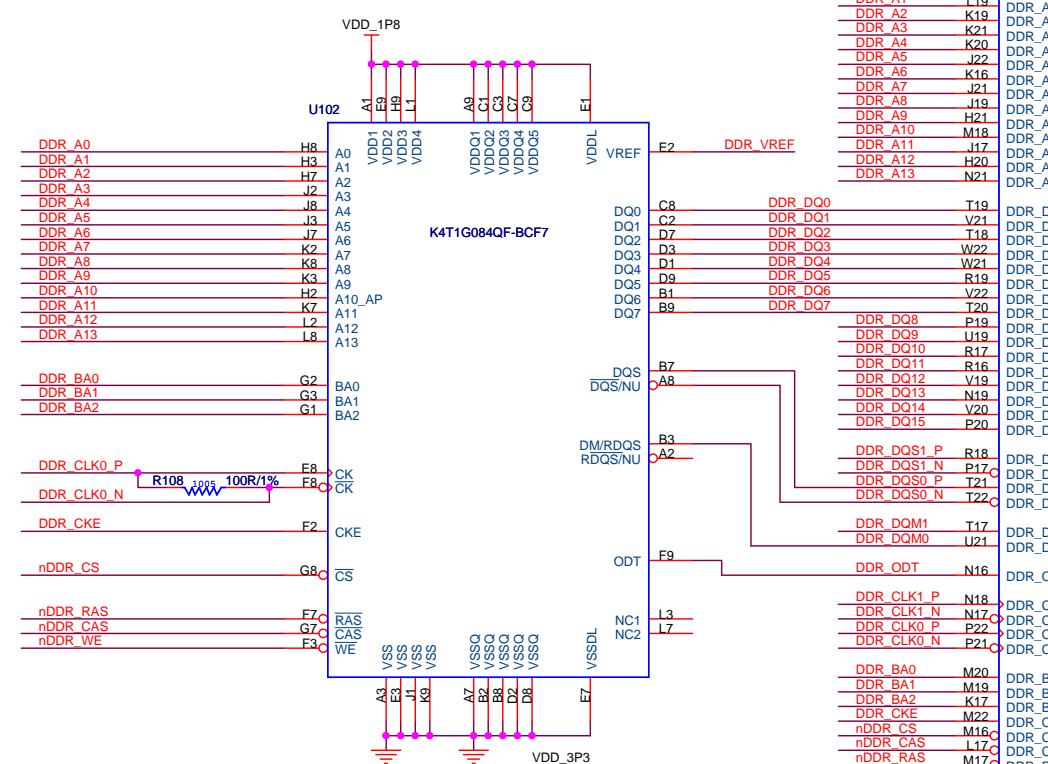
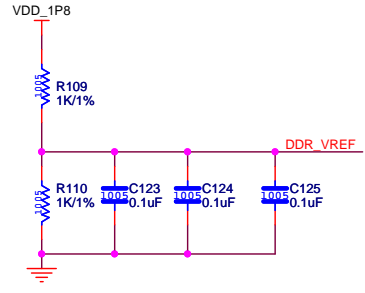
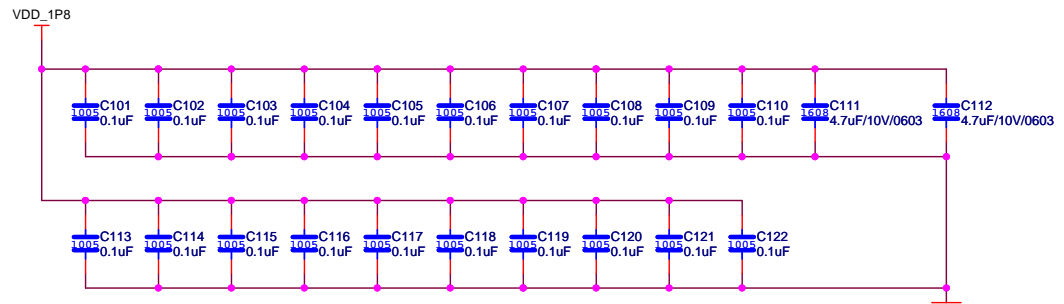
# Schematics

# ubiquoss

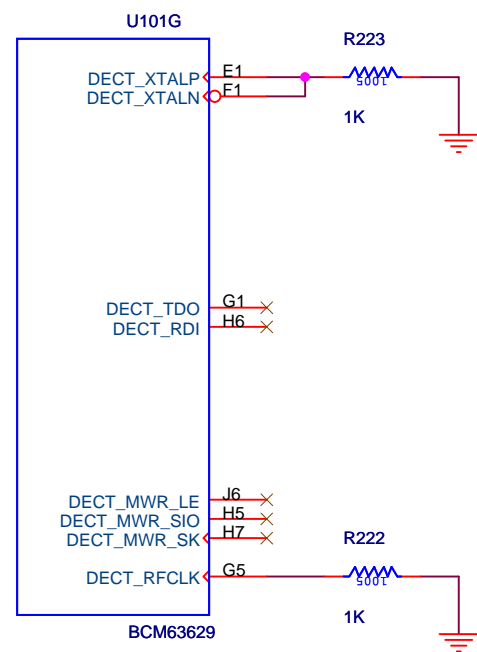
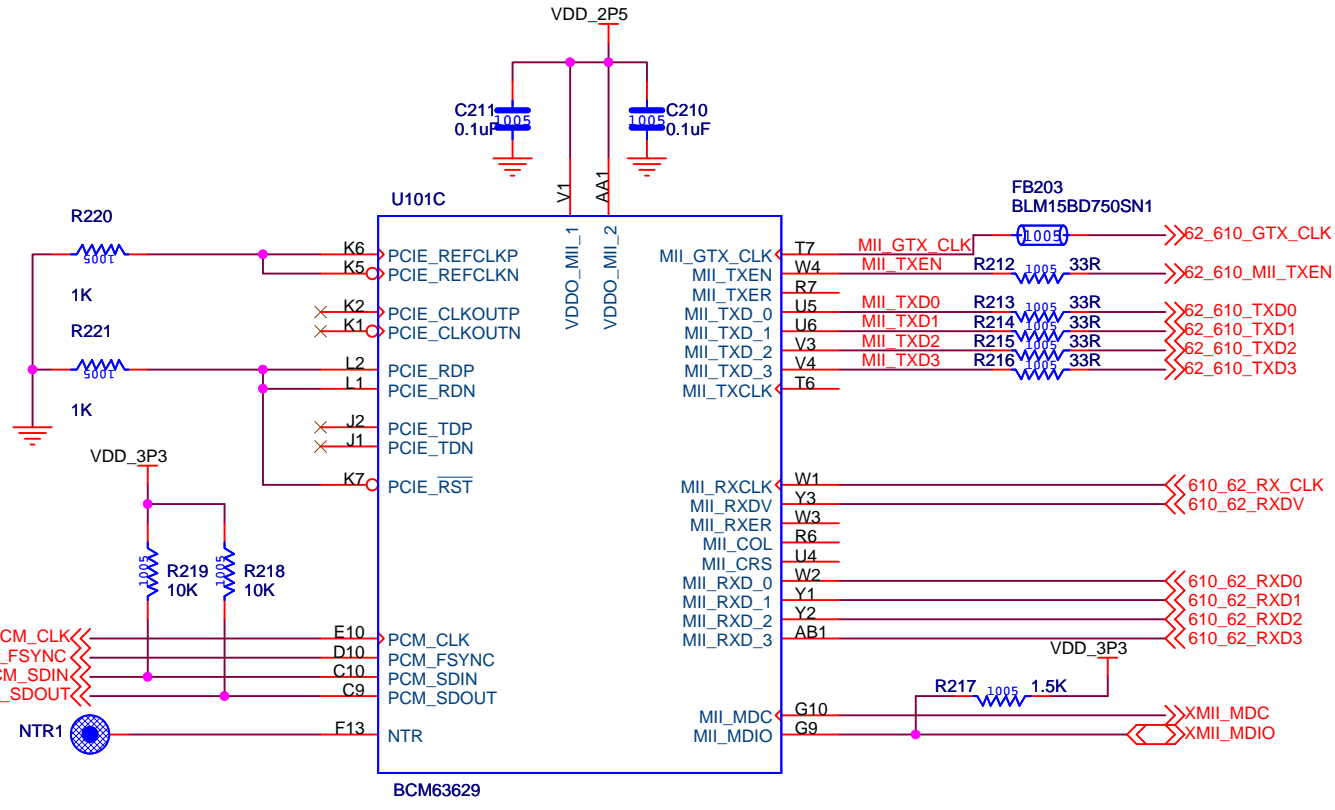
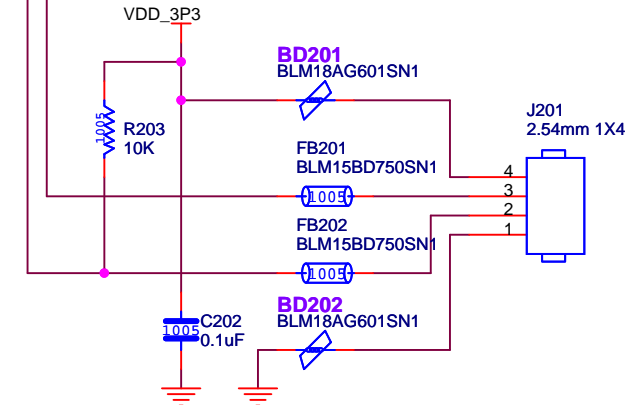
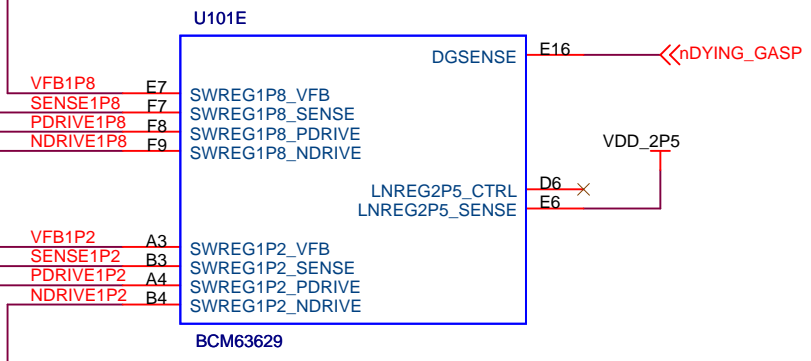
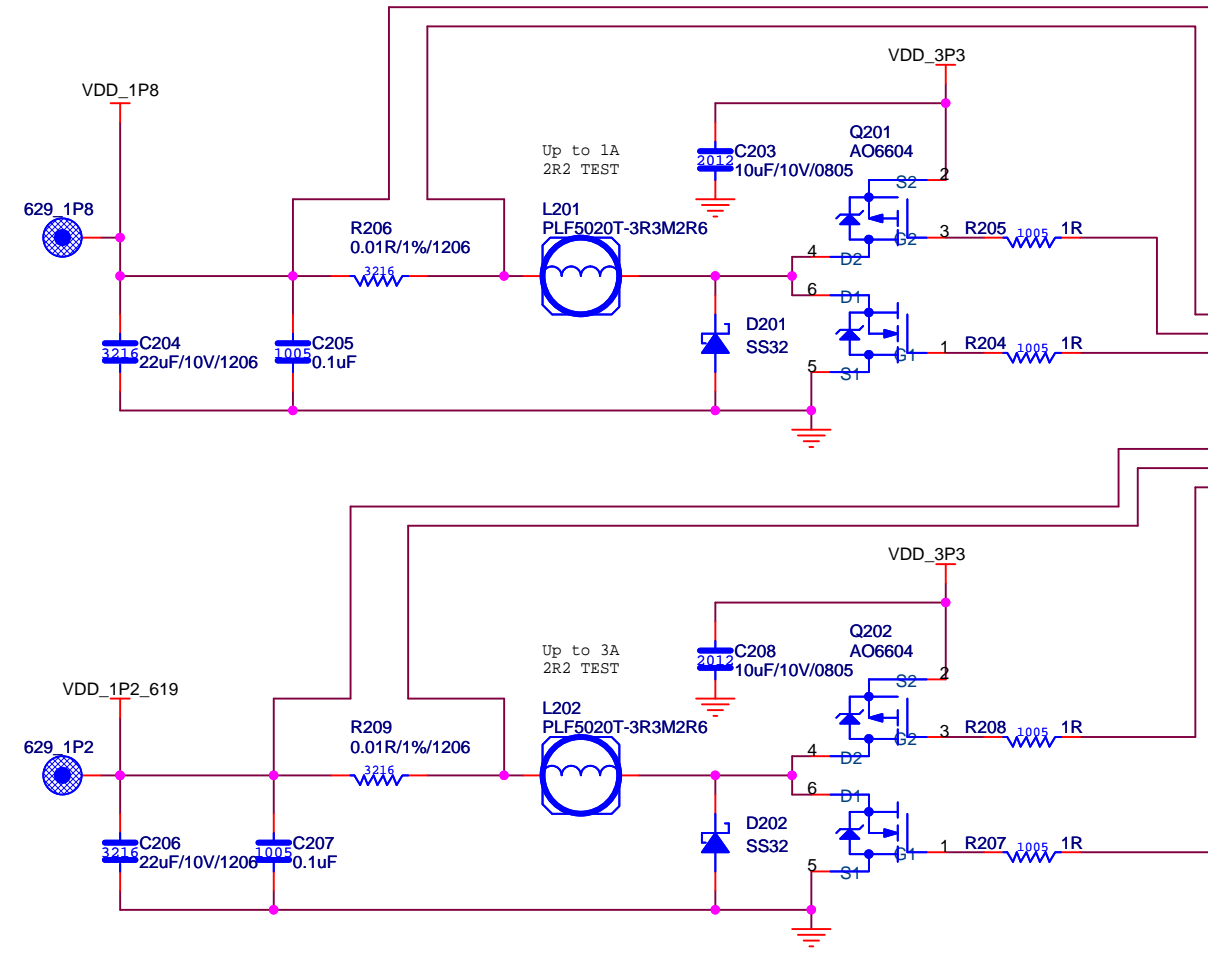
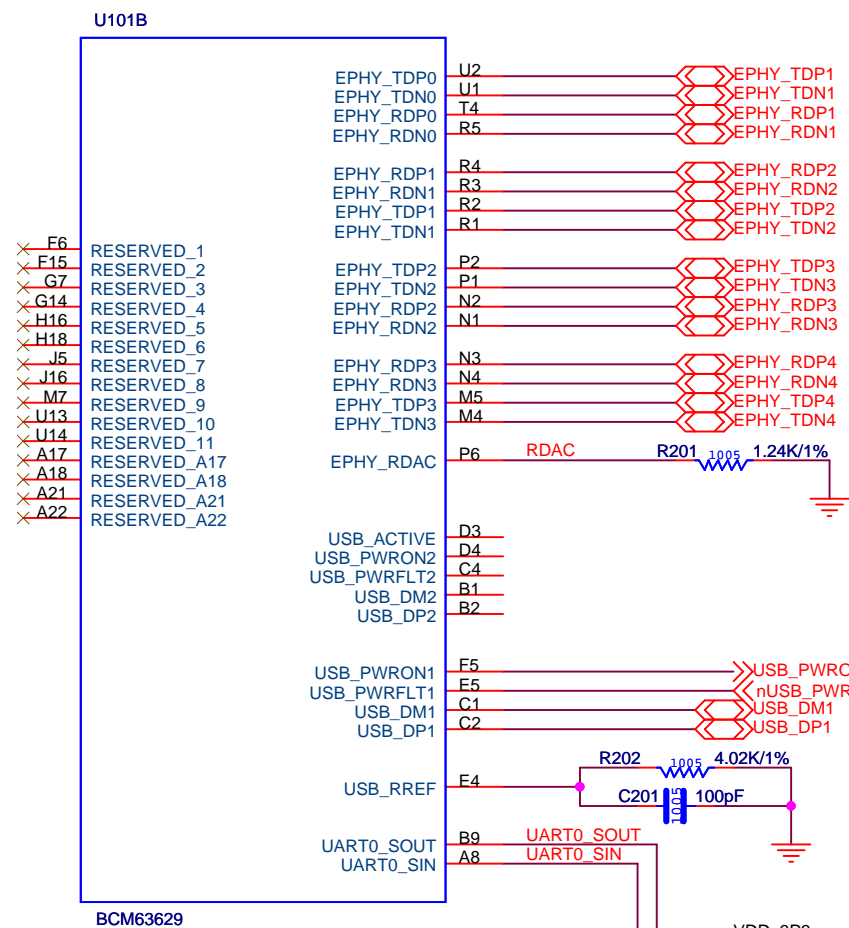
Company Confidential

Model	C524W
Version	Ver. 0.3
Date	
Designer	

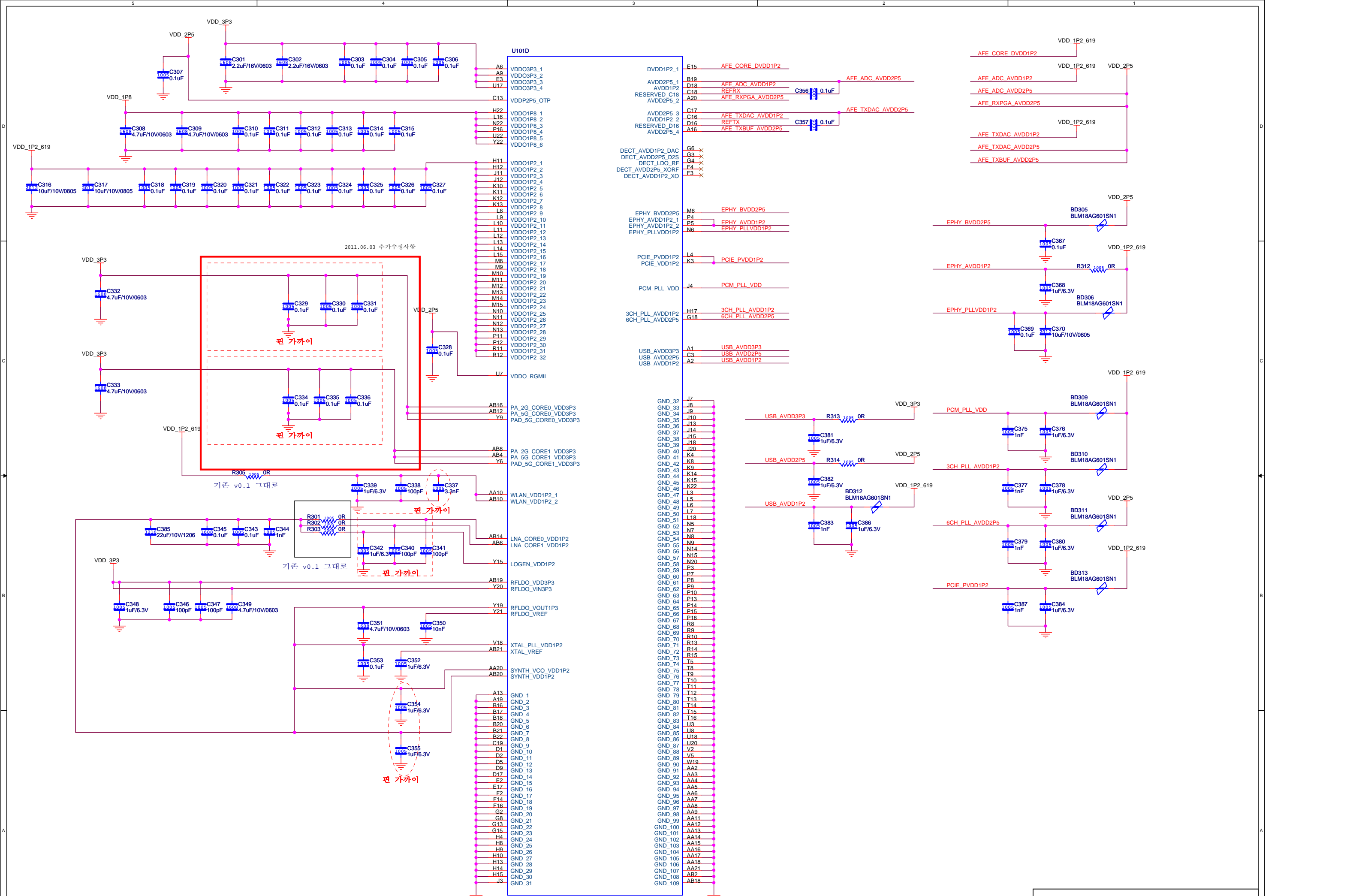
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Size A	Document Number <Doc>	Rev <RevCode>
Date:	Tuesday, October 11, 2011	Sheet 1 of 1



Title	<Title>	Rev	<Rev Code>
Size	Document Number		
C	<Doc>		
Date:	Tuesday, October 11, 2011	Sheet	1 of 1



Title		<Title>
Size	Document Number	Rev
A3	<Doc>	<RevC>
Date:	Tuesday, October 11, 2011	Sheet 1 of 1



2011.06.03 추가수정사항

변 가까이

변 가까이

변 가까이

기존 v0.1 그대로

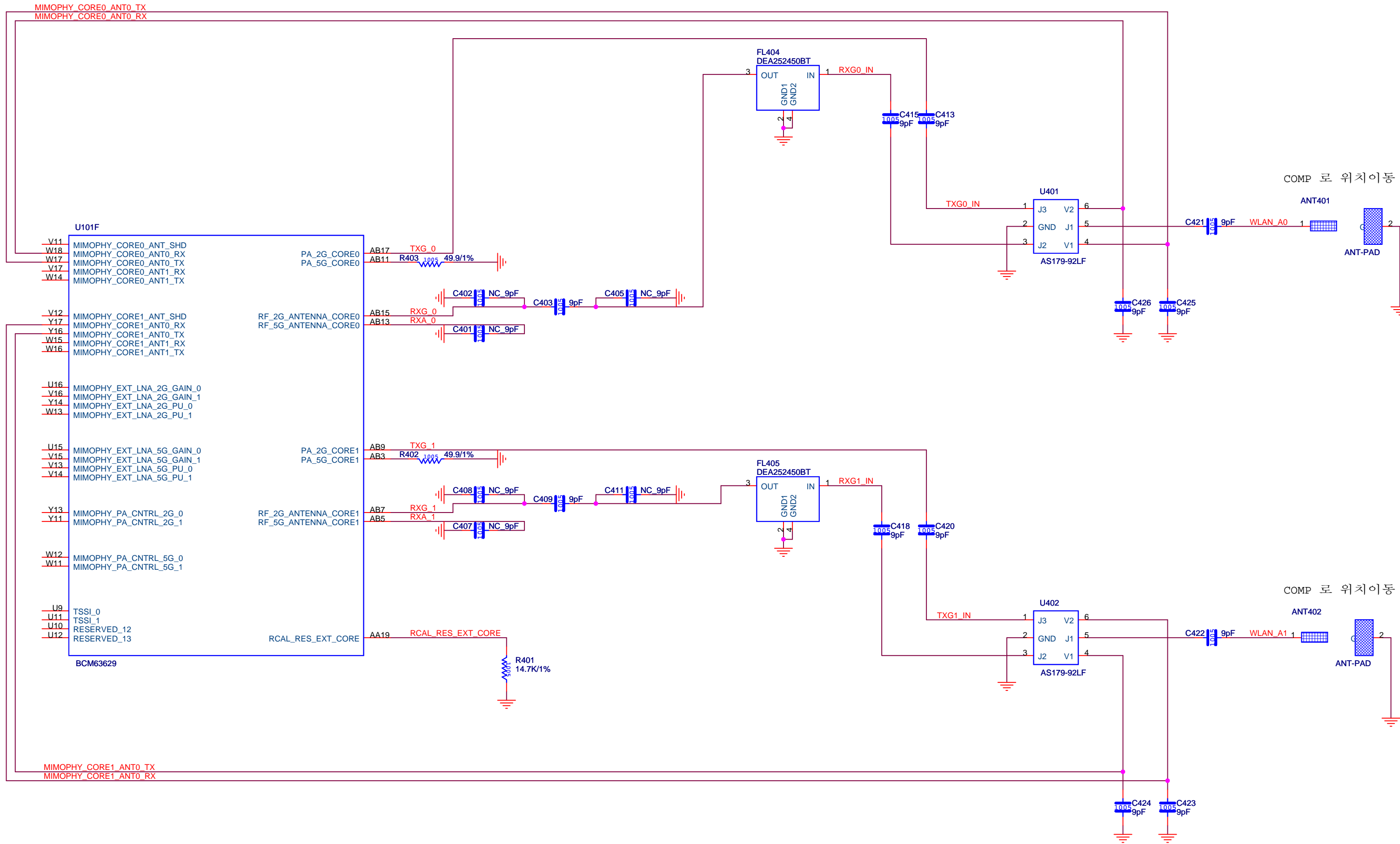
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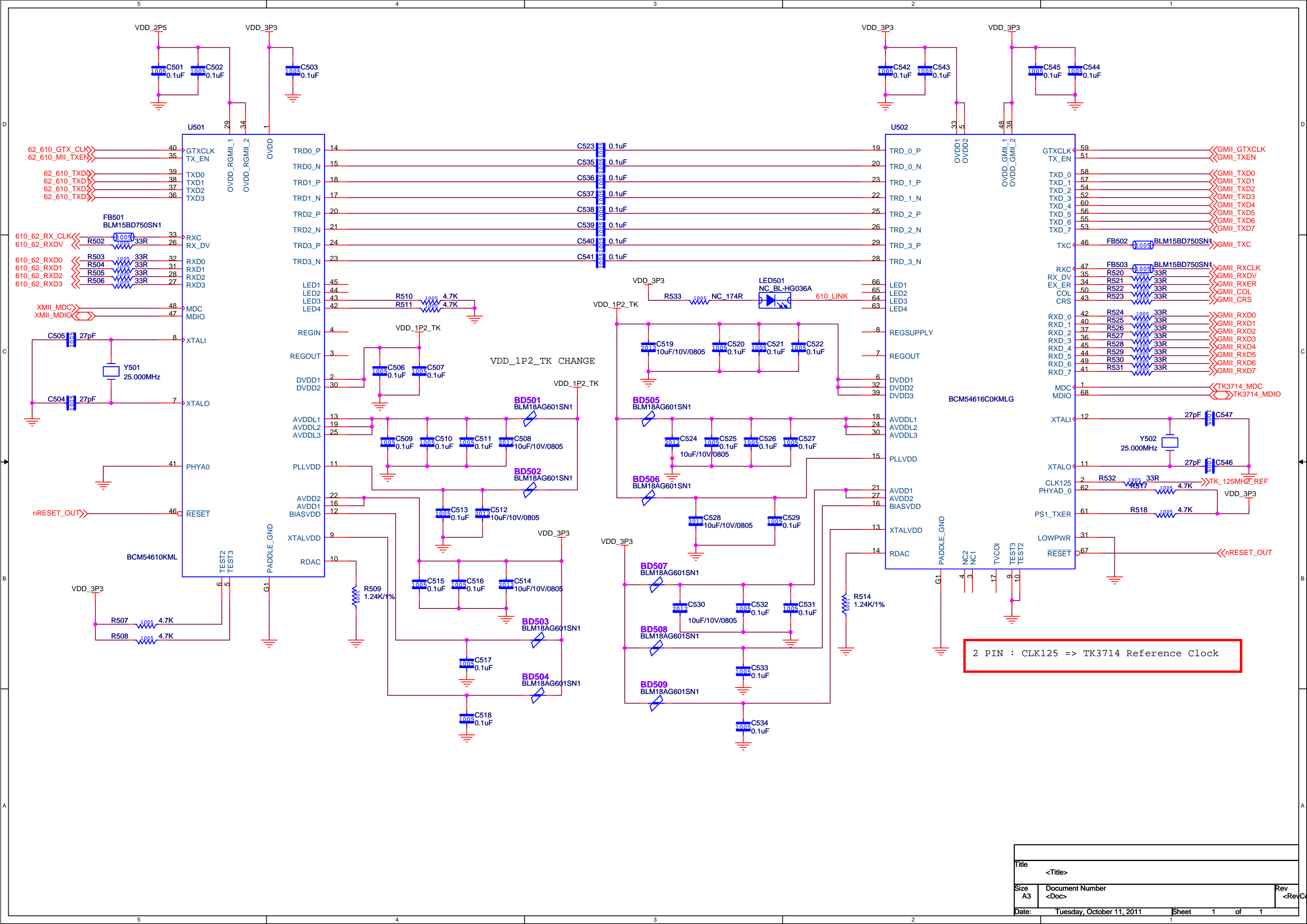
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U17	VDDO3P3_4
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H22	VDDO1P8_1
L16	VDDO1P8_2
N22	VDDO1P8_3
P16	VDDO1P8_4
U22	VDDO1P8_5
Y22	VDDO1P8_6
H11	VDDO1P2_1
H12	VDDO1P2_2
J11	VDDO1P2_3
J12	VDDO1P2_4
K10	VDDO1P2_5
K11	VDDO1P2_6
K12	VDDO1P2_7
K13	VDDO1P2_8
L8	VDDO1P2_9
L9	VDDO1P2_10
L10	VDDO1P2_11
L11	VDDO1P2_12
L12	VDDO1P2_13
L13	VDDO1P2_14
L14	VDDO1P2_15
L15	VDDO1P2_16
M8	VDDO1P2_17
M9	VDDO1P2_18
M10	VDDO1P2_19
M11	VDDO1P2_20
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M13	VDDO1P2_22
M14	VDDO1P2_23
M15	VDDO1P2_24
N10	VDDO1P2_25
N11	VDDO1P2_26
N12	VDDO1P2_27
N13	VDDO1P2_28
P11	VDDO1P2_29
P12	VDDO1P2_30
R11	VDDO1P2_31
R12	VDDO1P2_32
U7	VDDO_RGMII
AB16	PA_2G_CORE0_VDD3P3
AB12	PA_5G_CORE0_VDD3P3
Y9	PAD_5G_CORE0_VDD3P3
AB8	PA_2G_CORE1_VDD3P3
AB4	PA_5G_CORE1_VDD3P3
Y6	PAD_5G_CORE1_VDD3P3
AA10	WLAN_VDD1P2_1
AB10	WLAN_VDD1P2_2
AB14	LNA_CORE0_VDD1P2
AB6	LNA_CORE1_VDD1P2
Y15	LOGEN_VDD1P2
AB19	RFLDO_VDD3P3
Y20	RFLDO_VIN3P3
Y19	RFLDO_VOUT1P3
Y21	RFLDO_VREF
V18	XTAL_PLL_VDD1P2
AB21	XTAL_VREF
AA20	SYNTH_VCO_VDD1P2
AB20	SYNTH_VDD1P2
A13	GND_1
A19	GND_2
B16	GND_3
B17	GND_4
B18	GND_5
B20	GND_6
B21	GND_7
B22	GND_8
C19	GND_9
D1	GND_10
D2	GND_11
D5	GND_12
D9	GND_13
D17	GND_14
E2	GND_15
E17	GND_16
F2	GND_17
F14	GND_18
F16	GND_19
G2	GND_20
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G13	GND_22
G15	GND_23
H4	GND_24
H8	GND_25
H9	GND_26
H10	GND_27
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P10	GND_67
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P14	GND_69
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T13	GND_84
T14	GND_85
T15	GND_86
T16	GND_87
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U8	GND_89
U18	GND_90
U20	GND_91
V2	GND_92
V5	GND_93
W19	GND_94
AA2	GND_95
AA3	GND_96
AA4	GND_97
AA5	GND_98
AA6	GND_99
AA9	GND_100
AA11	GND_101
AA12	GND_102
AA13	GND_103
AA14	GND_104
AA15	GND_105
AA16	GND_106
AA17	GND_107
AA21	GND_108
AB2	GND_109
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Size	<Doc>
C	<Rev Code>
Date:	Tuesday, October 11, 2011
Sheet	1 of 1

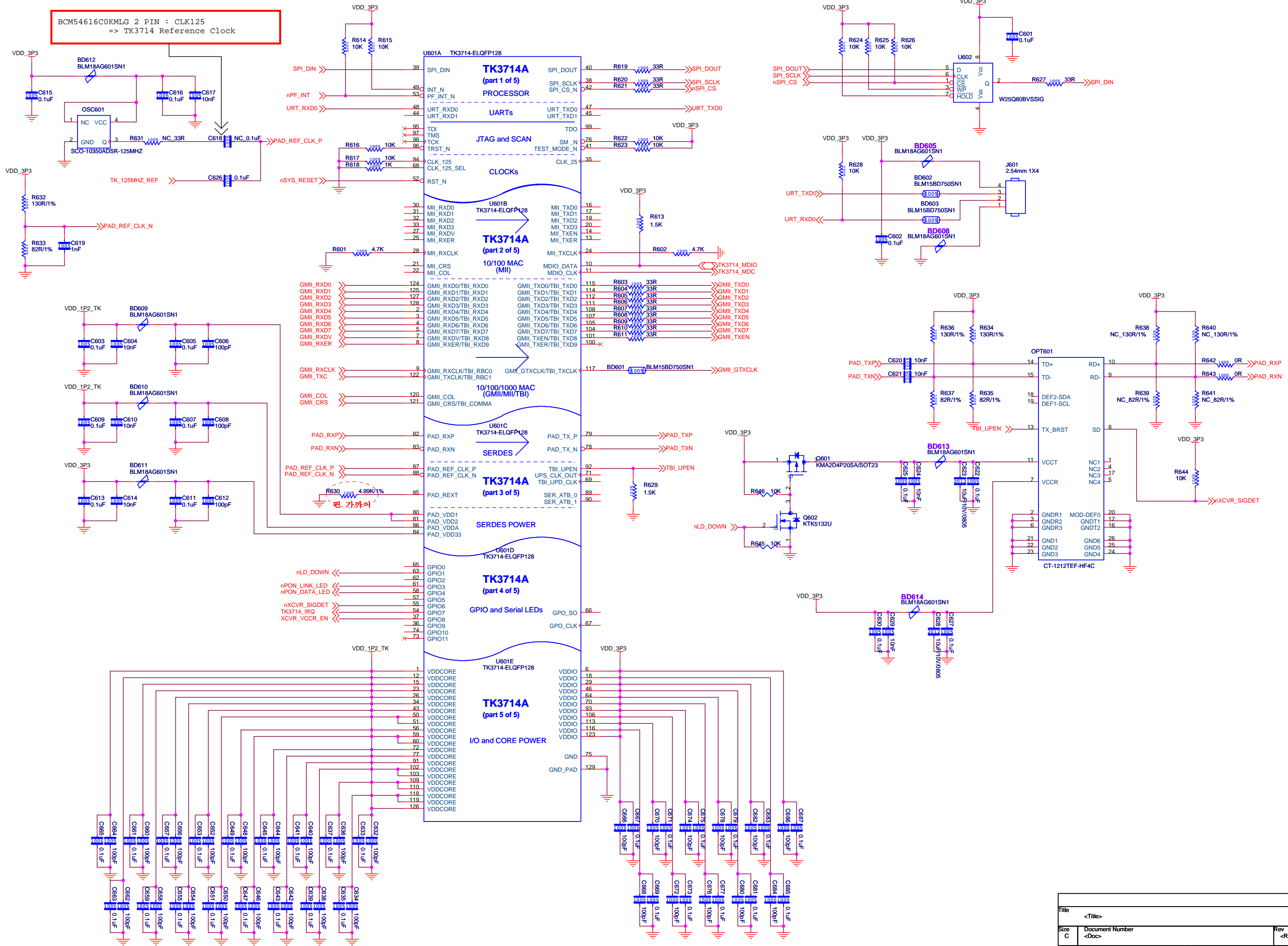


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Size A3	Document Number <Doc>	Rev <RevC>
Date: Tuesday, October 11, 2011	Sheet 1	of 1



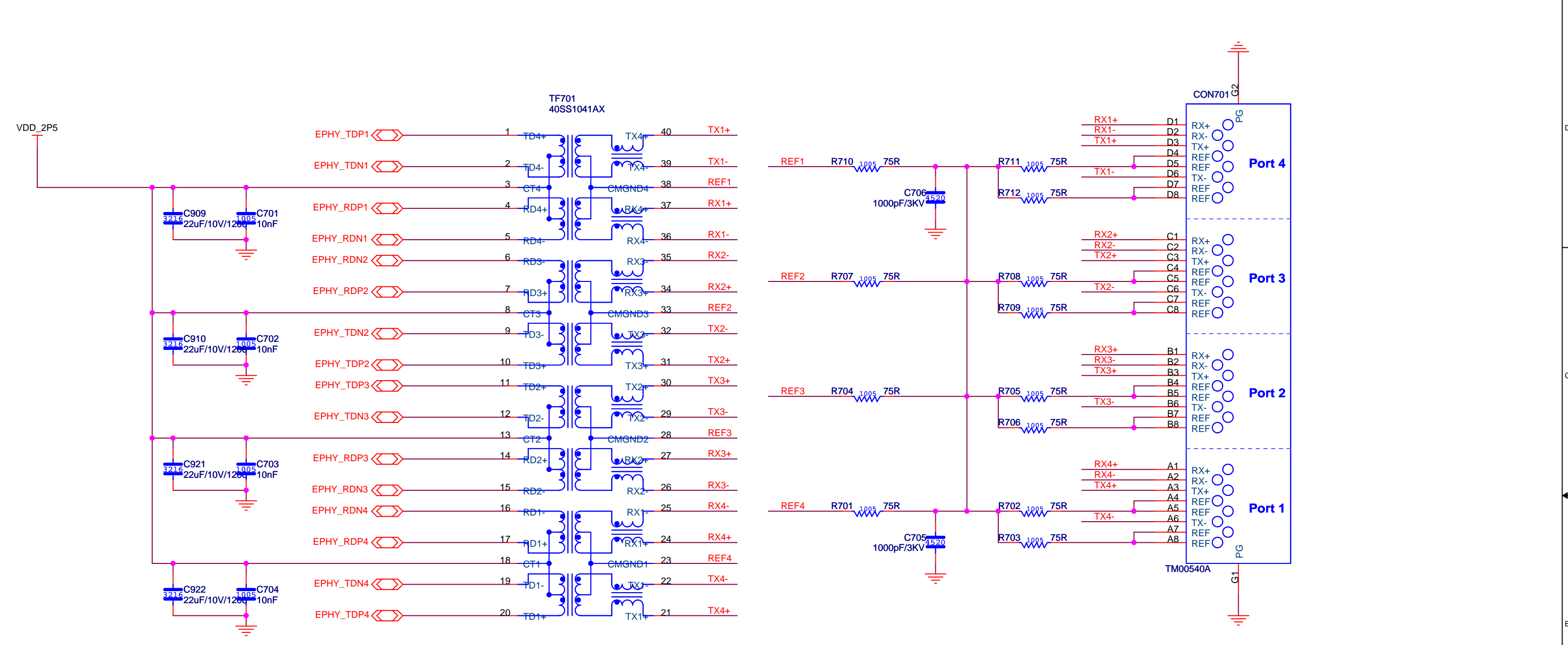
2 PIN : CLK125 => TK3714 Reference Clock

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Date:	Tuesday, October 11, 2011	Sheet	1 of 1

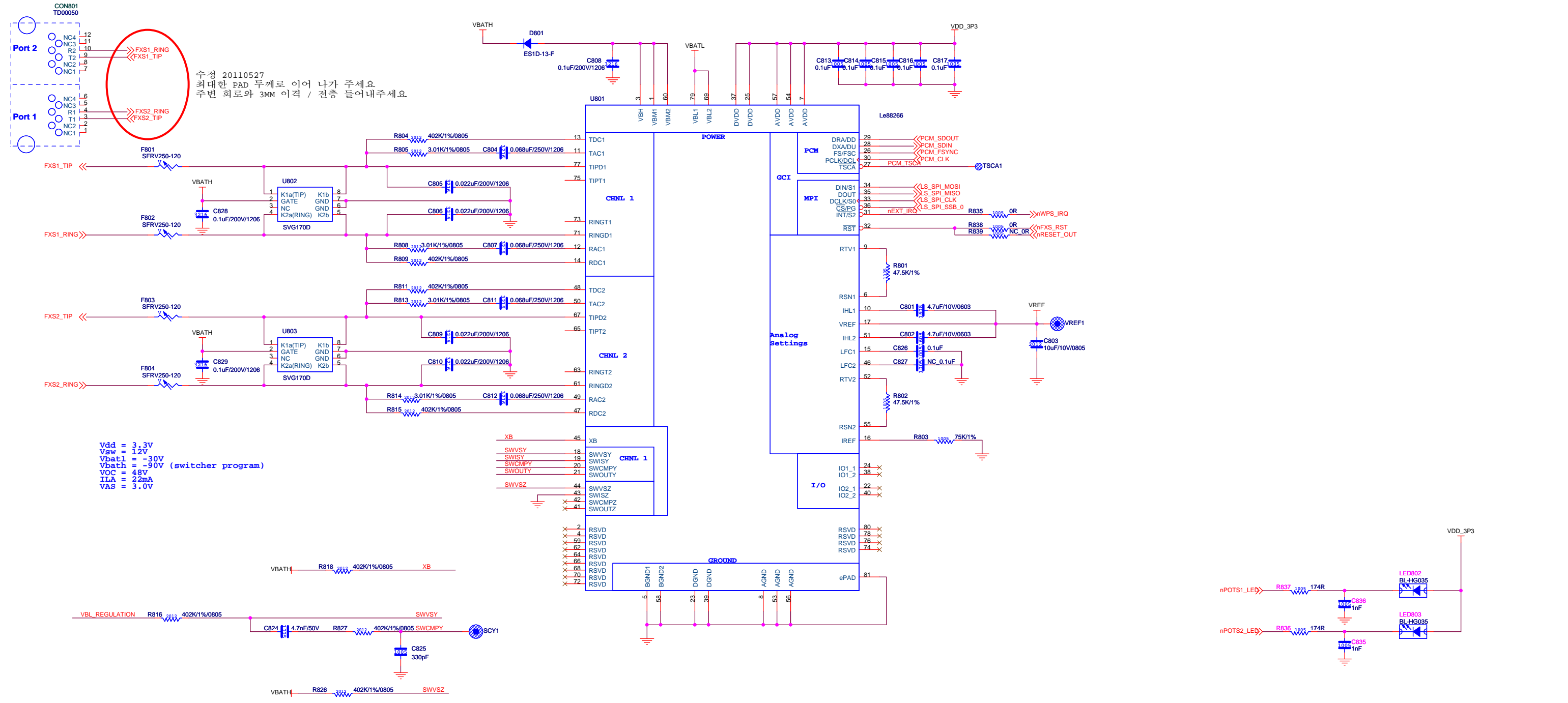


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Date:	Tuesday, October 11, 2011	Sheet 1 of 1

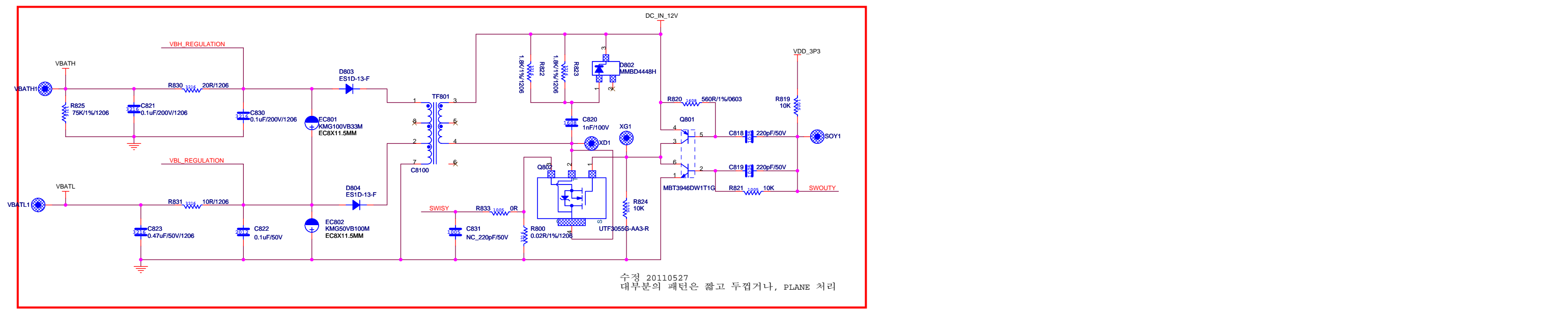




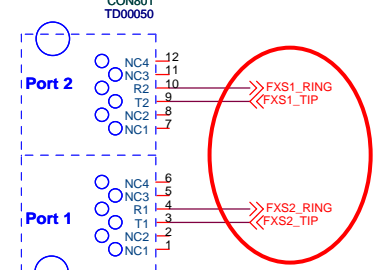
Title		
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Size	Document Number	Rev
B	<Doc>	<Rev Code>
Date:	Tuesday, October 11, 2011	Sheet 1 of 1



Vdd = 3.3V  
 Vsw = 1.2V  
 Vbat1 = -30V  
 VBath = -90V (switcher program)  
 VDC = 48V  
 ILA = 22mA  
 VAS = 3.0V



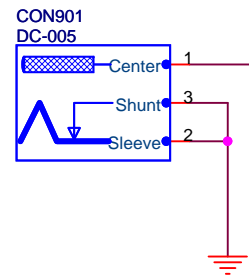
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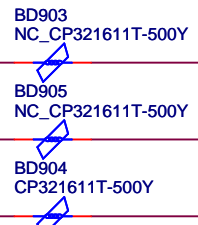
수정 20110527  
 최대한 PAD 두께로 이어 나가 주세요.  
 주변 회로와 3MM 이격 / 전층 들어내주세요.

Title		<Title>
Size	A2	Document Number <Doc>
Date:	Tuesday, October 11, 2011	Sheet 1 of 1

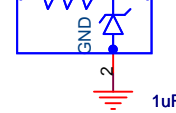
+12VDC IN



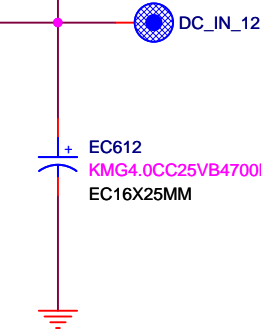
SW901 IWLS-102-A4



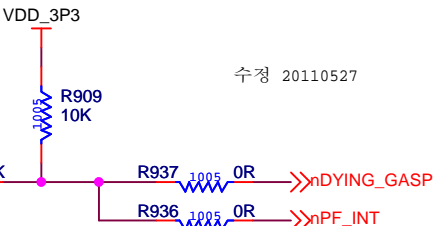
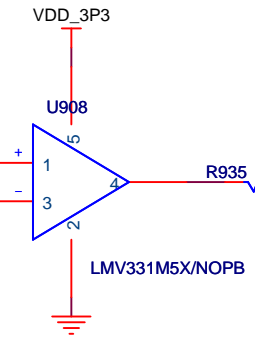
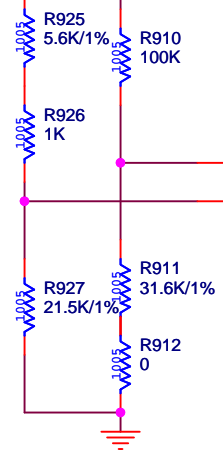
U904 ZEN132V230A16LS



DC\_IN\_12V



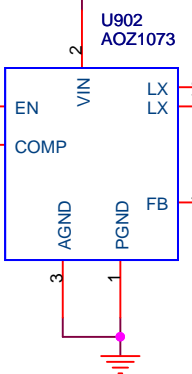
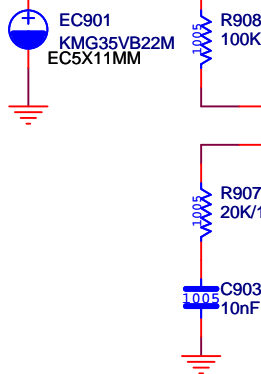
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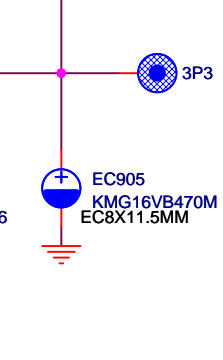
수정 20110527

[ POWER FAIL SIGNAL ]

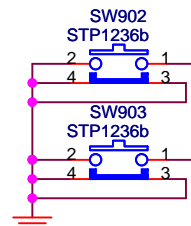
DC\_IN\_12V



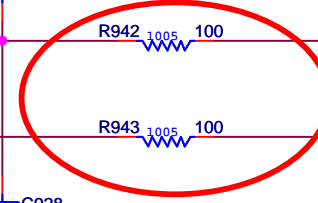
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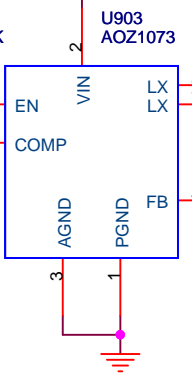
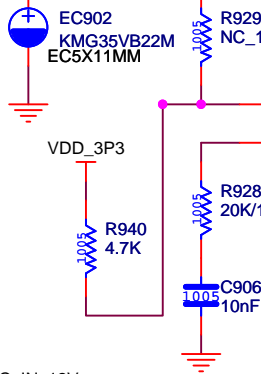
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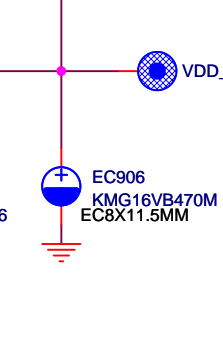
수정 20110530



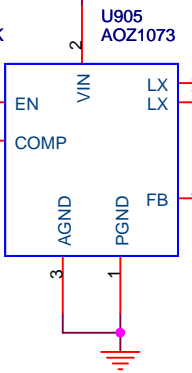
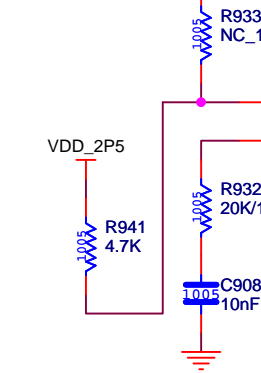
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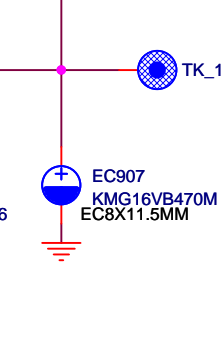
VDD\_2P5



DC\_IN\_12V

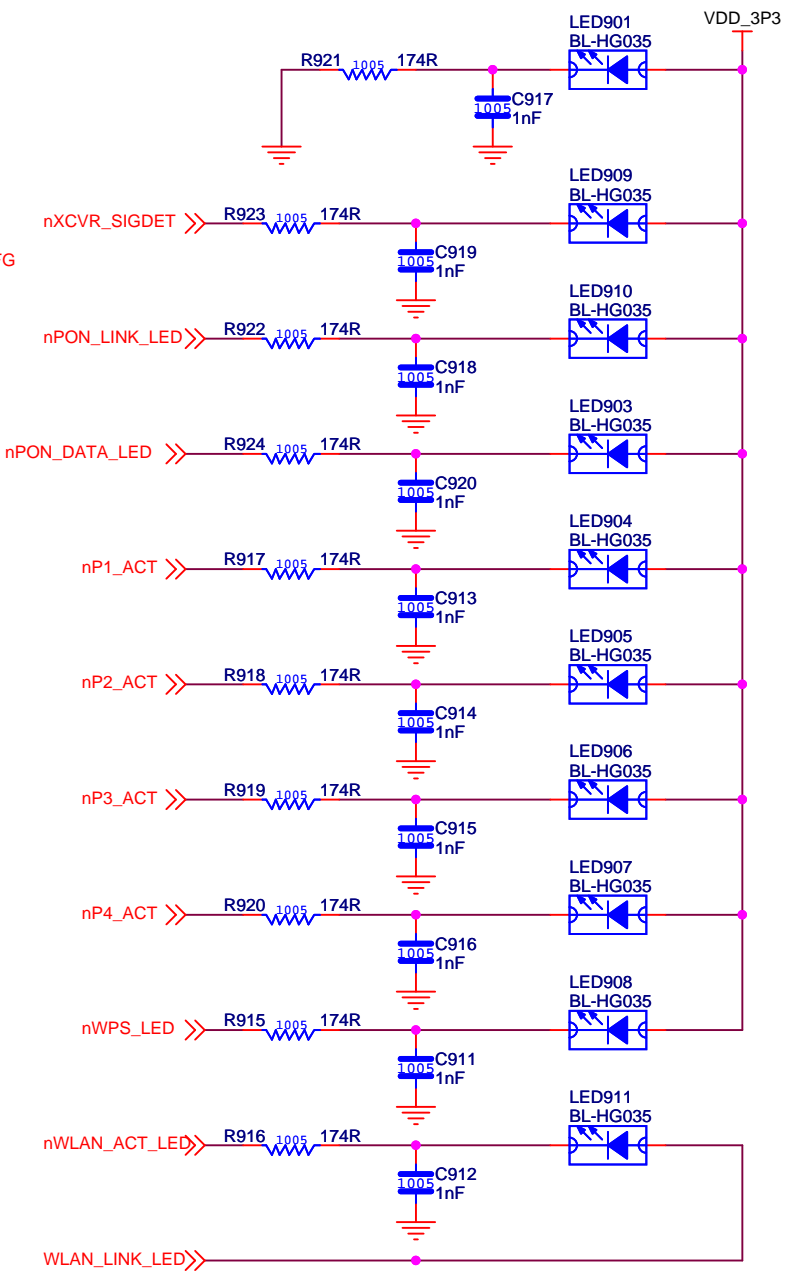


VDD\_1P2\_TK



C504W 소모 전류

- 5.0V: 1300mA, MAX 1500mA
  - 619\_3.3V: 760mA, MAX 1000mA
  - 619\_2.5V: 120mA, MAX 350mA
  - 3714\_3.3V: 360mA
  - 3714\_1.2V: 610mA
  - USB: 500mA
- \* 619\_2.5V: LAN 포트당 50mA  
\* BCM63629 Power sequency 확인



Title <Title>		
Size A3	Document Number <Doc>	Rev <RevC>
Date: Tuesday, October 11, 2011	Sheet 1 of 1	