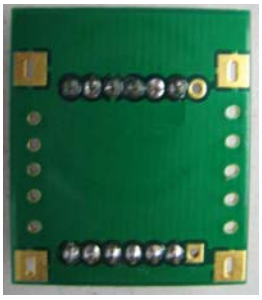
UNIVERSAL ISM BAND FSK TRANSCEIVER MODULE

VZ38915AZ

General Introduction



VZ38915AZ is a low costing ISM band transceiver module implemented with unique PLL. The SPI interface is used to communicate with microcontroller for parameter setting.

Features:

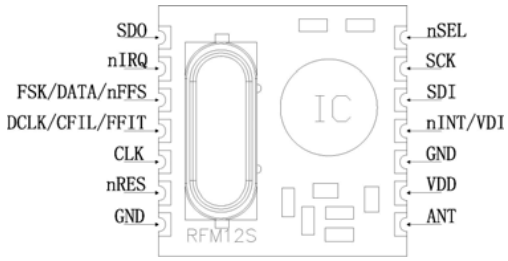
- Low costing, high performance and price ratio
- Tuning free during production
- PLL and zero IF technology
- Fast PLL lock time
- Automatic antenna tuning
- Analog and digital signal strength indicator (ARSSI/DRSSI)
- Automatic frequency control (AFC)
- Data quality detection (DQD)
- Internal data filtering and clock recovery
- RX synchron pattern recognition
- SPI compatible serial control interface
- Clock and reset signal output for external MCU use
- 16 bit RX Data FIFO
- Two 8 bit TX data registers
- Standard 10 MHz crystal reference
- Wakeup timer
- 3.3V power supply
- Low power consumption
- Standby current less than 0.3uA

“This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.”

“Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.”

Pin Definition：

SMD



definition	Type	Function
nINT/VDI	DI/ DO	Interrupt input (active low)/Valid data indicator
VDD	S	Positive power supply
SDI	DI	SPI data input
SCK	DI	SPI clock input
nSEL	DI	Chip select (active low)
SDO	DO	Serial data output with bus hold
nIRQ	DO	Interrupts request output（active low）
FSK/DATA/nFFS	DI/DO/DI	Transmit FSK data input/ Received data output (FIFO not used)/ FIFO select
DCLK/CFIL/FFIT	DO/AIO/DO	Clock output (no FIFO)/ external filter capacitor(analog mode)/ FIFO interrupts(active high)when FIFO level set to 1, FIFO empty interruption can be achieved
CLK	DO	Clock output for external microcontroller
nRES	DIO	Reset output（active low）
GND	S	Power ground

Electrical Parameter：

Maximum（not at working mode）

symbol	parameter	minimum	maximum	Unit
V_{dd}	Positive power supply	-0.5	6.0	V
V_{in}	All pin input level	-0.5	Vdd+0.5	V
Iin	Input current except power	-25	25	mA
ESD	Human body model		1000	V
Tst	Storage temperature	-55	125	℃
Tld	Soldering temperature(10s)		260	℃

Recommended working range

symbol	parameter	minimum	maximum	Unit
V_{dd}	Positive power supply	3.3*0.9	3.3*1.1	V
T_{op}	Working temperature	-40	85	℃

DC characteristic

symbol	parameter	Remark	minimum	typical	maximum	Unit
$I_{dd\_TX\_0}$	Supply current (TX mode, P_{out} = 0dBm)			17	19	mA
$I_{dd\_TX\_PMAX}$	Supply current (TX mode, P_{out} = P_{max})	915MHz band		24	26	mA
I_{dd_RX}	Supply current (RX mode)	915MHz band		13	15	mA
I_x	Idle current	Crystal oscillator on		0.62	1.2	mA
I_{pd}	Sleep mode current	All blocks off		0.3		uA
V_{il}	Low level input				0.3*V_{dd}	V
V_{ih}	High level input		0.7*V_{dd}			V
I_{il}	Leakage current	V_{il}=0V	-1		1	uA
I_{ih}	Leakage current	V_{ih}=V_{dd}, V_{dd}=5.4V	-1		1	uA
V_{ol}	Low level output	I_{ol}=2mA			0.4	V
V_{oh}	High level output	I_{oh}=-2mA	V_{dd}-0.4			V

AC characteristic

symbol	parameter	remark	min	typical	max	Unit
f_{ref}	PLL frequency		9	10	11	MHz
BW	Receiver bandwidth	mode 0 mode 1 mode 2 mode 3 mode 4 mode 5	60 120 180 240 300 360	67 134 200 270 350 400	75 150 225 300 375 450	KHz
t_{lock}	PLL lock time	After 10MHz step hopping, frequency error <10 kHz		30		us
tst, P	PLL startup time	With a running crystal oscillator		200	300	us
BR	Data rate	With internal digital demodulator	0.6		115.2	kbps
BR_A	Data rate	With external RC filter			256	kbps
P_{min}	sensitivity	BER 10^{-3}, BW=134KHz,BR=1.2kbps		-102	-96	dBm
AFC_{range}	AFC working range	df_{FSK} : FSK deviation in the received signal		0.8* df_{FSK}		
RS_A	RSSI accuracy			±5		dB
RS_R	RSSI range			46		dB
C_{ARSSI}	ARSSI filter			1		nF

RS_{STEP}	RSSI programmable step			6		dB
RS_{RESP}	DRSSI response time	RSSI output high after valid , CARRSI=5nF		500		us

AC characteristic(Transmitter)

symbol	parameter	remark	min	typical	max	Unit
P_{max_50}	Max. output power delivered to 50Ohm load over a suitable matching network	915MHZ band		5		dbm
P_{max_ant}	Max. EIRP with suitable selected PCB antenna.	915 MHz bands		7		dbm
P_{out}	Typical output power	Selectable in 3 dB steps	P_{max}-21		P_{max}	dbm
C_o	Output capacitance (set by the automatic antenna tuning circuit)	In low bands In high bands	2 2.1	2.6 2.7	3.2 3.3	pf
Q_o	Quality factor of the output capacitance	In low bands In high bands	13 8	15 10	17 12	
L_{out}	Output phase noise	100 kHz from carrier 1 MHz from carrier			-80 -103	dbc/HZ
BR_{TX}	FSK bit rate	Via internal TX data register			172	kbps
BRA_{TX}	FSK bit rate	TX data connected to the FSK input			256	kbps
df_{fsk}	FSK frequency deviation	Programmable in 15 kHz steps	15		240	kHZ

AC characteristic(Turn-on/Turnaround timings)

symbol	parameter	remark	min	typical	max	Unit
T_{st}	Crystal oscillator startup time	Crystal ESR < 100		1	5	ms
$T_{tx\_XTAL\_ON}$	Transmitter turn-on time	Synthesizer off, crystal oscillator on with 10 MHz step		250		us
$T_{rx\_XTAL\_ON}$	Receiver turn-on time	Synthesizer off, crystal oscillator on with 10 MHz step		250		us
$T_{tx\_rx\_SYNT\_ON}$	Transmitter – Receiver turnover time	Synthesizer and crystal oscillator on during TX/RX		150		us
$T_{rx\_tx\_SYNT\_ON}$	Receiver – Transmitter turnover time	Synthesizer and crystal oscillator on during RX/TX		150		us
C_{xl}	Crystal load capacitance	Programmable in 0.5 pF steps, tolerance+/- 10%	8.5		16	pf

t_{POR}	Internal POR timeout	After V_{dd} has reached 90% of final value			100	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.96		1.05	ms
$C_{in, D}$	Digital input apacitance				2	pf
$t_{r, f}$	Digital output rise/fall time	15pF pure capacitive load			10	ns

CONTROL INTERFACE

Commands to the transmitter are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on
pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-
bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control and command registers.

The receiver will generate an interrupt request (IT) for the microcontroller - by pulling the nIRQ pin low - on the following events:

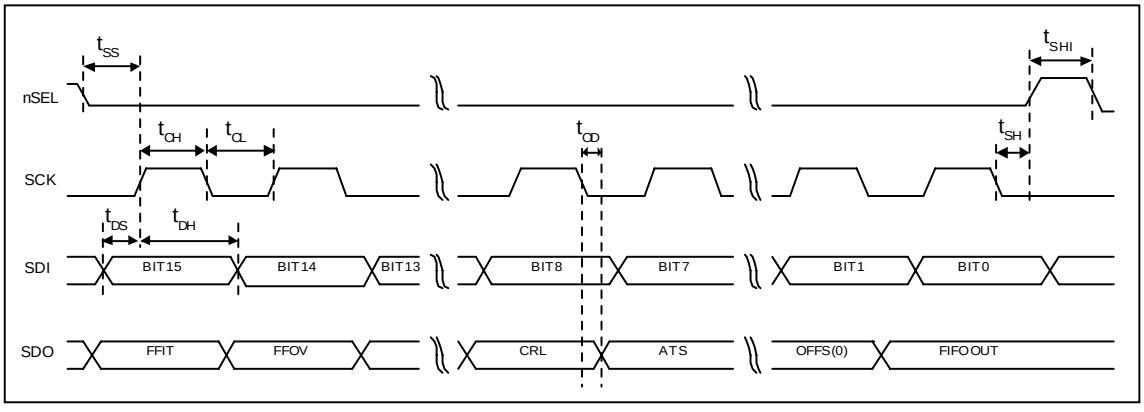
- The TX register is ready to receive the next byte (RGIT)
- The FIFO has received the preprogrammed amount of bits (FFIT)
- Power-on reset (POR)
- FIFO overflow (FFOV) / TX register underrun (RGUR)
- Wake-up timer timeout (WKUP)
- Negative pulse on the interrupt input pin nINT (EXT)
- Supply voltage below the preprogrammed value is detected (LBD)

FFIT and FFOV are applicable when the FIFO is enabled. RGIT and RGUR are applicable only when the TX register is enabled. To identify the source of the IT, the status bits should be read out.

Timing Specification

Symbol	Parameter	Minimum value [ns]
t_C	Clock high time	25
t_C	Clock low time	25
t_S	Select setup time (nSEL falling edge to SCK rising edge)	10
t_S	Select hold time (SCK falling edge to nSEL rising edge)	10
t_S	Select high time	25
t_D	Data setup time (SDI transition to SCK rising edge)	5
t_D	Data hold time (SCK rising edge to SDI transition)	5
t_O	Data delay time	10

Timing Diagram



Control Commands

	Control Command	Related Parameters/Functions	Related control bits
1	Configuration Setting Command	Frequency band, crystal oscillator load capacitance, RX FIFO and TX register enable	el, ef, b1 to b0, x3 to x0
2	Power Management Command	Receiver/Transmitter mode change, synthesizer, crystal oscillator, PA, wake-up timer, clock output enable	er, ebb, et, es, ex, eb, ew, dc
3	Frequency Setting Command	Frequency of the local oscillator/carrier signal	f11 to f0
4	Data Rate Command	Bit rate	cs, r6 to r0
5	Receiver Control Command	Function of pin 16, Valid Data Indicator, baseband bandwidth, LNA gain, digital RSSI	p16, d1 to d0, i2 to i0, g1 to g0, r2
6	Data Filter Command	Data filter type, clock recovery parameters	al, ml, s, f2 to f0
7	FIFO and Reset Mode Command	Data FIFO IT level, FIFO start control, FIFO enable and FIFO fill enable, POR sensitivity	f3 to f0, sp, ff, al, dr
8	Synchron Pattern Command	Synchron pattern	b7 to b0
9	Receiver FIFO Read Command	RX FIFO read	
10	AFC Command	AFC parameters	a1 to a0, rl1 to rl0, st, fi, oe, en
11	TX Configuration Control Command	Modulation parameters, output power	mp, m3 to m0, p2 to p0
12	PLL Setting Command	CLK out buffer speed, low power mode of the crystal oscillator, dithering, PLL bandwidth	ob1 to ob0, ddit, ddy, bw0
13	Transmitter Register Write	TX data register write	t7 to t0
14	Wake-Up Timer Command	Wake-up time period	r4 to r0, m7 to m0
15	Low Duty-Cycle Command	Enable and set low duty-cycle mode	d6 to d0, en
16	Low Battery Detector and Microcontroller Clock Divider Command	LBD voltage and microcontroller clock division ratio	d2 to d0, v3 to v0
17	Status Read Command	Status bit readout	

In general, setting the given bit to one will activate the related function. In the following tables, the POR column shows the default
values of the command registers after power-on.

Description of the Control Commands

1. Configuration Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	0	0	el	ef	b1	b0	x3	x2	x1	x0	8008h

Bit *el* enables the internal data register.
Bit *ef* enables the FIFO mode. If *ef*=0 then DATA (pin 6) and DCLK (pin 7) are used for data and data clock output.

b1	b0	Frequency Band [MHz]
0	0	Reserved
0	1	433
1	0	868
1	1	915

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
…				
1	1	1	0	15.5
1	1	1	1	16.0

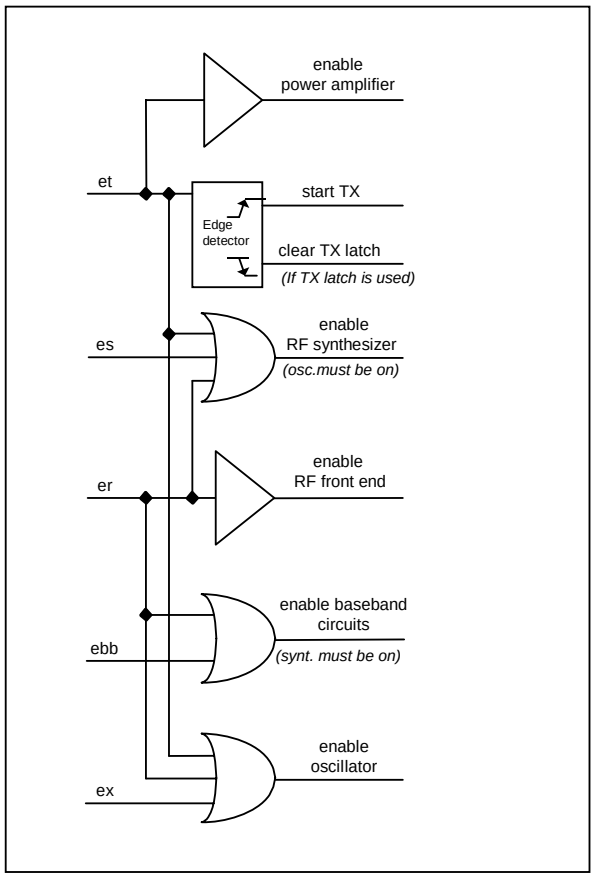
2. Power Management Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	1	0	er	ebb	et	es	ex	eb	ew	dc	8208h

Bit	Function of the control bit	Related blocks
er	Enables the whole receiver chain	RF front end, baseband, synthesizer, oscillator
ebb	The receiver baseband circuit can be separately switched	Baseband
et	Switches on the PLL, the power amplifier, and starts the transmission (If TX register is enabled)	Power amplifier, synthesizer, oscillator
es	Turns on the synthesizer	Synthesizer
ex	Turns on the crystal oscillator	Crystal oscillator
eb	Enables the low battery detector	Low battery detector
ew	Enables the wake-up timer	Wake-up timer
dc	Disables the clock output (pin 8)	Clock output buffer

The ebb, es, and ex bits are provided to optimize the TX to RX or RX to TX turnaround time.

Logic connections between power control bits:



Note:

If both *et* and *er* bits are set the chip goes to receive mode.

FSK / nFFSEL input are equipped with internal pull-up resistor. To achieve minimum current consumption do not pull this input to logic low in sleep mode.

3. Frequency Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A680h

The 12-bit parameter F (bits *f11* to *f0*) should be in the range of 96 and 3903. When F value sent is out of range, the previous value is kept. The synthesizer center frequency f_0 can be calculated as:

$f_0 = 10 * C1 * (C2 + F/4000)$ [MHz]

The constants C1 and C2 are determined by the selected band as:

Band [MHz]	C1	C2
433	1	43
868	2	43
915	3	30

4. Data Rate Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	cs	r6	r5	r4	r3	r2	r1	r0	C623h

The actual bit rate in transmit mode and the expected bit rate of the received data stream in receive mode is determined by the 7-bit parameter R (bits *r6* to *r0*) and bit *cs*.

BR = 10000 / 29 / (R+1) / (1+*cs**7) [kbps]

In the receiver set R according to the next function:

R= (10000 / 29 / (1+*cs**7) / BR) – 1, where BR is the expected bit rate in kbps.

5. Receiver Control Command

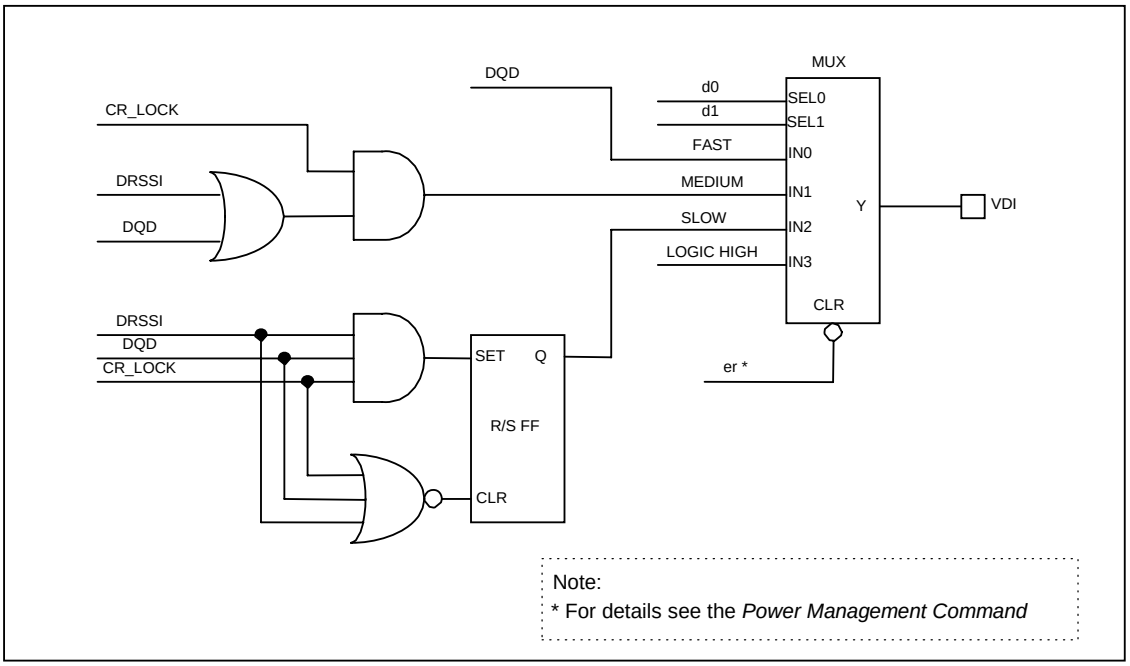
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	0	p16	d1	d0	i2	i1	i0	g1	g0	r2	r1	r0	9080h

Bit 10 *(p16)*: pin16 function select

p16	Function of pin 16
0	Interrupt
1	VDI

Bits 9-8 *(d1 to d0)*: VDI (valid data indicator) signal response time setting:

d1	d0	Response
0	0	Fas
0	1	Medium
1	0	Slo
1	1	Always on



Bits 7-5 *(i2 to i0)*: Receiver baseband bandwidth (BW) select:

i2	i1	i0	BW [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	67
1	1	1	reserved

Bits 4-3 *(g1 to g0)*: LNA gain select:

g1	g0	relative to maximum [dB]
0	0	0
0	1	-6
1	0	-14
1	1	-20

Bits 2-0 *(r2 to r0)*: RSSI detector threshold:

r2	r1	r0	$RSSI_{setth}$ [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85
1	0	0	-79
1	0	1	-73
1	1	0	Reserved
1	1	1	Reserved

The RSSI threshold depends on the LNA gain, the real RSSI threshold can be calculated:

$$RSSI_{th}=RSSI_{setth}+G_{LNA}$$

6. Data Filter Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	al	ml	1	s	1	f2	f1	f0	C22Ch

Bit 7 (*al*): Clock recovery (CR) auto lock control, if set.

CR will start in fast mode, then after locking it will automatically switch to slow

mode. Bit 6 (*ml*): Clock recovery lock control

1: fast mode, fast attack and fast release (4 to 8 bit preamble (1010...) is recommended)

0: slow mode, slow attack and slow release (12 to 16 bit preamble is

recommended) Using the slow mode requires more accurate bit timing (see *Data*

Rate Command).

Bits 4 (*s*): Select the type of the data filter:

s	Filter Type
0	Digital filter
1	Analog RC filter

Digital: This is a digital realization of an analog RC filter followed by a comparator with hysteresis. The time constant is
automatically adjusted to the bit rate defined by the *Data Rate*

Command. Note: Bit rate can not exceed 115 kpbs in this mode.

Analog RC filter: The demodulator output is fed to pin 7 over a 10 kOhm resistor. The filter cut-off frequency is set by the external capacitor connected to this pin and VSS.

The table shows the optimal filter capacitor values for different data rates

1.2 kbps	2.4 kbps	4.8 kbps	9.6 kbps	19.2 kbps	38.4 kbps	57.6 kbps	115.2 kbps	256 kbps
12 nF	8.2 nF	6.8 nF	3.3 nF	1.5 nF	680 pF	270 pF	150 pF	100 pF

Note: If analog RC filter is selected the internal clock recovery circuit and the FIFO can not be

used. Bits 2-0 (*f2* to *f0*): DQD threshold parameter.

Note: To let the DQD report "good signal quality" the threshold parameter should be 4 in cases where the bitrate is close to the deviation. At higher deviation/bitrate settings, a higher threshold parameter can report "good signal quality" as well.

7. FIFO and Reset Mode Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	1	0	f3	f2	f1	f0	sp	al	ff	dr	CA80h

Bits 7-4 (*f3* to *f0*): FIFO IT level. The FIFO generates IT when the number of received data bits reaches this level.

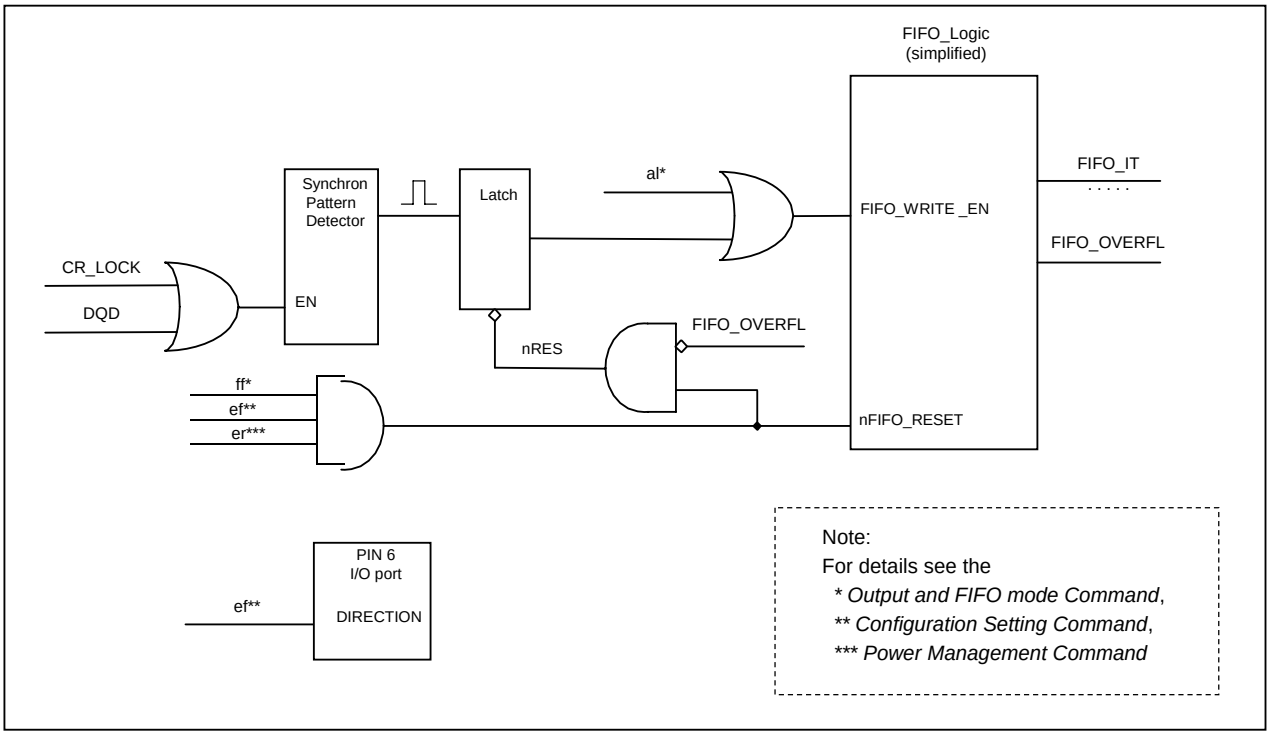
Bit 3 (*sp*): Select the length of the synchron pattern:

sp	Byte1	Byte0 (POR)	Synchron Pattern (Byte1+Byte0)
0	2Dh	D4h	2DD4h
1	Not used	D4h	D4h

Note: Byte0 can be programmed by the *Synchron Pattern Command*.

Bit 2 (*al*): Set the input of the FIFO fill start condition:

al	
0	Synchron pattern
1	Always fill



Bit 1 (*ff*): FIFO fill will be enabled after synchron pattern reception. The FIFO fill stops when this bit is cleared.

Bit 0 (*dr*): Disables the highly sensitive RESET mode.

Reset mode	Reset triggered when
Sensitive reset dr=0	Vdd below 1.5V Vdd glitch greater than 500mV
Non-sensitive reset dr=1	Vdd below 0.25V

Note: To restart the synchron pattern recognition, bit 1 should be cleared and set.

8. Synchron Pattern Command

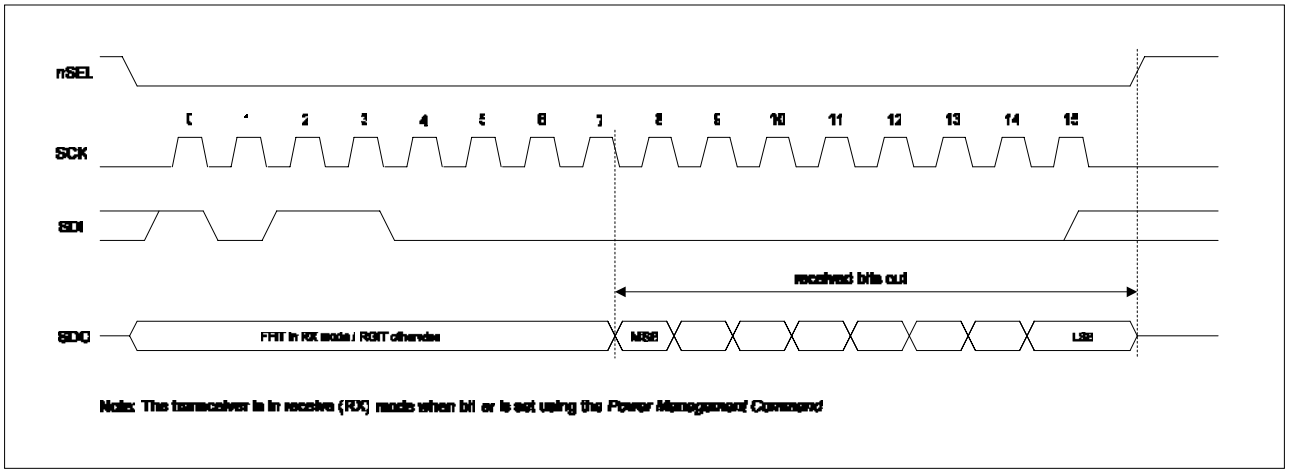
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	b7	b6	b5	b4	b3	b2	b1	b0	CED4h

The Byte0 used for synchron pattern detection can be reprogrammed by B <b7:b0>.

9. Receiver FIFO Read Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	B000h

With this command, the controller can read 8 bits from the receiver FIFO. Bit 6 *(ef)* must be set in *Configuration Setting Command.*



Note:: During FIFO access f_{SCK} cannot be higher than $f_{ref}/4$, where f_{ref} is the crystal oscillator frequency. When the duty-cycle of the clock signal is not 50 % the shorter period of the clock pulse width should be at least $2/f_{ref}$.

10. AFC Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	a1	a0	rl1	rl0	st	fi	oe	en	C4F7h

Bit 7-6 (*a1 to a0*): Automatic operation mode selector:

a1	**a0**	
0	0	Auto mode off (Strobe is controlled by microcontroller)
0	1	Runs only once after each power-up
1	0	Keep the f_{offset} only during receiving (VDI=high)
1	1	Keep the f_{offset} value independently from the state of the VDI signal

Bit 5-4 *(rl1 to rl0)*: Range limit. Limits the value of the frequency offset register to the next values:

rl1	**rl0**	**Max deviation**
0	0	No restriction
0	1	+15 f_{res} to -16 f_{res}
1	0	+7 f_{res} to -8 f_{res}
1	1	+3 f_{res} to -4 f_{res}

f_{res}:
433 MHz bands: 2.5 kHz
868 MHz band: 5 kHz
915 MHz band: 7.5 kHz

Bit 3 *(st)*: Strobe edge, when *st* goes to high, the actual latest calculated frequency error is stored into the offset register of the AFC block.

Bit 2 (*fi*): Switches the circuit to high accuracy (fine) mode. In this case, the processing time is about twice as long, but the measurement uncertainty is about half.

Bit 1 (*oe*): Enables the frequency offset register. It allows the addition of the offset register to the frequency control word of the PLL.

Bit 0 (*en*): Enables the calculation of the offset frequency by the AFC circuit.

There are three operation modes, examples from the possible application:

1, (*a1*=0, *a0*=1) The circuit measures the frequency offset only once after power up. This way, extended TX-RX maximum distance can be achieved.

Possible application:

In the final application, when the user inserts the battery, the circuit measures and compensates for the frequency offset caused by the crystal tolerances. This method allows for the use of a cheaper quartz in the application and provides protection against tracking
an interferer.

2a, (*a1*=1, *a0*=0) The circuit automatically measures the frequency offset during an initial effective low data rate pattern – easier to receive- (i.e.: 00110011) of the package and changes the receiving frequency accordingly. The further part of the package can be received by the corrected frequency settings.

2b, (*a1*=1, *a0*=0) The transmitter must transmit the first part of the packet with a step higher deviation and later there is a possibility
of reducing it.

In both cases (2a and 2b), when the VDI indicates poor receiving conditions (VDI goes low), the output register is automatically cleared. Use these settings when receiving signals from different transmitters transmitting in the same nominal frequencies.

3, (*a1*=1, *a0*=1) It's the same as 2a and 2b modes, but suggested to use when a receiver operates with only one transmitter. After a complete measuring cycle, the measured value is kept independently of the state of the VDI signal.

11. TX Configuration Control Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	1	0	0	mp	m3	m2	m1	m0	0	p2	p1	p0	9800h

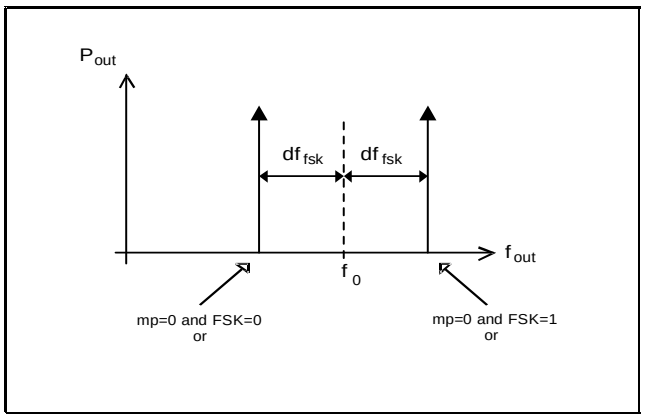
Bits 8-4 *(mp, m3 to m0)*: FSK modulation parameters:

The resulting output frequency can be calculated as:

$$f_{out} = f_0 + (-1)^{SIGN} * (M + 1) * (15\ kHz)$$

where:

f_0 is the channel center frequency (see the *Frequency Setting Command*)
M is the four bit binary number <*m3 : m0*>
SIGN = (*mp*) XOR FSK



Bits 2-0 *(p2 to p0)*: Output power:

p2	p1	p0	Relative Output Power [dB]
0	0	0	0
0	0	1	-2.5
0	1	0	-5
0	1	1	-7.5
1	0	0	-10
1	0	1	-12.5
1	1	0	-15
1	1	1	-17.5

mp=1 and FSK=1 mp=1 and FSK=0

Note:

FSK represents the value of the actual data bit.

The output power given in the table is relative to the maximum available power, which depends on the actual antenna impedance. (See: Antenna Application Note: IA ISM-AN1)

12. PLL Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	0	ob1	ob0	1	ddy	ddit	1	bw0	CC67h

Note: POR default setting of the register carefully selected to cover almost all typical applications.

Bit 6-5 (ob1-ob0): Microcontroller output clock buffer rise and fall time control.

ob1	ob0	Selected uC CLK frequency
0	0	5 or 10 MHz (recommended)
0	1	3.3 MHz
1	X	2.5 MHz or less

Bit 3 (ddy): Switches on the delay in the phase detector when this bit is set.

Bit 2 (*ddit*): When set, disables the dithering in the PLL loop.

Bit 0 (*bw0*): PLL bandwidth can be set for optimal TX RF performance.

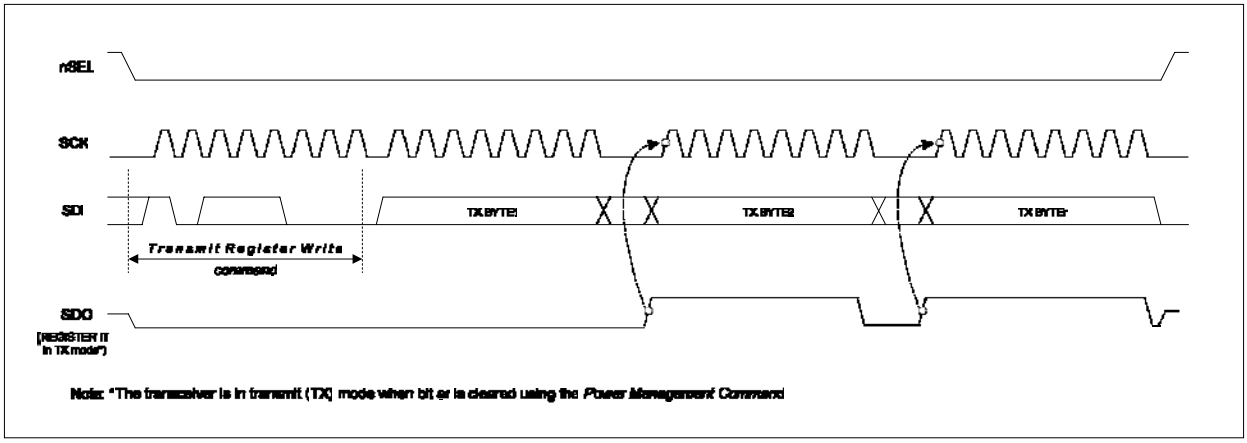
bw0	Max bit rate [kbps]	Phase noise at 1MHz offset [dBc/Hz]
0	86.2	-107
1	256	-102

13. Transmitter Register Write Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	1	0	0	0	t7	t6	t5	t4	t3	t2	t1	t0	B8AAh

With this command, the controller can write 8 bits *(t7 to t0)* to the transmitter data register. Bit 7 *(el)* must be set in *Configuration*
Setting Command.

Multiple Byte Write with Transmit Register Write Command:



Note: Alternately the transmit register can be directly accessed by nFFSEL (pin6).

14. Wake-Up Timer Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up time period can be calculated by (*m7 to m0*) and (*r4 to r0*):

$T_{wake\text{-}up} = 1.03 * M * 2^R + 0.5$ [ms]

Note:

For continual operation the *ew* bit should be cleared and set at the end of every cycle.

For future compatibility, use R in a range of 0 and 29.

15. Low Duty-Cycle Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	d6	d5	d4	d3	d2	d1	d0	en	C80Eh

With this command, Low Duty-Cycle operation can be set in order to decrease the average power consumption in receiver mode.

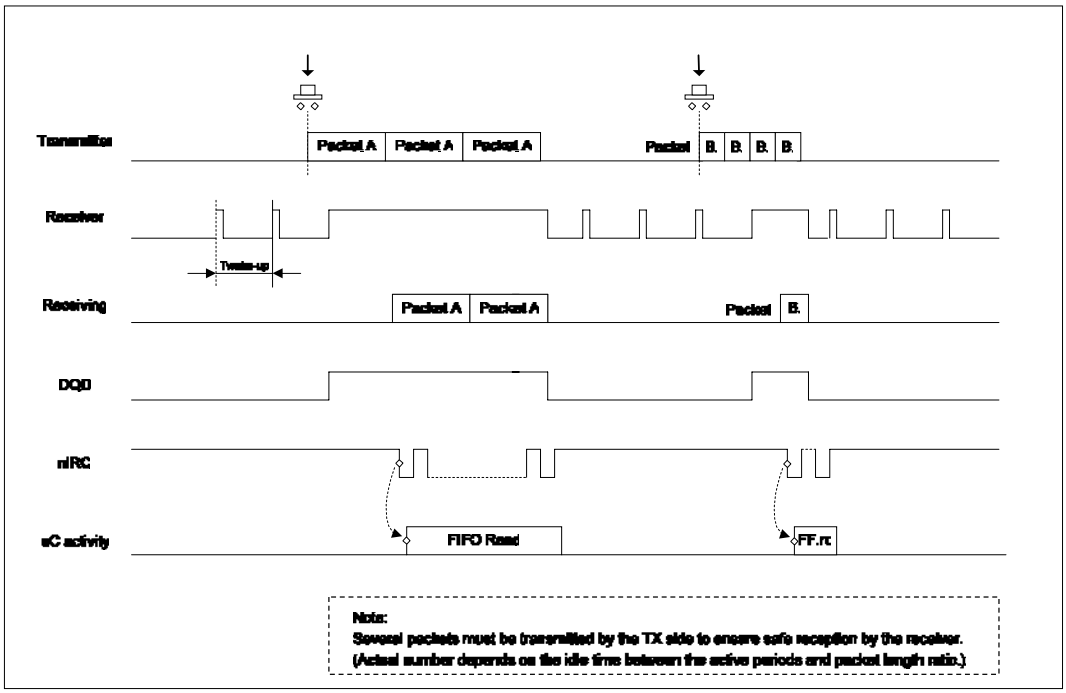
The time cycle is determined by the *Wake-Up Timer Command*.

The Duty-Cycle can be calculated by using (*d6* to *d0*) and M. (M is parameter in a *Wake-Up Timer*

Command.) Duty-Cycle= (D * 2 +1) / M *100%

The on-cycle is automatically extended while DQD indicates good received signal condition (FSK transmission is detected in the frequency range determined by *Frequency Setting Command* plus and minus the baseband filter bandwidth determined by the *Receiver Control Command*).

Application Proposal For LPDM (Low Power Duty-Cycle Mode) Receivers:



Bit 0 *(en)*: Enables the Low Duty-Cycle Mode. Wake-up timer interrupt is not generated in this mode.

Note: In this operation mode, bit *er* must be cleared and bit *ew* must be set in the *Power Management Command.*

16. Low Battery Detector and Microcontroller Clock Divider Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d2	d1	d0	0	v3	v2	v1	v0	C000h

The 4 bit parameter *(v3 to v0)* represents the value V, which defines the threshold voltage V$_{lb}$ of the detector:

V_{lb} = 2.25 + V * 0.1 [V]

Clock divider configuration:

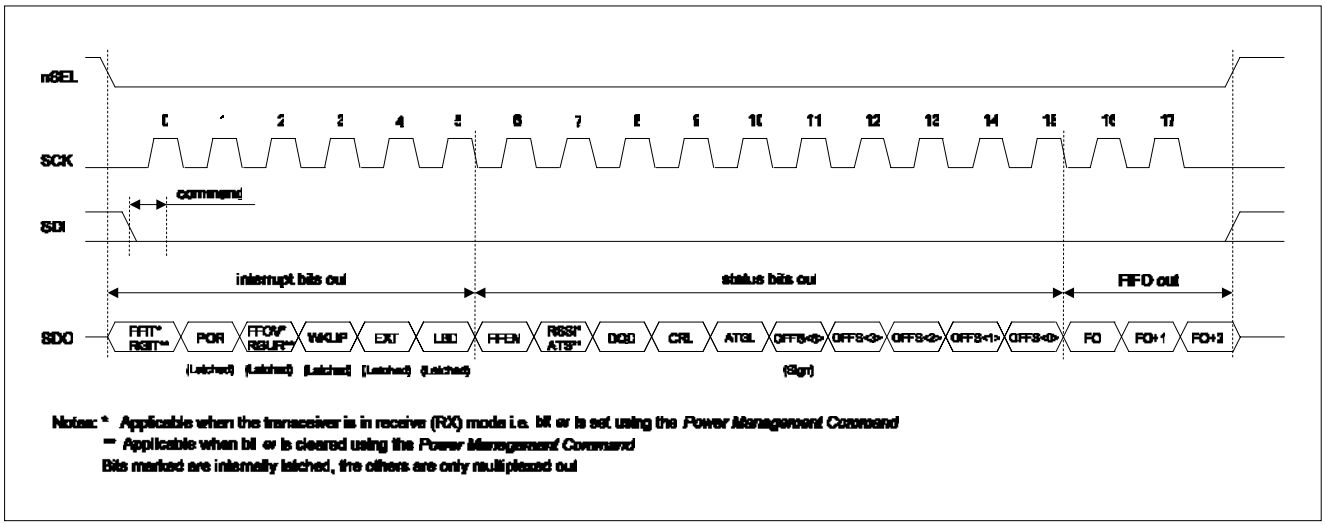
d2	**d1**	**d0**	**Clock Output Frequency [MHz]**
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

The low battery detector and the clock output can be enabled or disabled by bits *eb* and *dc,* respectively, using the *Power Management Command.*

17. Status Read Command

The read command starts with a zero, whereas all other control commands start with a one. If a read command is identified, the status bits will be clocked out on the SDO pin as follows:

Status Register Read Sequence with FIFO Read Example:



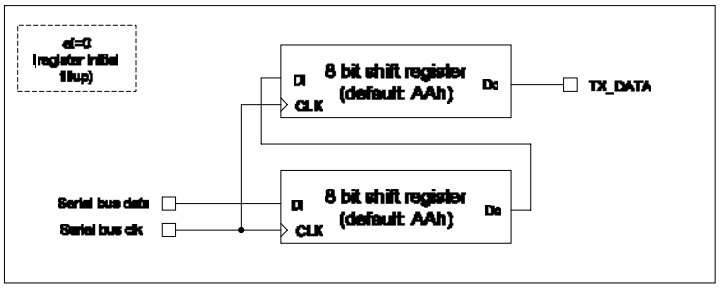
RGIT	TX register is ready to receive the next byte (Can be cleared by *Transmitter Register Write Command*)
FFIT	The number of data bits in the RX FIFO has reached the pre-programmed limit (Can be cleared by any of the FIFO read methods)
POR	Power-on reset (Cleared after *Status Read Command*)
RGUR	TX register under run, register over write (Cleared after *Status Read Command*)
FFOV	RX FIFO overflow (Cleared after *Status Read Command*)
WKUP	Wake-up timer overflow (Cleared after *Status Read Command*)
EXT	Logic level on interrupt pin (pin 16) changed to low (Cleared after *Status Read Command*)
LBD	Low battery detect, the power supply voltage is below the pre-programmed limit
FFEM	FIFO is empty
ATS	Antenna tuning circuit detected strong enough RF signal
RSSI	The strength of the incoming signal is above the pre-programmed limit
DQD	Data quality detector output
CRL	Clock recovery locked
ATGL	Toggling in each AFC cycle
OFFS(6)	MSB of the measured frequency offset (sign of the offset value)
OFFS(3) -OFFS(0)	Offset value to be added to the value of the frequency control parameter (Four LSB bits)

Note: In order to get accurate values the AFC has to be disabled during the read by clearing the "*en*" bit in the AFC Control Command (bit 0).

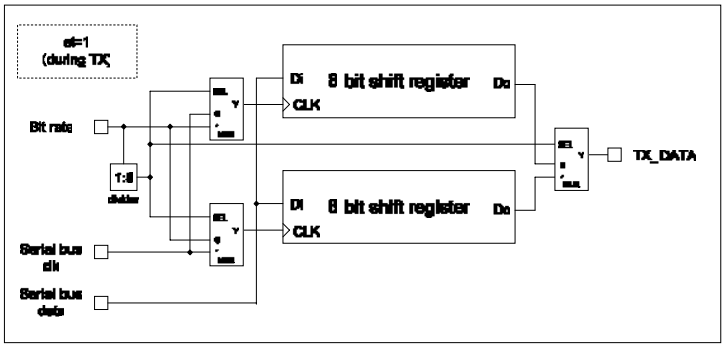
TX REGISTER BUFFERED DATA TRANSMISSION

In this operating mode (enabled by bit *el,* in the *Configuration Control Command*) the TX data is clocked into one of the two 8-bit data registers. The transmitter starts to send out the data from the first register (with the given bit rate) when bit *et* is set with the *Power Management Command*. The initial value of the data registers (AAh) can be used to generate preamble. During this mode, the SDO
pin can be monitored to check whether the register is ready (SDO is high) to receive the next byte from the microcontroller.

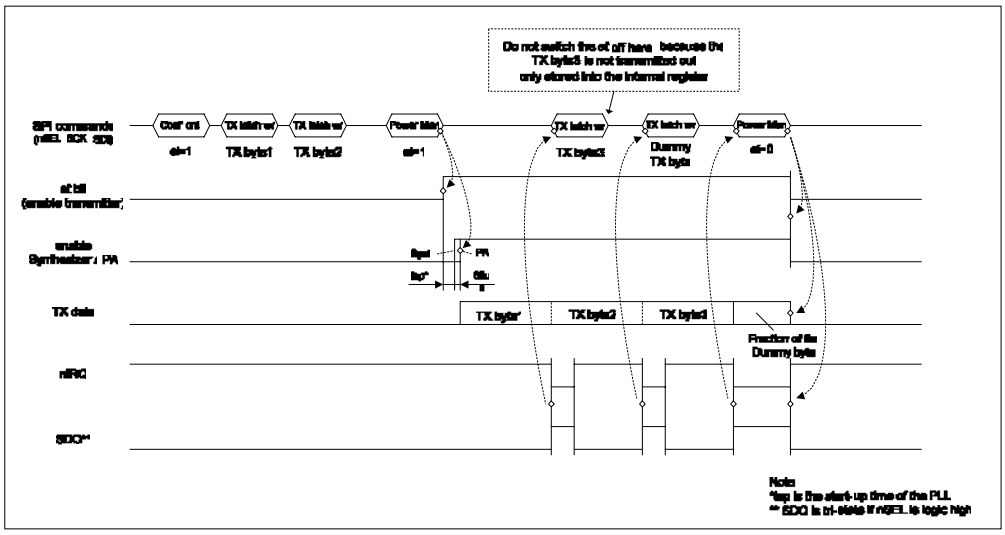
TX register simplified block diagram (before transmit)



TX register simplified block diagram (during transmit)



Typical TX register usage



Note: The content of the data registers are initialized by clearing bit *et*.

RX FIFO BUFFERED DATA READ

In this operating mode, incoming data are clocked into a 16 bit FIFO buffer. The receiver starts to fill up the FIFO when the Valid Data Indicator (VDI) bit and the synchron pattern recognition circuit indicates potentially real incoming data. This prevents the FIFO from being filled with noise and overloading the external microcontroller.

Interrupt Controlled Mode:

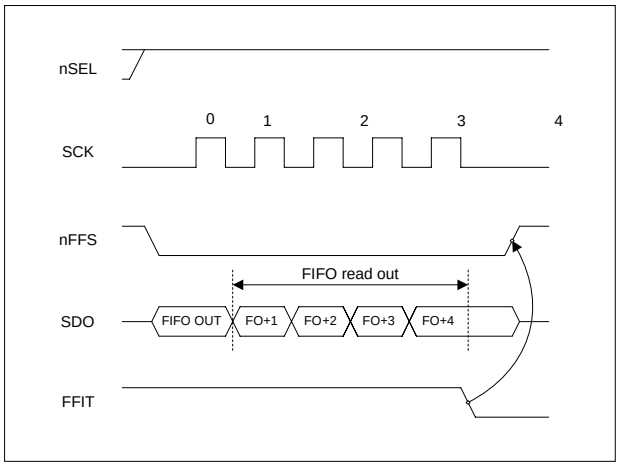
The user can define the FIFO IT level (the number of received bits) which will generate the nFFIT when exceeded. The status bits report the changed FIFO status in this case.

Polling Mode:

When nFFS signal is low the FIFO output is connected directly to the SDO pin and its content can be clocked out by the SCK. Set the
FIFO IT level to 1. In this case, as long as FFIT indicates received bits in the FIFO, the controller may continue to take the bits away. When FFIT goes low, no more bits need to be taken.

An SPI read command is also available to read out the content of the FIFO.

FIFO Read Example with FFIT Polling



Note:: During FIFO access f_{SCK} cannot be higher than f_{ref} /4, where f_{ref} is the crystal oscillator frequency. When the duty-cycle of the
clock signal is not 50 % the shorter period of the clock pulse should be at least $2/f_{ref}$.