Blackboard SE3-RDR100 Reader Circuit Description

The SE3-RDR100 Reader is designed to work with Blackboard's Point of Sales systems. The reader allows the use of Near Field Communication cards (Contactless) to be used in addition to the current series of mag-stripe readers. The function of SE3-RDR100 is to read an encrypted account number from an NFC card and transmit it to a cash register or similar device.

The reader is powered from a USB cable permanently attached to the device

The SE3-RDR100 contains two circuit boards, a main processor board and an antenna board. The main processor board contains a DS5250 Secure microcontroller, an NXP PN532 and a linear regulator. The DS5250 Secure microcontroller is a highly secure, 8051 compatible microprocessor which encrypts its program and data memory with a hardware-based data encryption standard algorithm.

The antenna board contains a loop antenna integrated on the PWB and three Light-Emitting diodes. The loop antenna consists of a continuous trace which circles around the board perimeter to create three loops. The effective loop size is approximately 1.6" x 3.0".

The two boards are connected by two through-hole headers which are soldered and permanently connect both boards.

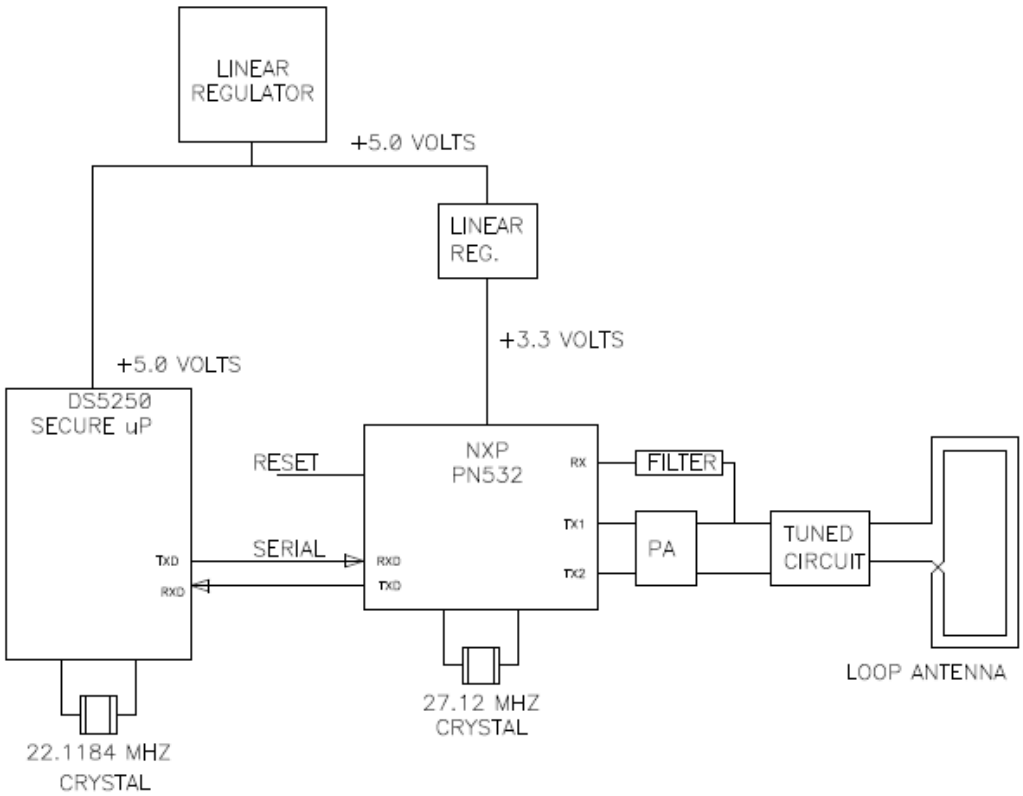
Power is supplied to the circuit board through a terminal block header.

13.56 MHz Circuitry

The SE3-RDR100 Reader supports Near Field Communication (NFC) in the unlicensed radio frequency ISM band of 13.56 MHz. The reader operates in the passive communication mode and supports ISO 14443A/MIFARE® and FeliCa™ contactless cards.

The SE3-RDR100 uses the PN532 from NXP. This device has an integrated transceiver module for contactless communication and is controlled by an embedded 80C51 microcontroller core. The PN532 is controlled by software from a MAXIM DS5250 Secure micro-controller. The two devices communicate over a serial UART.

A block diagram of the circuitry is shown below:



Circuit Operation

The PN532 uses an external crystal for a clock source. The crystal has a resonance frequency of 27.12 MHz. This clock is divided by 2 to generate the 13.56MHz carrier frequency.

The signal delivered on pin TX1 and pin TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. The data signal on the 13.56 MHz carrier uses 8% - 14% Amplitude-Shift-Keying (ASK) and is Manchester coded at a baud rate of 212 Kbits/second.

The power amplifier circuit consists of two symmetric emitter amplifiers. Each transistor is used as a switch. The TX1 and TX2 output pins of the PN532 generate digital signals which drive the base of each transistor through a base resistor. The resistor limits the current into the base. An AC-decoupling inductor is connected to the collector of each transistor and the power supply. The AC-decoupling inductor and the capacitor that shunts the transistor collector to ground interact as a 13.56 MHz oscillator. A resistor and capacitor connect the emitter of the transistor to ground. The resistor value controls the gain and limits the current.

The series inductor connected between the transistor collector and the capacitor to ground, provide an EMC filter. The series resistor connected directly to the loop antenna

is used to regulate the quality factor of the antenna. The capacitors and the resistors are used to achieve the required 13.56 MHz resonance frequency to achieve a quality factor for appropriate signal shaping according to ISO/IEC 14443.

The loop antenna is integrated in a PWB and was designed to have maximum area within the reader form factor. The dimensions of the antenna are 1.6” x 3.0”. The read range is approximately 2 inches.

The signal to the receiver is AC-coupled and filtered at the RX pin of the PN532.