AW-NM430

IEEE 802.11 1X1 b/g/n Wireless LAN and Bluetooth 4.2 12mm x 12mm LGA module

Datasheet

Rev. A

DF

(For Standard)

Features

WiFi

- Support 802.11n 1x1 SISO and HT40 operation
- IEEE 802.11n compliant with maximum data rates up to 150 Mbps (40 MHz channel)
- SDIO 2.0 interface for connecting WLAN technologies to the host processor
- Security support for WPA/WPA2 personal, WPS2.0
- Support 802.11w protected manages frames
- Support 802.11e QoS Enhancement(WMM)
- Support 802.11i WPA, WPA2. Open, shared key and pair-wise key authentication services

Bluetooth

- Compatible with Bluetooth v2.1+EDR and v4.2 Systems
- Supports Bluetooth 4.0 Low Energy(BLE)
- HS-UART interface for Bluetooth data tran smission compliant with H5 specification
- PCM interface for audio data transmission via Bluetooth controller

Revision History

Document NO: R2-2430-DST-01

Revision	Revision Date	DCN NO.	Description	Initials	Approved
A	2021/06/29	DCN022852	● Initial Version	Morris.	N.C. Chen

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AzureWave Technologies, Inc.

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the IEEE 802.11b/g/n WLAN LGA module – **AW-NM430.** With four advanced radio technologies integrated into a LGA module, AW-NM430 provides the best and most convenient SMT process. The module is targeted to mobile devices including**,** Tablet PC, Portable Media Players (PMPs), Portable Navigation Devices (PNDs), Personal Digital Assistants (PDAs), Tracking Devices, Gaming Devices which need convenient SMT process and low power consumption.

By using AW-NM430, the customers can easily integrate the Wi-Fi by a LGA card module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11b/g/n standard, the AW-NM430 uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-NM430.

The AW-NM430 supports standard interface **SDIO** for WLAN, **HS-UART** for Bluetooth.

1.2 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	802.11 1X1 b/g/n Wireless LAN and Bluetooth 4.2
Major Chipset	RTL8723DS-CG
Host Interface	WiFi + BT ● SDIO + UART
Dimension	12mm x 12mm x 1.8mm(max)
Form factor	LGA module
Antenna	● For LGA, “1T1R, external” Main：WiFi/Bluetooth → TX/RX
Weight	0.4910g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 b/g/n
Frequency Rage	WLAN: 2.4 GHz : 2.412 ~ 2.484 GHz
Modulation	WLAN:DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM
Number of Channels	WLAN 2.4GHz ■ USA, NORTH AMERICA, Canada and Taiwan – 1 ~ 11 ■ China, Australia, Most European Countries – 1 ~ 13
Output Power (Board Level Limit)(1)	**2.4G**

	Min	Typ	Max	Unit
11b (11Mbps) @EVM<35%	14	16	18	dBm
11g (54Mbps) @EVM≦-25 dB	12	14	16	dBm
11n (HT20 MCS7) @EVM≦-27 dB	11	13	15	dBm
11n (HT40 MCS7) @EVM≦-28 dB	11	13	15	dBm

<table>
<tr><td>Receiver Sensitivity</td><td>2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td></td><td>-83</td><td>-80</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td></td><td>-71</td><td>-68</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td></td><td>-67</td><td>-64</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td></td><td>-64</td><td>-61</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Data Rate</td><td>WLAN:
802.11b : 1, 2, 5.5, 11Mbps
802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n : up to 150Mbps-single</td></tr>
<tr><td>Security</td><td>WPA/WPA2</td></tr>
</table>

(1) If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

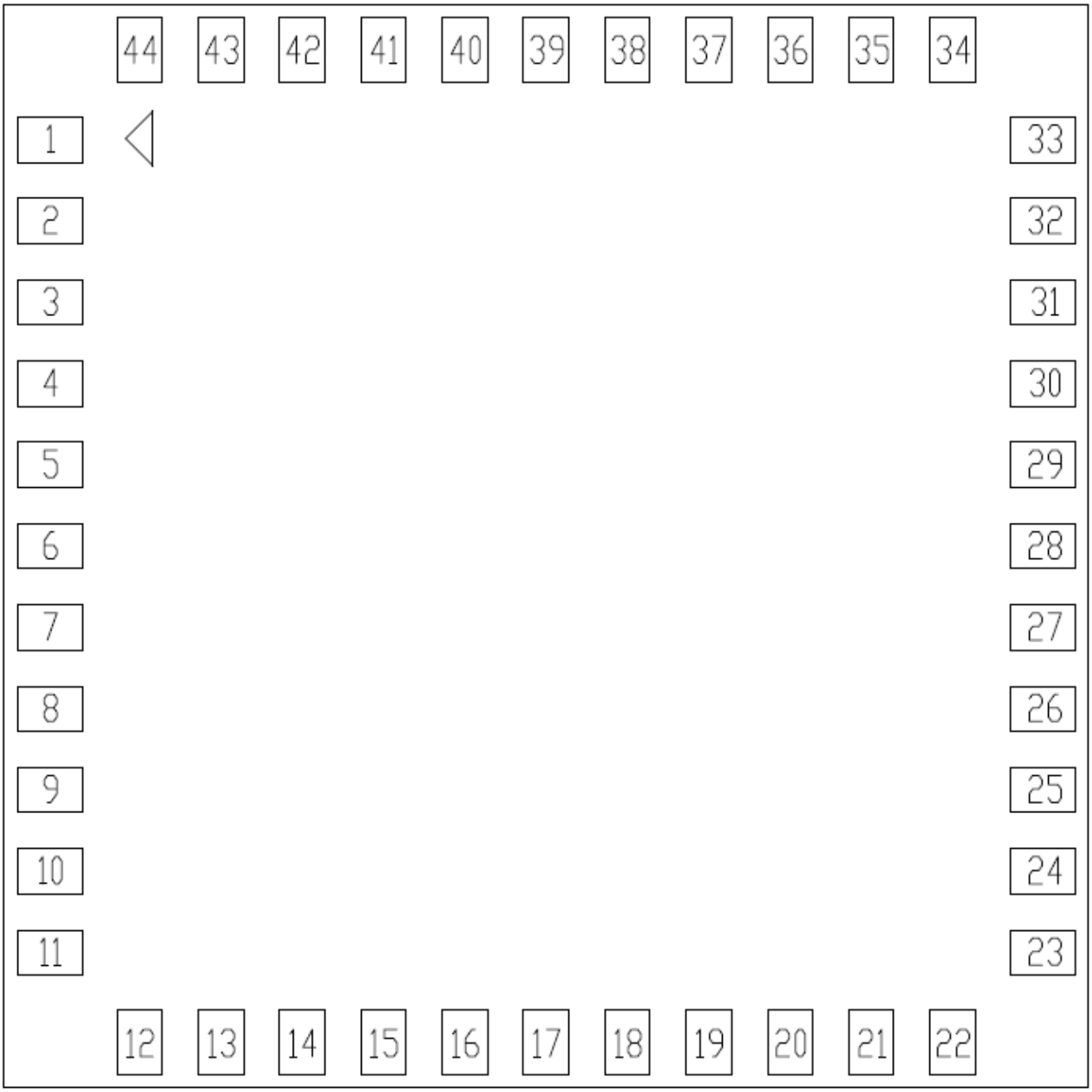
<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 2.1+Enhanced Data Rate (EDR) + BT4.2</td></tr>
<tr><td>Frequency Rage</td><td>2402~2480MHz</td></tr>
<tr><td>Modulation</td><td>GFSK (1Mbps), Π/4 DQPSK (2Mbps) and 8DPSK (3Mbps)</td></tr>
<tr><td>Output Power</td><td>BT Power
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BER</td><td>3</td><td>5</td><td>7</td><td>dBm</td></tr>
<tr><td>EDR</td><td>3</td><td>5</td><td>7</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>3</td><td>5</td><td>7</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity</td><td>BT Sensitivity (BER<0.1%)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BER</td><td></td><td>-91</td><td>-82</td><td>dBm</td></tr>
<tr><td>EDR</td><td></td><td>-83</td><td>-70</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td></td><td>-94</td><td>-70</td><td>dBm</td></tr>
</table></td></tr>
</table>

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V
Operating Temperature	0℃~70 ℃
Operating Humidity	less than 85%R.H
Storage Temperature	-40℃~90 ℃
Storage Humidity	less than 60%R.H
ESD Protection	
Human Body Model	3.5KV
Changed Device Model	500V

2. Pin Definition

2.1 Pin Map



AW-NM430 Pin Map (Top View)

2.2 Pin Table

Pin No.	Definition	Basic Description	Type	Voltage
1	GND_1	Ground	---	---
2	WL_BT_ANT	Option for RF I/O pin out	I/O	1.8V
3	GND_2	Ground	---	---
4	NC_1	Floating Pin, No connect to anything.	Floating	---
5	NC_2	Floating Pin, No connect to anything.	Floating	---
6	BT_WAKE	BT Device Wake	I	VDDIO
7	BT_HOST_WAKE	BT Host Wake	O	VDDIO
8	NC_3	Floating Pin, No connect to anything.	Floating	---
9	VD33	3.3V power voltage source input	P	3.3V
10	NC	Floating Pin, No connect to anything.	Floating	---
11	NC	Floating Pin, No connect to anything.	Floating	---
12	WL_DIS#	This Pin can externally shut down the RTL8723DS WLAN function when WL_DIS# is pulled low. When this Pin is pulled low, SDIO interface will be also disabled. This Pin can be also defined as the WLAN Radio-off function with host interface remaining connected.	I	VDDIO
13	WL_DEV_WAKE_HOST	WL Host Wake	I/O	VDDIO
14	SD_D2	SDIO Data line Bit[2]	I/O	VDDIO
15	SD_D3	SDIO Data line Bit[3]	I/O	VDDIO
16	SD_CMD	SDIO Command	I/O	VDDIO
17	SD_CLK	SDIO Clock input	I	VDDIO
18	SD_D0	SDIO Data line Bit[0]	I/O	VDDIO
19	SD_D1	SDIO Data line Bit[1]	I/O	VDDIO
20	GND_3	Ground	---	---
21	NC	Floating Pin, No connect to anything.	Floating	---
22	VDDIO	1.8V/3.3V Digital I/O Power Supply	P	1.8V/3.3V
23	NC	Floating Pin, No connect to anything.	Floating	---
24	LPO	External Low Power Clock input (32.768KHz)	I	VDDIO

25	PCM_OUT	PCM Data output	I/O	VDDIO
26	PCM_CLK	PCM Clock	I/O	VDDIO
27	PCM_IN	PCM data input	I/O	VDDIO
28	PCM_SYNC	PCM sync signal	I/O	VDDIO
29	NC	Floating Pin, No connect to anything.	Floating	---
30	TCXO_IN	External Xtal in	Floating	---
31	GND_4	Ground	---	---
32	NC_4	Floating Pin, No connect to anything.	Floating	---
33	GND_5	Ground	---	---
34	BT_DIS#	This Pin can externally shut down the RTL8723DS BT function when BT_DIS# is pulled low. When this Pin is pulled low, UART interface will be also disabled. This Pin can be also defined as the BT Radio-off function with host interface remaining connected.	I	VDDIO
35	NC_5	Floating Pin, No connect to anything.	Floating	---
36	GND_6	Ground	---	---
37	NC	Floating Pin, No connect to anything.	Floating	---
38	NC	Floating Pin, No connect to anything.	Floating	---
39	NC_6	GPIO Mode : GPIO[8]. Bluetooth External Coexistence Mode : BT_FREQ.	I/O	VDDIO
40	NC_7	GPIO Mode : GPIO[9]. Bluetooth External Coexistence Mode : BT_STATE.	I/O	VDDIO
41	UART_RTS	Module internal default pull down. Floating Pin, No connect to anything.	Floating	---
42	UART_OUT	UART_OUT High speed UART DATA OUT	O	---
43	UART_IN	UART_IN High speed UART Data In	I	---
44	UART_CTS	UART_CTS High speed UART DTS	I	---

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD33	3.3V input	-	3.3	3.6	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD33	3.3V power supply	3.0	3.3	3.6	V
VDDIO	Digital IO Supply Voltage	1.62	1.8~3.3	3.6	V

3.3 Digital IO Pin DC Characteristics

3.3.1 3.3V Operation

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	-	0	0.9	
V_{OH}	Output high voltage	2.97	-	3.3	
V_{OL}	Output low voltage	0	-	0.33	

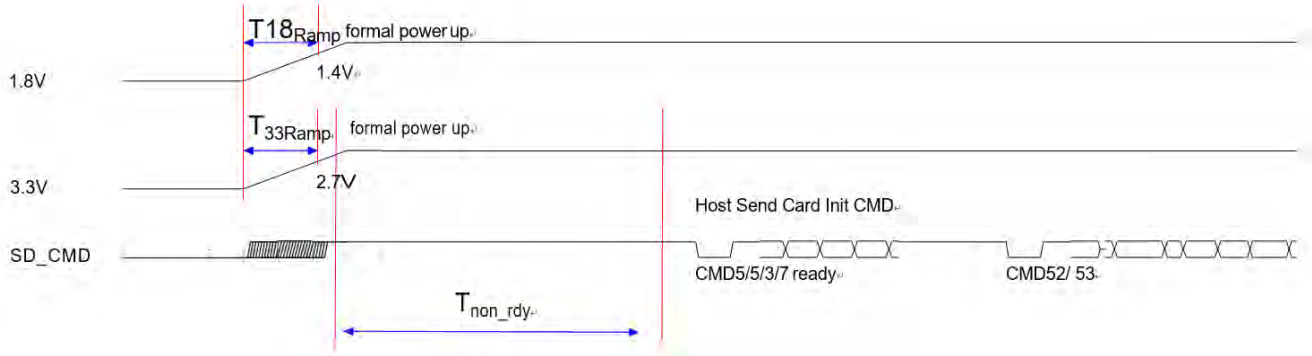
2.8v Operation

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	1.8	2.8	3.1	V
V_{IL}	Input low voltage		0	0.8	
V_{OH}	Output high voltage	2.5	-	3.1	
V_{OL}	Output low voltage	0	-	0.28	

1.8v Operation

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	1.3	1.8	2.0	V
V_{IL}	Input low voltage	-	0	0.8	
V_{OH}	Output high voltage	1.62	-	1.8	
V_{OL}	Output low voltage	0	-	0.18	

3.4 SDIO Power-On Sequence

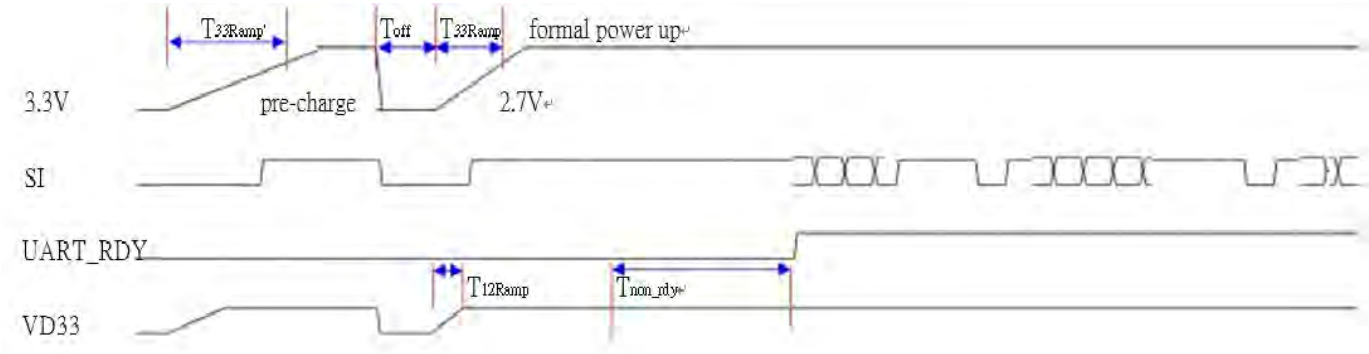


Symbol	Description
T_{33ramp}	The 3.3V main power ramp up duration.
T_{18ramp}	The 1.8V main power ramp up duration.
T_{non_rdy}	SDIO Not Ready Duration. In this state, the RTL8723DS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.

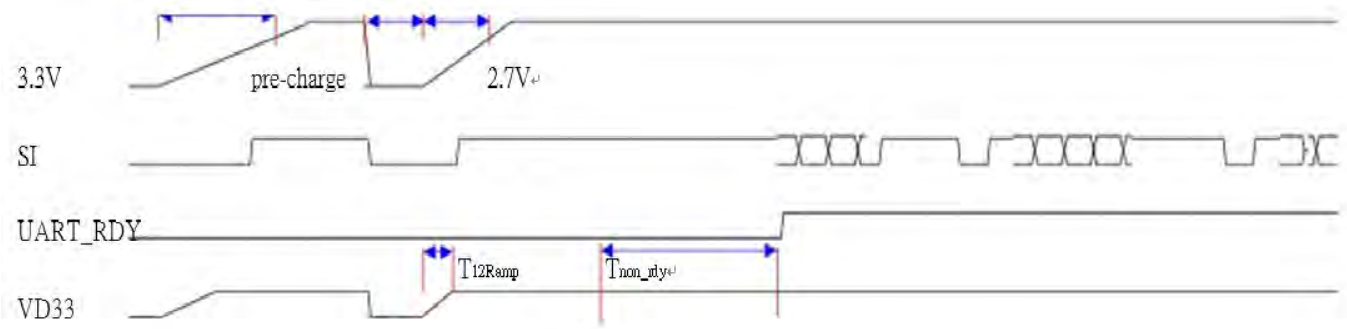
Symbol	Min	Typical	Max	Units
T_{33ramp}	0.2	0.5	2.5	ms
T_{18ramp}	0.2	0.5	2.5	ms
T_{non_rdy}	1	2	2.5	ms

3.5 UART Interface Power-On Sequence

3.5.1 UART Hardware Flow Control Not Supported



3.5.2 UART Hardware Flow Control Supported



Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommended that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fail.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the RTL8723DS will not respond to any commands.

Symbol	Min	Typical	Max	Units
T_{33ramp}	0.2	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.2	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{non_rdy}	1	2	10	ms

3.6 Power Consumption*

3.6.1 WLAN

No.	Item	VBAT_IN=3.3V

Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit			Receive	
				Max.	Avg.	DUTY %	Max.	Avg.
2.4	11b@1Mbps	20	16	278.4	277.1	98.8%	93.8	85.5
	11g@54Mbps	20	14	144.2	142.7	29.8%	96.2	91.8
	11n@MCS7	40	13	136.4	135.2	27.7%	96.9	94.2

No.	Mode	VBAT_IN=3.3V	
		Max.	Avg.
1	Radio Off	21uA	21uA
2	Power Save DTM 1 (2.4GHz)	160uA	2.7mA
3	Power Save DTM 3 (2.4GHz)	237uA	1.4mA

* The power consumption is based on Azurewave test environment, these data for reference only.

* Current Unit: mA

3.6.2 Bluetooth

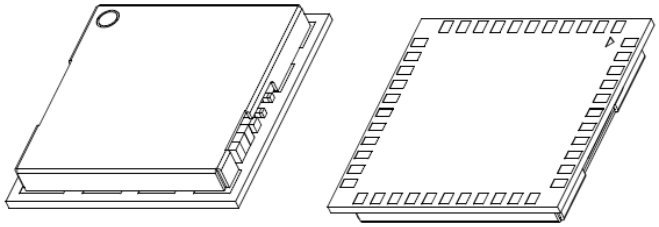
No.	Mode	VBAT_IN=3.3V	
		Max.	Avg.
1	Transmit	64.1	51.5(124.22kB/s)
2	Receive	50.6	46.3(207.33kB/s)

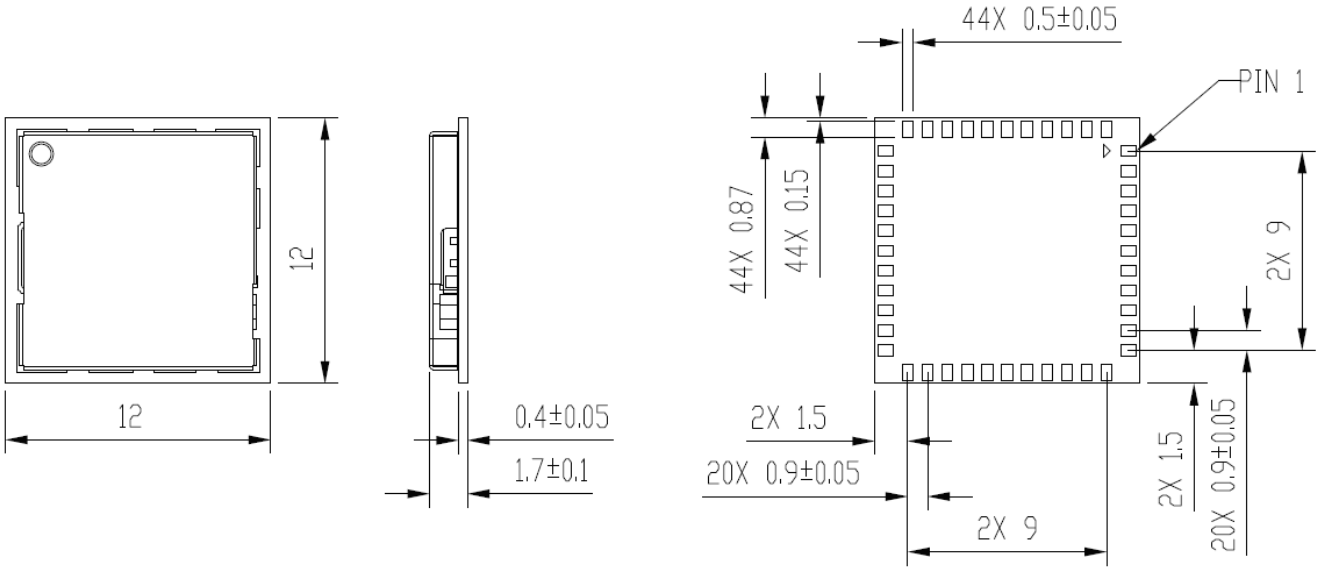
* The power consumption is based on Azurewave test environment, these data for reference only.

* Current Unit: mA

4. Mechanical Information

4.1 Mechanical Drawing



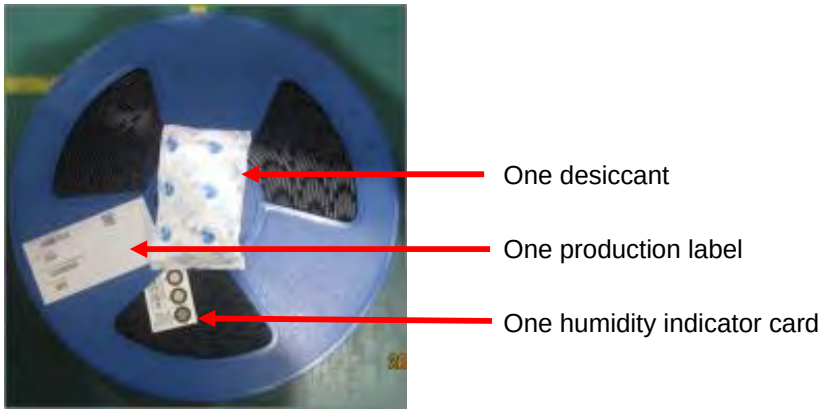


Unit: mm

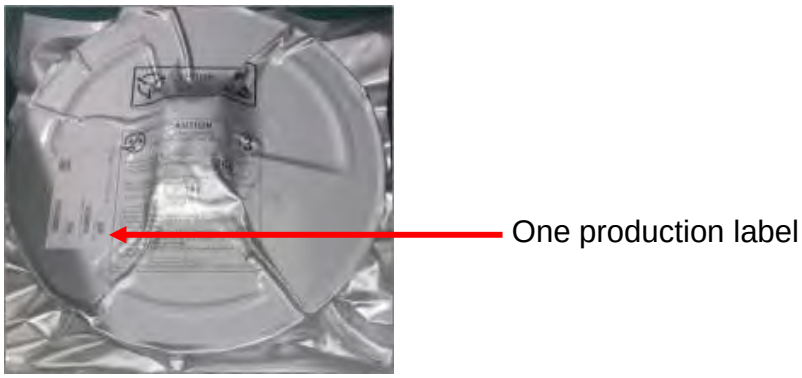
5. Packaging Information

One reel can pack 1,500pcs 12x12 LGA modules

1. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel



2. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag



3. A bag is put into the anti-static pink bubble wrap

4. A bubble wrap is put into the inner box and then one label is pasted on the inner box

One production label

5. 5 inner boxes could be put into one carton

6. Sealing the carton by AzureWave tape

7. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on

the carton

One carton label

One box label

AzureWave Technologies, Inc.

Layout Guide

Rev. C

(For Standard)

Revision History

Version	Revision Date	Description	Initials	Approved
A	2019/08/01	● Initial Version	Renton Tao	N.C. Chen
B	2020/04/22	● Modify module type name	Jimmy Chen	N.C. Chen
C	2021/08/30	● Modify RF Trace Guide	Morris Huang	N.C. Chen

INTRODUCTION

This document provides key guidelines and recommendations to be followed when creating AW-NM430 layout. It is strongly recommended that layouts be reviewed by the AzureWave engineering team before being released for fabrication.

The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

- GENERAL RF GUIDELINES
- Ground Layout
- Power Layout
- Digital Interface
- RF Trace
- Antenna
- Antenna Matching
- GENERAL LAYOUT GUIDELINES
- THE OTHER LAYOUT GUIDE INFORMATION

1. GENERAL RF GUIDELINES

Follow these steps for optimal WLAN performance.

1. Control WLAN 50 ohm RF traces by doing the following:
   - Route traces on the top layer as much as possible and use a continuous reference ground plane underneath them.
   - Verify trace distance from ground flooding. At a minimum, there should be a gap equal to the width of one trace between the trace and ground flooding. Also keep RF signal lines away from metal shields. This will ensure that the shield does not detune the signals or allow for spurious signals to be coupled in.
   - Keep all trace routing inside the ground plane area by at least the width of a trace.
   - Check for RF trace stubs, particularly when bypassing a circuit.

2. Keep RF traces properly isolated by doing the following:
   - Do not route any digital or analog signal traces between the RF traces and the reference ground.
   - Keep the balls and traces associated with RF inputs away from RF outputs. If two RF traces are close each other, then make sure there is enough room between them to provide isolation with ground fill.
   - Verify that there are plenty of ground vias in the shield attachment area. Also verify that there are no non-ground vias in the shield attachment area. Avoid traces crossing into the shield area on the shield layer.

3. Consider the following RF design practices:
   - Confirm antenna ground keep-outs.
   - Verify that the RF path is short, smooth, and neat. Use curved traces or microwave corners for all turns; never use 90-degree turns. Avoid width discontinuities over pads. If trace widths differ significantly from component pad widths, then the width change should be mitered. Verify there are no stubs.
   - Do not use thermals on RF traces because of their high loss.
   - The RF traces between AW-NM430 RF_ANT pin and antenna must be made using 50Ω controlled-impedance transmission line.

2. Ground Layout

Please follow general ground layout guidelines. Here are some general rules for customers' reference.

- The layer 2 of PCB should be a complete ground plane. The rule has to be obeyed strictly in the RF section while RF traces are on the top layer.
- Each ground pad of components on top layer should have via drilled to PCB layer 2 and via should be as close to pad as possible. A bulk decoupling capacitor needs two or more.
- Don't place ground plane and route signal trace below printed antenna or chip antenna to avoid destroying its electromagnetic field, and there is no organic coating on printed antenna. Check antenna chip vendor for the layout guideline and clearance.
- Move GND vias close to the pads.

3. Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

- A 4.7uF capacitor is used to decouple high frequency noise at digital and RF power terminals. This capacitor should be placed as close to power terminals as possible.
- In order to reduce PCB's parasitic effects, placing more via on ground plane is better.

4. Digital Interface

Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

- The digital interface to the module must be routed using good engineering practices to minimize coupling to power planes and other digital signals.
- The digital interface must be isolated from RF trace.

5. RF Trace

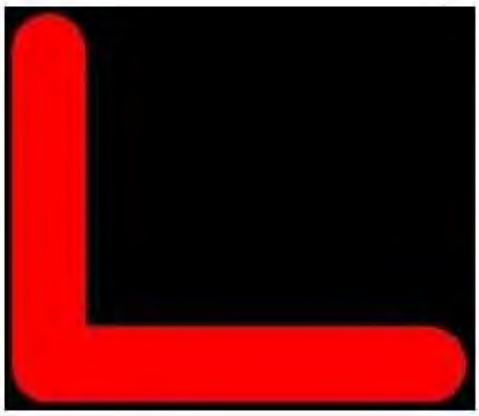
The RF trace is the critical to route. Here are some general rules for customers' reference.

- The RF trace impedance should be 50Ω between ANT port and antenna matching network.
- The length of the RF trace should be minimized.
- To reduce the signal loss, RF trace should laid on the top of PCB and avoid any via on it.

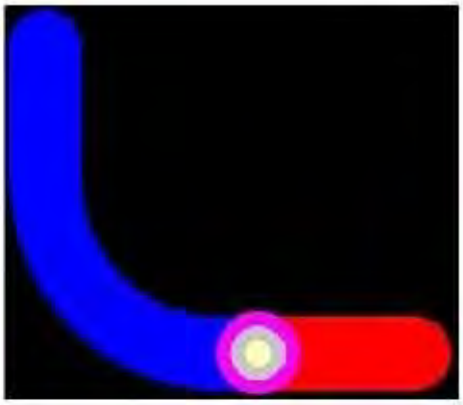
- The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.
- The RF trace must be isolated with aground beneath it. Other signal traces should be isolated from the RF trace either by ground plane or ground vias to avoid coupling.
- To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

If the customers have any problem in calculation of trace impedance, please contact AzureWave.

Correct RF trace



Right-angled corner

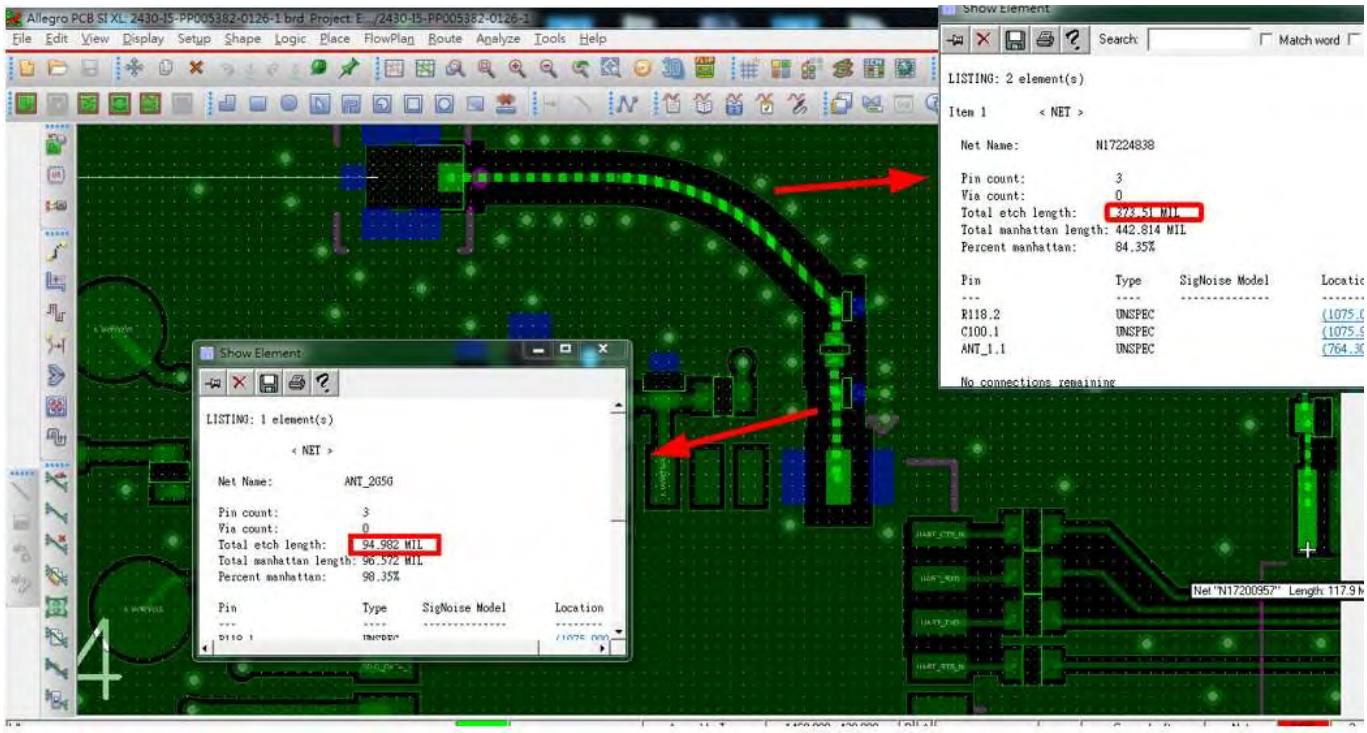


Via on RF trace

Incorrect RF trace

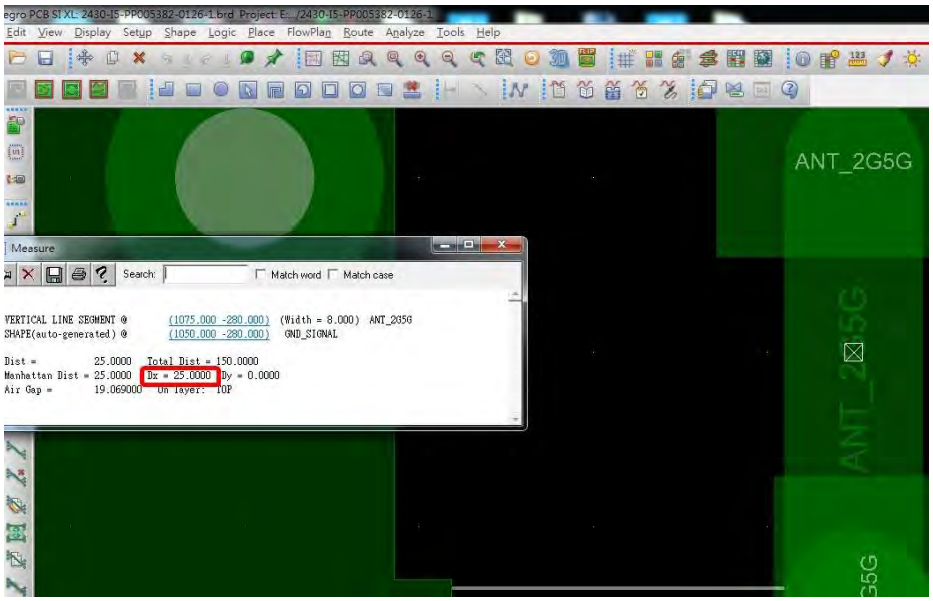
AW-NM430 RF trace should be follow the rules as below

a. Line length of Antenna trace about 373.5 mil and 94.9 mil



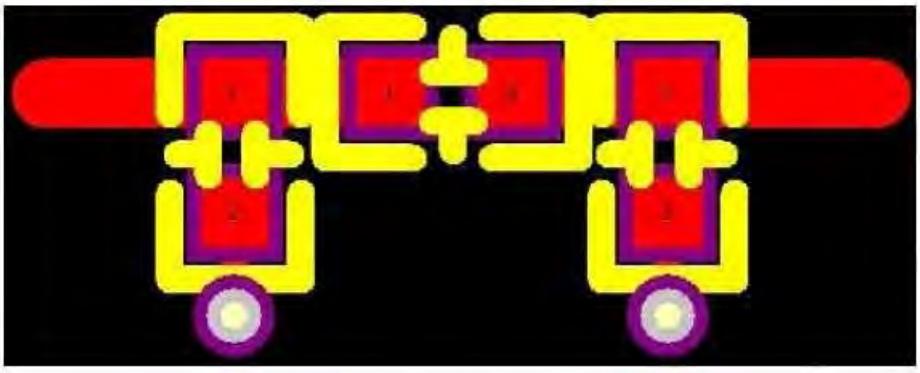
b. Line width of Antenna trace about 8 mil

c. Air gap between RF trace and ground about 25 mil

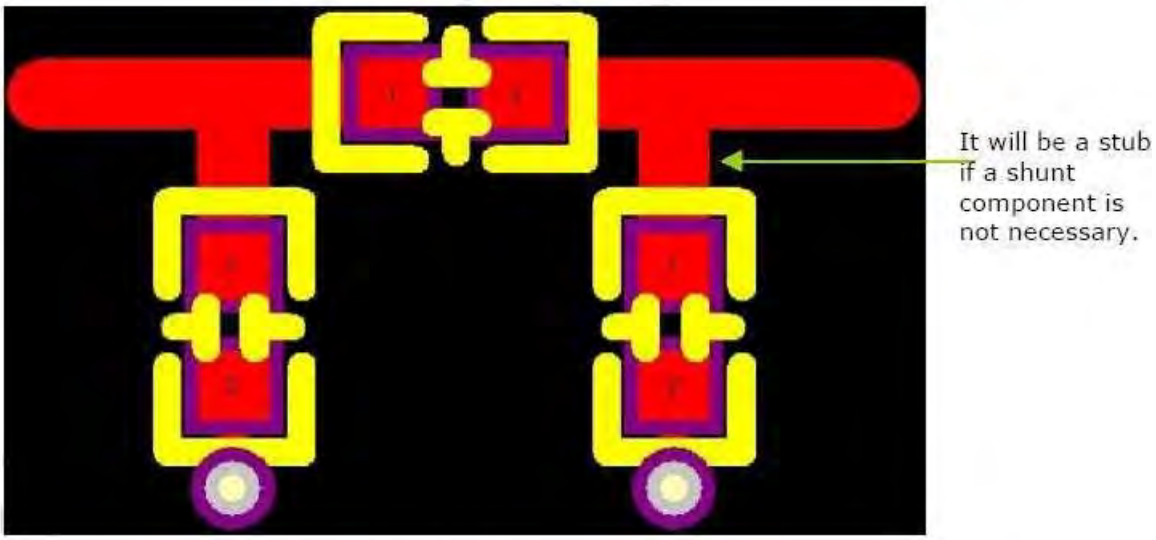


6. Antenna Matching

PCB designer should reserve an antenna matching network for post tuning to ensure the antenna performance in different environments. Matching components should be close to each other. Stubs should also be avoided to reduce parasitic while no shunt component is necessary after tuning.



Correct layout for antenna matching



Incorrent layut for antenna matching

7. GENERAL LAYOUT GUIDELINES

Follow these guidelines to obtain good signal integrity and avoid EMI:

1. Place components and route signals using the following design practices:
   • Keep analog and digital circuits in separate areas.

• Identify all high-bandwidth signals and their return paths. Treat all critical signals as current loops. Check each critical loop area before the board is built. A small loop area is more important than short trace lengths.

• Orient adjacent-layer traces so that they are perpendicular to one another to reduce crosstalk.

• Keep critical traces on internal layers, where possible, to reduce emissions and improve immunity to external noise.

However, RF traces should be routed on outside layers to avoid the use of vias on these traces.

• Keep all trace lengths to a practical minimum. Keep traces, especially RF traces, straight wherever possible. Where turns are necessary, use curved traces or two 45-degree turns. Never use 90-degree turns.

2. Consider the following with respect to ground and power supply planes:

• Route all supply voltages to minimize capacitive coupling to other supplies. Capacitive coupling can occur if supply traces on adjacent layers overlap. Supplies should be separated from each other in the stack-up by a ground plane, or they should be coplanar (routed on different areas of the same layer).

• Provide an effective ground plane. Keep ground impedance as low as possible. Provide as much ground plane as possible and avoid discontinuities. Use as many ground vias as possible to connect all ground layers together.

• Maximize the width of power traces. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.

3. Consider these power supply decoupling practices:

• Place decoupling capacitors near target power pins. If possible, keep them on the same side as the IC they decouple to avoid vias that add inductance. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it by a copper trace. Instead, make the connection directly to the associated planes using vias.

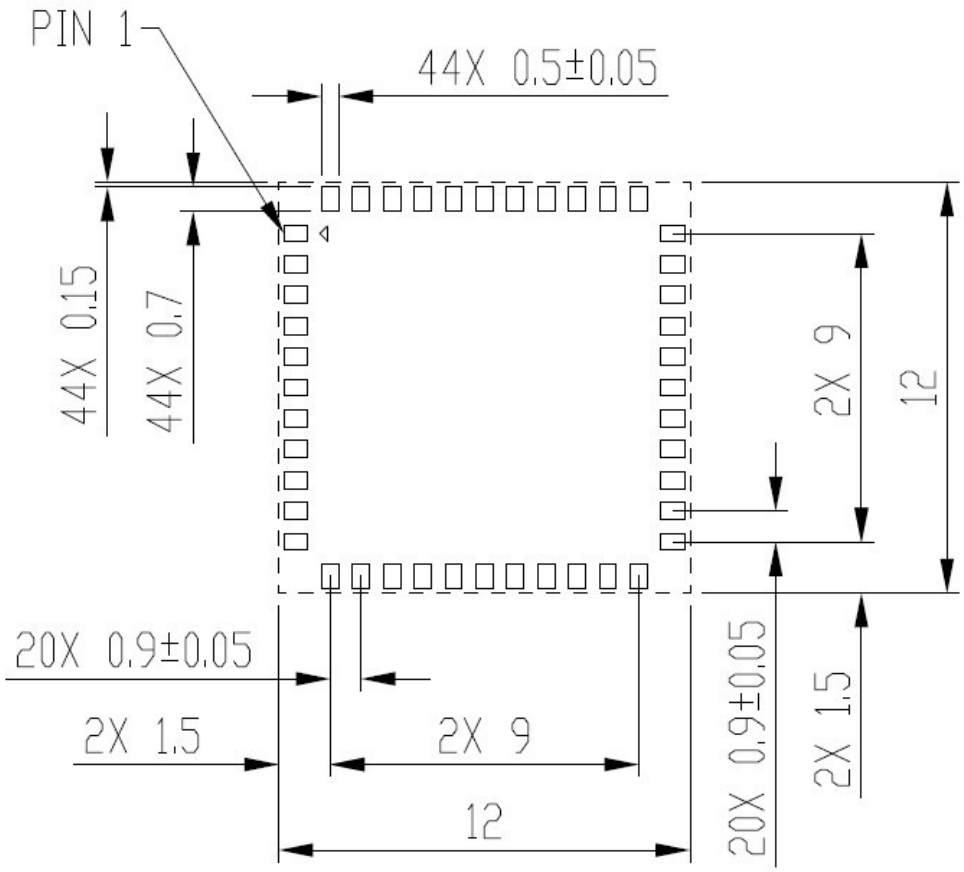
• Use appropriate capacitance values for the target circuit, and consider each capacitor's self-resonant frequency.

10. Stamp Module stencil and Pad opening Suggestion

- Stencil thickness：0.10~0.12mm
- Function Pad opening size suggestion: Max. 1:1

PS: This opening suggestion just for customer reference, please discuss with AzureWave's Engineer before you start SMT.

- Solder Printer Opening and Customer PCB Footprint suggestion.
- Example:



RECOMMENDED PCB LAYOUT (TOP VIEW)

11. The other layout guide Information

• Make sure every power traces have good return path (ground path).

• Connect the input pins of unused internal regulators to ground.

• Leave the output pins of unused internal regulators floating.

• High speed interface (i.e. UART/SDIO/HSIC) shall have equal electrical length. Keep them away from noise sensitive blocks.

• Good power integrity of VDDIO will improve the signal integrity of digital interfaces.

• Good return path and well shielded signal can reduce crosstalk, EMI emission and improve signal integrity.

• RF IO is around 50 ohms, reserve Pi or T matching network to have better signal transition from port to port.

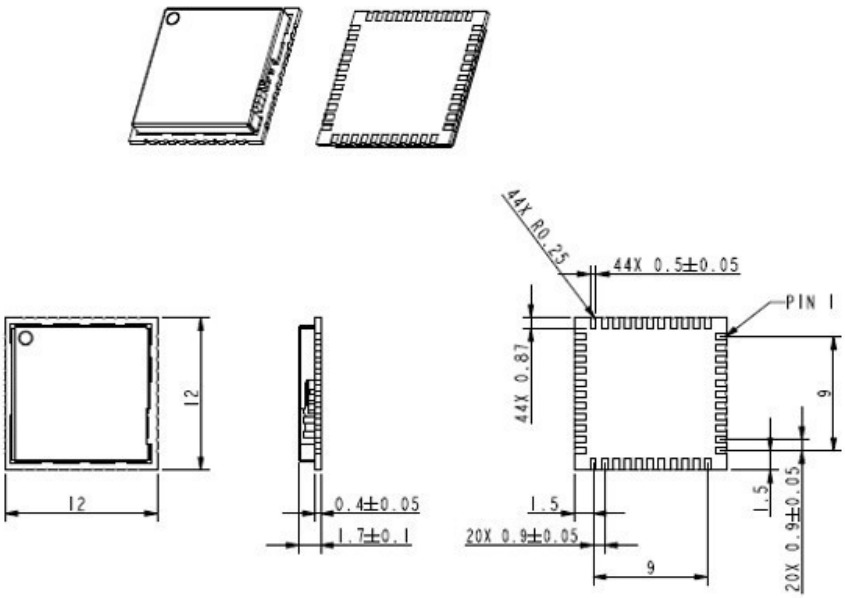
• Smooth RF trace help to reduce insertion loss. Do not use 90 degrees turn (use two 45 degrees turns or one miter bend instead).

• Well arranged ground plane near antenna and antenna itself will help to reduce near field coupling between other RF sources (e.g. GSM/CDMA … antennas).

• Discuss with AzureWave Engineer after you finish schematic and layout job.

12. Mechanical Drawing

•Package Outline Drawing



Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

IMPORTANT NOTE:

This module is intended for OEM integrator. This module is only FCC authorized for the specific rule parts listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Additional testing and certification may be necessary when multiple modules are used.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following " Contains TX FCC ID: TLZ-NM430SM ".

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

Antenna List

Ant.	Brand	Model Name	Antenna Type	Connector	Gain (dBi)
1	YAGEO	ANT3216A063R2400A	Chip Antenna	I-PEX	1.69
2	MAG. LAYERS	MSA-4008-25GC1-A2	PIFA Antenna	I-PEX	2.98

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:
(1) This device may not cause interference.
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil contient des émetteurs / récepteurs exempts de licence qui sont conformes au (x) RSS (s) exemptés de licence d'Innovation, Sciences et Développement économique Canada. L'opération est soumise aux deux conditions suivantes:
(1) Cet appareil ne doit pas provoquer d'interférences.
(2) Cet appareil doit accepter toute interférence, y compris les interférences susceptibles de provoquer un fonctionnement indésirable de l'appareil.

This device and its antenna(s) must not be co-located with any other transmitters except in accordance with IC multi-transmitter product procedures.
Referring to the multi-transmitter policy, multiple-transmitter(s) and module(s) can be operated simultaneously without reassessment permissive change.
Cet appareil et son antenne (s) ne doit pas être co-localisés ou fonctionnement en association avec une autre antenne ou transmetteur.

This radio transmitter [6100A-NM430SM] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Le présent émetteur radio (6100A-NM430SM) a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal d'antenne. Les types d'antennes non inclus dans cette liste qui ont un gain supérieur au gain maximal indiqué pour tout type listé sont strictement interdits pour une utilisation avec cet appareil.

IMPORTANT NOTE:
IC Radiation Exposure Statement:
This equipment complies with IC RSS-102 radiation exposure limits set forth

for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

IMPORTANT NOTE:

This module is intended for OEM integrator. The OEM integrator is responsible for the compliance to all the rules that apply to the product into which this certified RF module is integrated.

Additional testing and certification may be necessary when multiple modules are used.

20cm minimum distance has to be able to be maintained between the antenna and the users for the host this module is integrated into. Under such configuration, the IC RSS-102 radiation exposure limits set forth for an population/uncontrolled environment can be satisfied.

Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the IC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment. Operation is subject to the following two conditions: (1) this device may not cause harmful interference (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following " Contains IC: 6100A-NM430SM".

The Host Model Number (HMN) must be indicated at any location on the exterior of the end product or product packaging or product literature which shall be available with the end product or online.

Antenna List

Ant.	Brand	Model Name	Antenna Type	Connector	Gain (dBi)
1	YAGEO	ANT3216A063R2400A	Chip Antenna	I-PEX	1.69
2	MAG. LAYERS	MSA-4008-25GC1-A2	PIFA Antenna	I-PEX	2.98