AW-HM482

IEEE 802.11ah Wireless LAN Module

Datasheet

Rev. B

DF

(For STD)

Features

General

- Supports 903 ~ 927MHz frequency band
- Supports single-stream 150kbps ~ 15Mbps data rate
- Supports AP and STA mode

Host interface

- UART and SPI support for host interface

Standards Supported

- IEEE Std 802.11ah-2016 compliant
- Security: OPEN, WPA2-PSK(AES), WPA3-OWE, WPA3-SAE

MAC Features

- S1G Beacon, NDP Control frame, TIM compression, Unified scaling factor for max idle period/listen interval/WNM-sleep interval, STA Type, S1G baseline functions (DCF, HCF, multi-rate support, A-MPDU), and S1G BSS operation
- Network efficiency enhancements: PV1 frames, NDP PS-Poll/PS-Poll Ack/Probe Req./Probe Resp., RAW avoidance, TSBTT, and Differentiated EDCA Parameter
- Power saving: Non-TIM operation, dynamic AID assignment, TWT, and Rescheduling STA's doze/awake cycle
- Wider coverage: Relay
- BSS scalability (up to 1024 STAs): Multicast AID, and Authentication control
- Low-cost STA/AP: EL operation, Flow Control

Peripheral Interfaces

- I2C, SPI and UART
- A Wi-Fi dedicated HSPI for data transfer to Host

Peripheral Interfaces

- Full IEEE 802.11ah compatibility with enhanced performance
- Supports 1/2/4 MHz channel with optional SGI
- Supports S1G_1M, Short/Long format
- Modulation: OFDM with BPSK, QPSK, 16QAM, 64QAM

Revision History

Document NO: R2-2482-DST-01

AzureWave Technologies, Inc.

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/08/25	DCN018492	● Initial version	Daniel Lee	N.C. Chen
B	2021/05/18	DCN022034	● Add Power Consumption and ESD Data ● Modify Frequency Range	Daniel Lee	N.C. Chen

Table of Contents

1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the pioneer of the IEEE 802.11ah WIFI solder down module --- **AW-HM482**. The **AW-HM482** is the smallest IEEE 802.11ah Wi-Fi module that operates in the Sub 1GHz license-exempt band, offering longer ranger and higher data rate for internet of things (IoT) applications. The **AW-HM482** enables streamlined data transfer interoperability with existing Wi-Fi networks while meeting up to 1Km long range data transfer with low power consumption requirements.

The **AW-HM482** integrated Newracom NRC7292 and external RF front end module (FEM) which can increase transmission power up to 23dBm. Two embedded ARM processors, Cortex-M0 and Cortex-M3, in the NRC7292 offers rich processing power to accommodate Wi-Fi subsystem as well as user application in a single Wi-Fi SoC. NRC7292 also includes two host interfaces, HSPI and UART, and many peripherals such as general SPI, I2C, UART, PWM, auxiliary ADC and GPIOs. In addition, it provides a memory large enough for both AP (access point) and STA (station) operation. The low-leakage retention memory can be used to store code and data necessary for fast wake-up from deep-sleep mode.

1.2 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11ah Wireless LAN Module
Major Chipset	Newracom NRC7292 (268-pin CABGA)
Host Interface	SPI
Dimension	18mm x 24mm x 2.55mm (Tolerance remarked in mechanical drawing)
Form Factor	LGA module, 74 pins
Antenna	● For LGA, “1T1R, external” ANT Main：TX/RX
Weight	2.2g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11ah
WLAN VID/PID	TBD
WLAN SVID/SPID	TBD
Frequency Rage	(US/CA): Unit MHz 1MHz Bandwidth: 903.5, 904.5, 905.5, 906.5, 907.5, 908.5, 909.5, 910.5, 911.5, 912.5, 913.5, 914.5, 915.5, 916.5, 917.5, 918.5, 919.5, 920.5, 921.5, 922.5, 923.5, 924.5, 925.5, 926.5 2MHz Bandwidth: 905, 907, 909, 911, 913, 915, 917, 919, 921, 923, 925 4MHz Bandwidth: 906, 910, 914, 918, 922
Modulation	OFDM, BPSK, QPSK, 16-QAM, 64-QAM
Channel Bandwidth	1/2/4 MHz
Output Power **(Board Level Limit)***	

	Min	Typ	Max	Unit
MCS0 (1/2/4 MHz)	20.5	22	23.5	dBm
MCS7 (1/2/4 MHz)	17.5	19	20.5	dBm

	MCS10 (1 MHz)	20.5	22	23.5	dBm

Receiver Sensitivity

	Min	Typ	Max	Unit
MCS0 (1 MHz)		-106	-95	dBm
MCS0 (2 MHz)		-99	-92	dBm
MCS0 (4 MHz)		-98	-89	dBm
MCS7 (1 MHz)		-88	-77	dBm
MCS7 (2 MHz)		-84	-74	dBm
MCS7 (4 MHz)		-81	-71	dBm
MCS10 (1 MHz)		-109	-98	dBm

Data Rate

- 1 MHz Bandwidth: up to 3Mbps
- 2 MHz Bandwidth: up to 6.5Mbps
- 4 MHz Bandwidth: up to 13.5Mbps

Security

- OPEN, WPA2-PSK(AES), WPA3-OWE, WPA3-SAE

standard

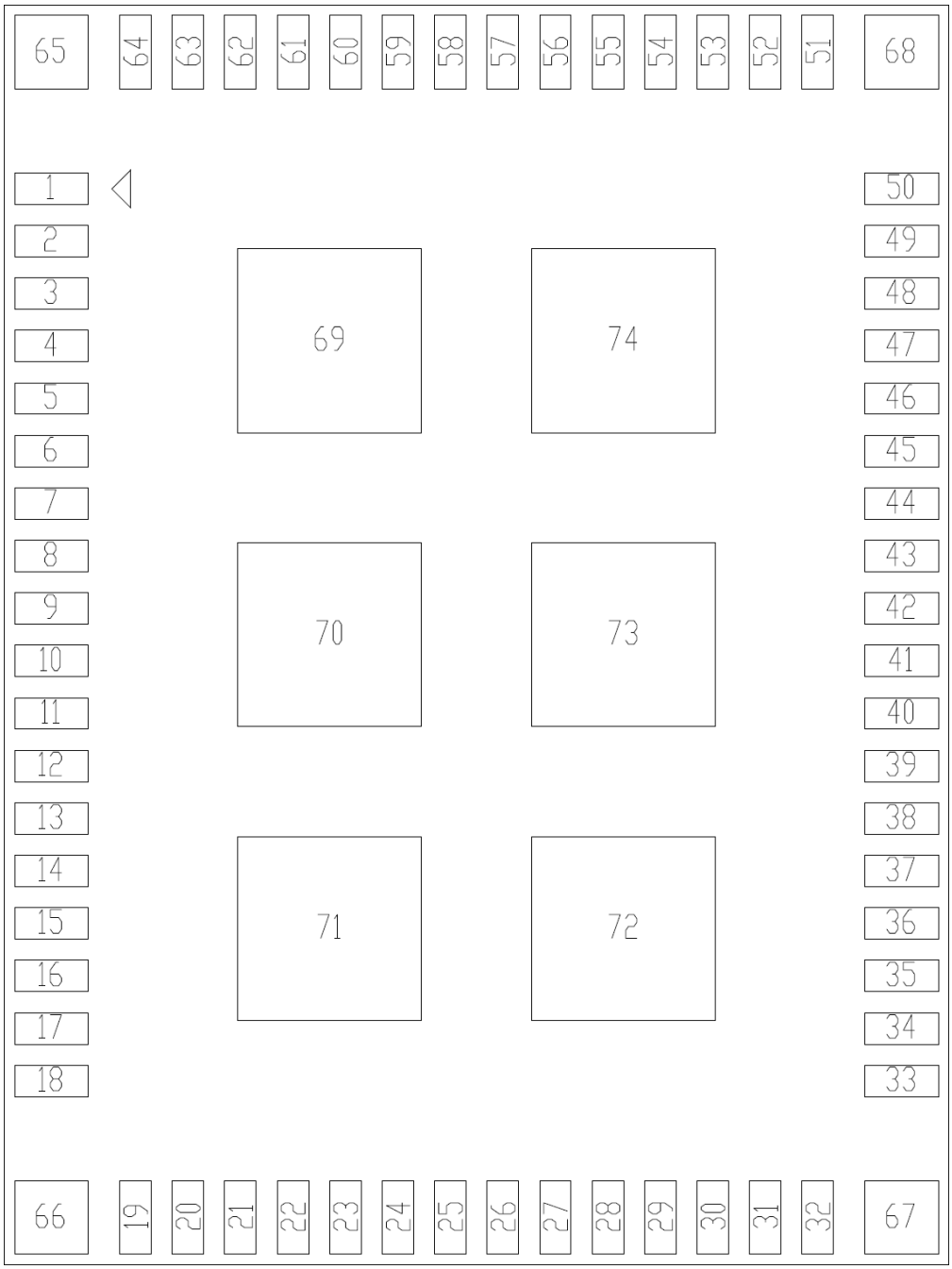
*** If you have any certification questions about output power please contact FAE directly.**

1.3.3 Operating Conditions

Features	Description
Operating Conditions	
Voltage	VBAT: 3.3V VDD_FEM: 4.0V VDDIO: 3.3V
Operating Temperature	-20℃~70 ℃
Operating Humidity	less than 85%R.H
Storage Temperature	-30℃~85 ℃
Storage Humidity	less than 60%R.H
ESD Protection	
Human Body Model	±2KV per ANSI/ESDA/JEDEC JS-001-2017
Changed Device Model	±500V per ESDA/JEDEC JS-002-2018

2. Pin Definition

2.1 Pin Map



AW-HM482 Pin Map (Top View)

2.2 Pin Table

Pin No.	Definition	Basic Description	Voltage	Type
1	GND	GROUND		GND
2	GND	GROUND		GND
3	GND	GROUND		GND
4	GND	GROUND		GND
5	VDD_FEM	Front End Module power input	4.0V	Power
6	VBAT	3.3V power supply	3.3V	Power
7	GND	GROUND		GND
8	GND	GROUND		GND
9	MODE_00	SW Define (When ROM BOOT) 11: Internal SRAM BOOT		I
10	MODE_01			I
11	MODE_02	0: ROM BOOT 1: XIP BOOT		I
12	MODE_03	0: Cortex-M0 Master 1: Cortex-M3 Master		I
13	MODE_04	0: Two CPU 1: One CPU		I
14	GND	GROUND		GND
15	HSPI_CSn	Host SPI – Chip Select (active low)		I
16	HSPI_CLK	Host SPI – Clock		I
17	HSPI_MISO	Host SPI – Master in Slave out		O
18	HSPI_MOSI	Host SPI – Master out Slave in		I
19	HSIP_EIRQ	Host SPI – Interrupt		O
20	GND	GROUND		GND
21	GND	GROUND		GND
22	GP_00_UART2_TX	UART Channel2 Tx		I/O
23	GP_01_UART2_RX	UART Channel2 Rx		I/O

24	GP_02_UART2_RTS	UART Channel2 RTS		I/O
25	GP_03_UART2_CTS	UART Channel2 CTS		I/O
26	GP_04_UART0_TX	UART Channel0 Tx		I/O
27	GP_05_UART0_RX	UART Channel0 Rx		I/O
28	GP_06_UART3_TX	UART Channel3 Tx		I/O
29	GP_07_UART3_RX	UART Channel3 Rx		I/O
30	GP_08_UART1_RX	UART Channel1 Rx		I/O
31	GP_11_UART1_TX	UART Channel1 Tx		I/O
32	GP_17_I2C_SDA	I2C_SDA		I/O
33	GP_10_GPIO	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)		I/O
34	GP_09_GPIO	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)		I/O
35	GP_16_I2C_SCL	I2C_SCL		I/O
36	GP_15_SSP0_CLK	SPI0_Clock		O
37	PD_14_SSP0_CS	SPI0_Chip Enable(active low)		O
38	PD_13_SSP0_MOSI	SPI0_Master out slave in		O
39	PD_12_SSP0_MISO	SPI0_Master in Slave out		I
40	RESET	Reset (active high)		I
41	GND	GROUND		GND
42	JTAG_TRSTN	JTAG reset		I
43	JTAG_TMS	JTAG mode selection		I
44	JTAG_TCK	JTAG clock		I
45	JTAG_TDI	JTAG data input		O
46	JTAG_TDO	JTAG data output		I
47	GND	GROUND		GND
48	GND	GROUND		GND
49	RF_ANT	RF IN/OUT		I/O

50	GND	GROUND		GND
51	VDDIO	I/O supply Input		Power
52	GND	GROUND		GND
53	GND	GROUND		GND
54	AUXADCIN3	AUXADC input 3		I
55	AUXADCIN2	AUXADC input 2		I
56	AUXADCIN1	AUXADC input 1		I
57	GND	GROUND		GND
58	NC	No Connection		
59	NC	No Connection		
60	GND	GROUND		GND
61	GND	GROUND		GND
62	GND	GROUND		GND
63	GND	GROUND		GND
64	GND	GROUND		GND
65	GND	GROUND		GND
66	GND	GROUND		GND
67	GND	GROUND		GND
68	GND	GROUND		GND
69	GND	GROUND		GND
70	GND	GROUND		GND
71	GND	GROUND		GND
72	GND	GROUND		GND
73	GND	GROUND		GND
74	GND	GROUND		GND

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_FEM	Front End Module power input	-0.5	-	5.25	V
VBAT	3.3V power supply	-0.5		3.8	
VDDIO	I/O supply Input	-0.5		3.8	
T_{stg}	Storage temperature	TBD	TBD	TBD	℃

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_FEM	Front End Module power input	3.8	4.0	4.2	V
VBAT	3.3V power supply	2.8	3.3	3.6	V
VDDIO	3.3V I/O supply Input	3.0	3.3	VBAT	V
VDDIO	1.8V I/O supply Input	1.62	1.8	1.98	V
$T_{AMBIENT}$	Ambient temperature	TBD	TBD	TBD	℃

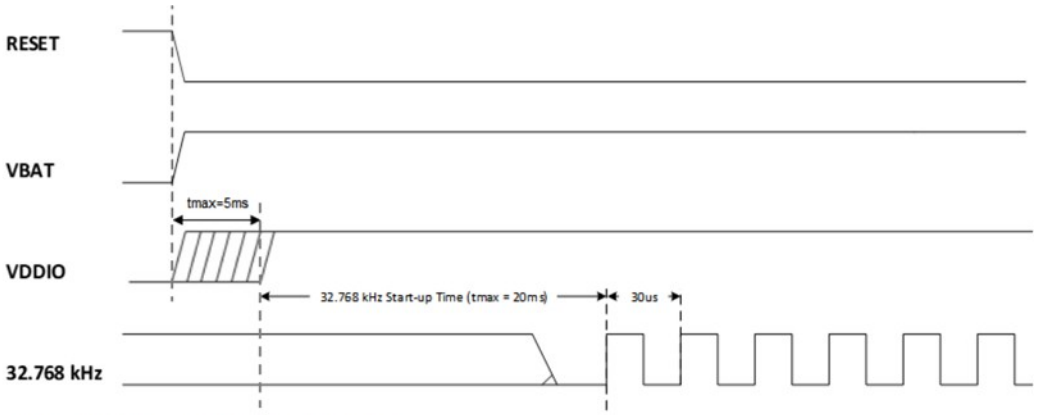
3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	2	-	3.6	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{OH}	Output high voltage	2.4	-		V
V_{OL}	Output low voltage		-	0.4	V

3.4 Timing Sequence

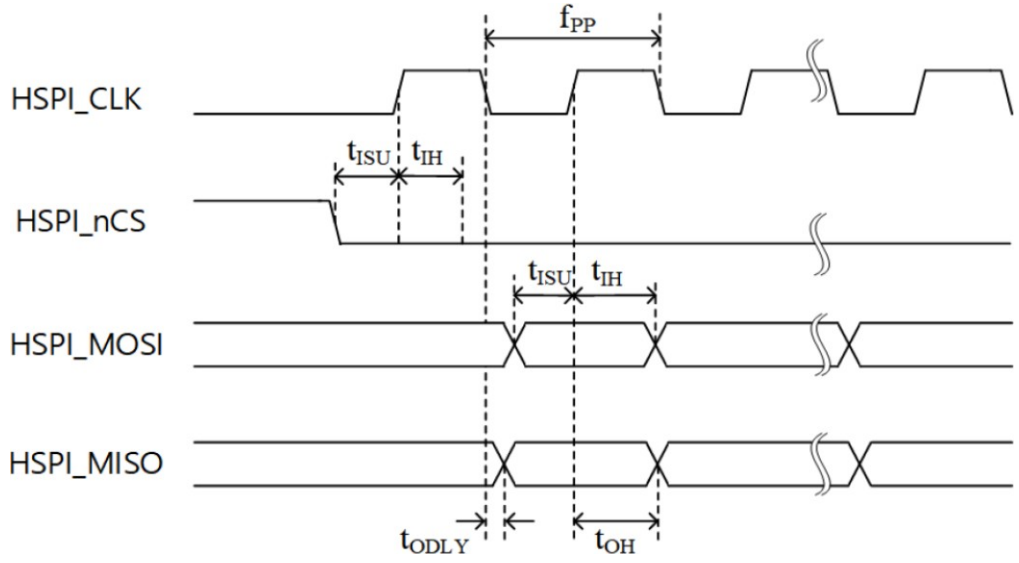
3.4.1 Power on sequence

The figure below shows the module power on sequence.



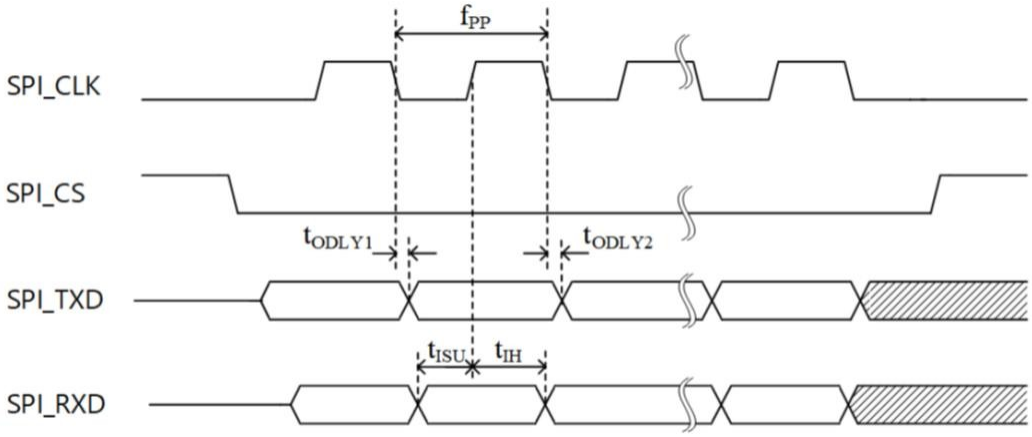
- ✓ Note : VDD_FEM power up is indepent of VBAT
- ✓ Recommended to supply VBAT, VDDIO and VDD_FEM in sequence, or to supply 3 powers at the same time.

3.4.2 HSPI Timing



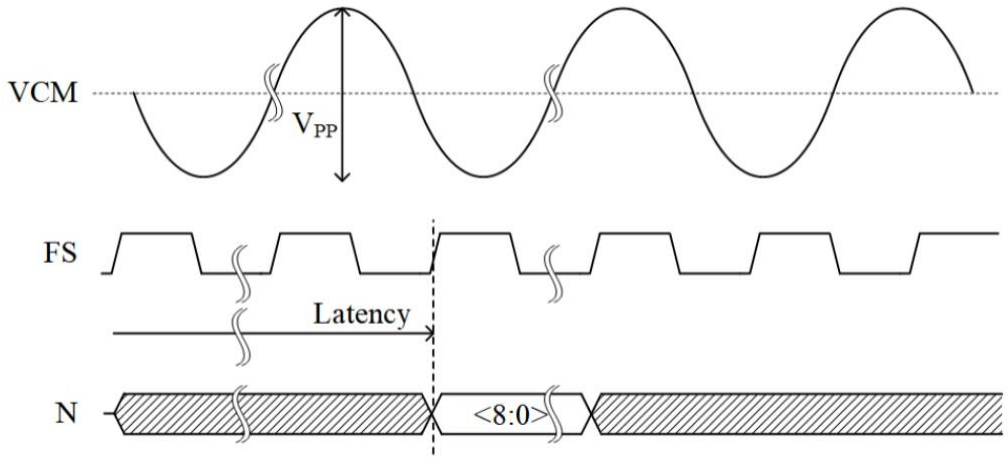
Symbol	Parameter	Min	Typ	Max	Unit
f_{PP}	Frequency	-	-	25	MHz
t_{ODLY}	Output delay time	6	-	-	ns
t_{OH}	Output hold time	2	-	-	ns
t_{ISU}	Input setup time	14	-	-	ns
t_{IH}	Input hold time	2.5	-	-	ns

3.4.3 SPI Timing



Symbol	Parameter		Min	Typ	Max	Unit
f_{PP}	Frequency	master	-	-	24	MHz
		slave	-	-	4	MHz
t_{ODLY1}	Output delay time1		0	-	10	ns
t_{ODLY2}	Output delay time2		0	-	10	ns
t_{ISU}	Input setup time		18	-	-	ns
t_{IH}	Input hold time		20	-	-	ns

3.4.4 AUXADC Timing



Symbol	Parameter	Min	Typ	Max	Unit
VCM	Input common-mode voltage	0.25	0.28	0.31	V
V_{PP}	Input Swing	-	0.5	-	Vpp
FS	Sampling Clock	-	32	-	MHz
Latency	Conversion latency (1 cycle = 31.25 ns)	-	11	-	cycle
N	Resolution	-	9	-	Bit
RIN	Input impedance	-	1	-	Mohms
I_active	Current consumption (1.2V supply)	-	-	300	uA
I_down	Power-down current (1.2V supply)	-	-	1	uA

3.5 Power Consumption

3.5.1 Transmit Power Consumption

Band (MHz)	Modulation	BW (MHz)	DUT Condition	VBAT = 3.3V, VDD_FEM = 4.0V			
				VBAT (mA)		VDD_FEM (mA)	
				Max.	Avg.	Max.	Avg.
915	MCS0	1	Tx @ 22 dBm	36	33	260	228
		2		36	33	260	227
		4		37	34	260	230
	MCS7	1	Tx @ 19 dBm	38	35	200	182
		2		38	35	200	177
		4		38	35	200	168
	MCS10	1	Tx @ 22 dBm	36	33	260	232

* The power consumption is based on AzureWave test environment, these data for reference only.

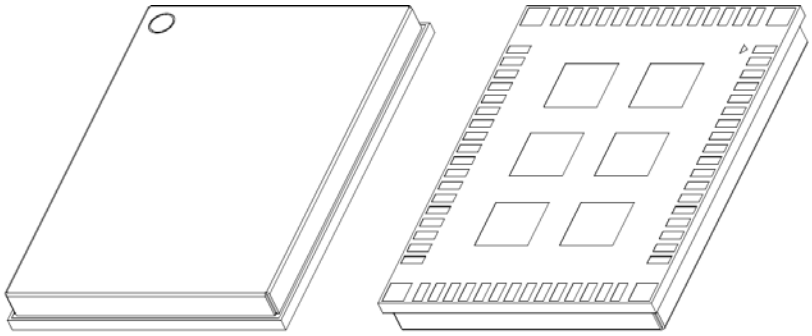
3.5.2 Receive Power Consumption

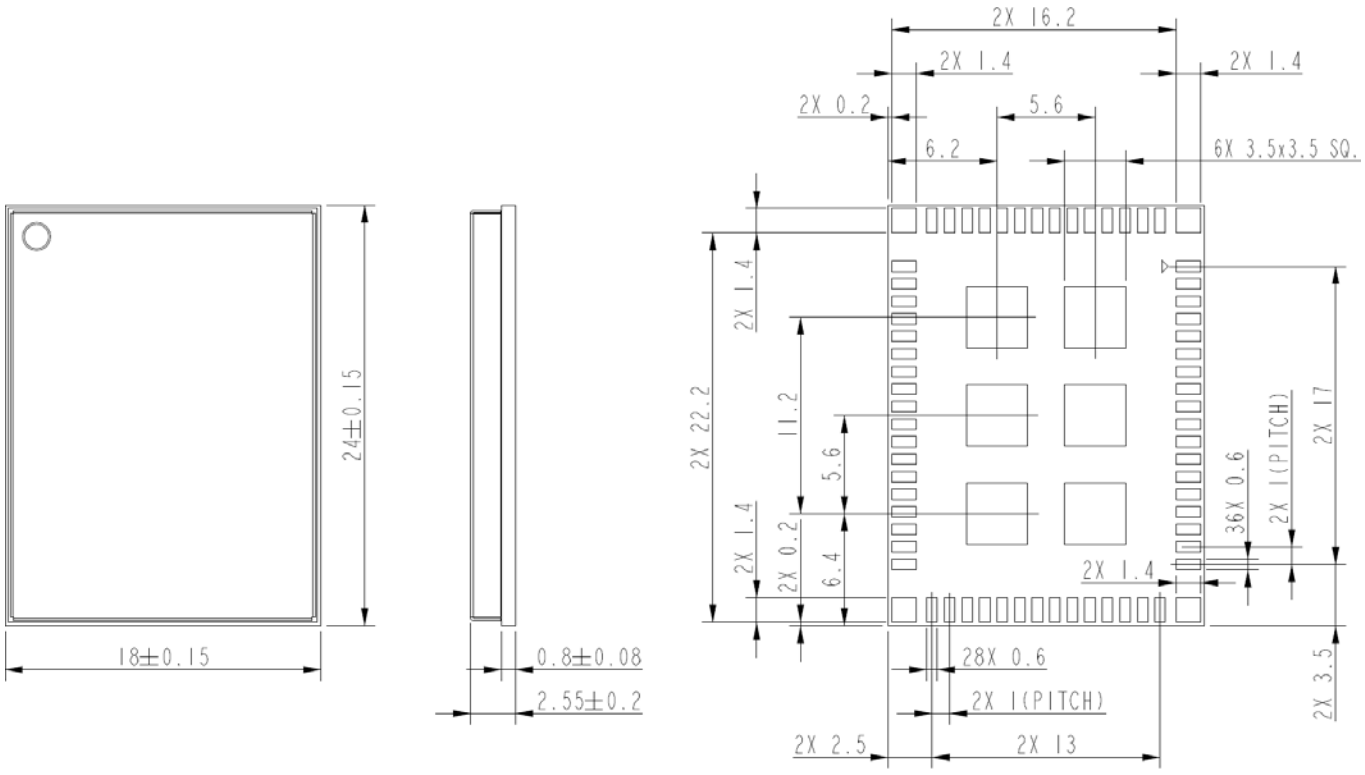
Band (MHz)	Modulation	BW (MHz)	DUT Condition	VBAT = 3.3V, VDD_FEM = 4.0V			
				VBAT (mA)		VDD_FEM (mA)	
				Max.	Avg.	Max.	Avg.
915	MCS0	1	Continuous Rx @ -80 dBm	36	33	8	7
		2	Continuous Rx @ -80 dBm	36	33	8	7
		4	Continuous Rx @ -80 dBm	36	34	8	7
	MCS7	1	Continuous Rx @ -80 dBm	36	33	8	7
		2	Continuous Rx @ -80 dBm	36	33	8	7
		4	Continuous Rx @ -80 dBm	36	34	8	7
	MCS10	1	Continuous Rx @ -80 dBm	36	33	8	7

* The power consumption is based on AzureWave test environment, these data for reference only.

4. Mechanical Information

4.1 Mechanical Drawing





TOLERANCES UNLESS OTHERWISE SPECIFIED:±0.1mm

5. Package information

TBD

AzureWave Technologies, Inc.

Layout Guide

Rev. 0.1

(For Standard)

Revision History

Document NO:

Version	Revision Date	DCN NO.	Description	Initials	Approved
0.1	2021/2/22		● Initial Version	Daniel Lee	NC Chen

Table of Contents

1 Overview

1.1 Device supported

This document provides key guidelines and recommendations to be followed when creating AW-HM482 (18 x 24 mm LGA Module) layout. It is strongly recommended that layouts be reviewed by the AzureWave engineering team before being released for fabrication.

The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

2 GENERAL RF GUIDELINES

Follow these steps for optimal WLAN performance.

1. Control WLAN 50 ohm RF traces by doing the following:
   - Route traces on the top layer as much as possible and use a continuous reference ground plane underneath them.
   - Verify trace distance from ground flooding. At a minimum, there should be a gap equal to the width of one trace between the trace and ground flooding. Also keep RF signal lines away from metal shields. This will ensure that the shield does not detune the signals or allow for spurious signals to be coupled in.
   - Keep all trace routing inside the ground plane area by at least the width of a trace.
   - Check for RF trace stubs, particularly when bypassing a circuit.

2. Keep RF traces properly isolated by doing the following:
   - Do not route any digital or analog signal traces between the RF traces and the reference ground.
   - Keep the pins and traces associated with RF inputs away from RF outputs. If two RF traces are close each other, then make sure there is enough room between them to provide isolation with ground fill.
   - Verify that there are plenty of ground vias in the shield attachment area. Also verify that there are no non-ground vias in the shield attachment area. Avoid traces crossing into the shield area on the shield layer.

3. Consider the following RF design practices:
   - Verify that the RF path is short, smooth, and neat. Use curved traces for all turns; never use 90-degree turns. Avoid width discontinuities over pads. If trace widths differ significantly from component pad widths, then the width change should be mitered. Verify there are no stubs.
   - Do not use thermals on RF traces because of their high loss.
   - The RF traces between AW-HM482 RF_ANT pin and antenna must be made using 50Ω controlled-impedance transmission line.

3 Ground Layout

Please follow general ground layout guidelines. Here are some general rules for customers' reference.

- The layer 2 of PCB should be a complete ground plane. The rule has to be obeyed strictly in the RF section while RF traces are on the top layer.
- Each ground pad of components on top layer should have via drilled to PCB layer 2 and via should be as close to pad as possible. A bulk decoupling capacitor needs two or more.
- Don't place ground plane and route signal trace below printed antenna or chip antenna to avoid destroying its electromagnetic field, and there is no organic coating on printed antenna. Check antenna chip vendor for the layout guideline and clearance.
- Move GND vias close to the pads.

4 Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

- A 10uF capacitor is used to decouple high frequency noise at digital and RF power terminals. This capacitor should be placed as close to power terminals as possible.
- In order to reduce PCB's parasitic effects, placing more via on ground plane is better.

5 Digital Interface

Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

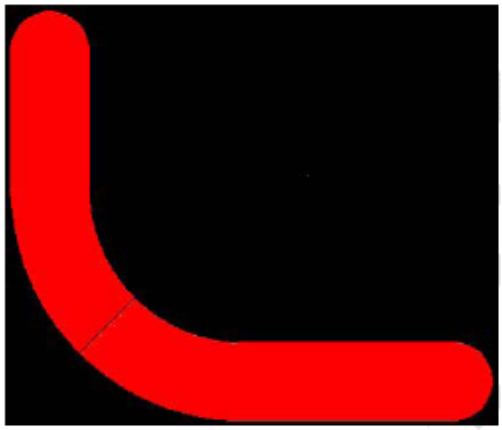
- The digital interface to the module must be routed using good engineering practices to minimize coupling to power planes and other digital signals.
- The digital interface must be isolated from RF trace.

6 RF Trace

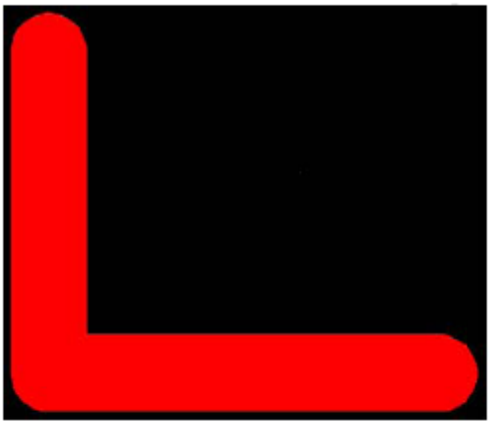
The RF trace is the critical to route. Here are some general rules for customers' reference.

- The RF trace impedance should be 50Ω between ANT port and antenna matching network.
- The length of the RF trace should be minimized.
- To reduce the signal loss, RF trace should laid on the top of PCB and avoid any via on it.
- The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.
- The RF trace must be isolated with aground beneath it. Other signal traces should be isolated from the RF trace either by ground plane or ground vias to avoid coupling.
- To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

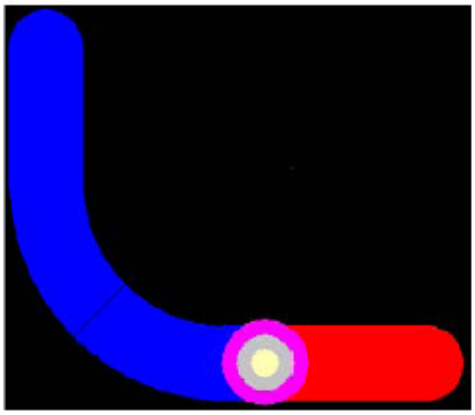
If the customers have any problem in calculation of trace impedance, please contact AzureWave.



Correct RF trace



Right-angled corner



Via on RF trace

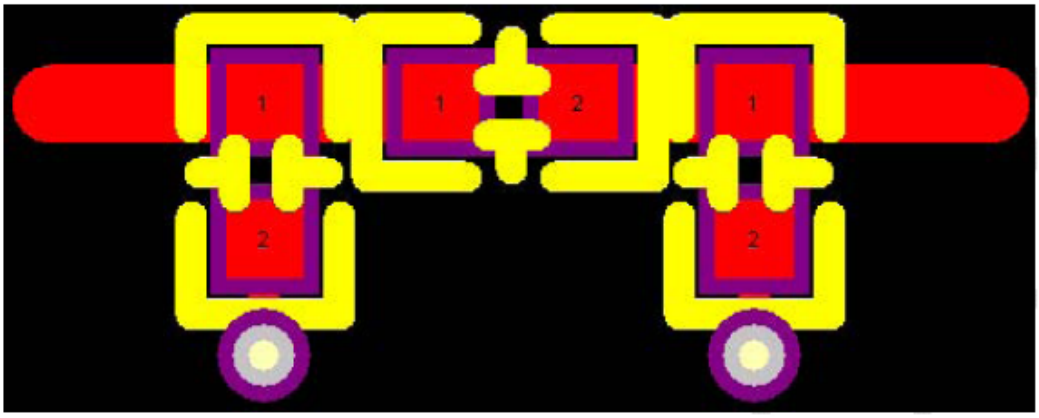
Incorrect RF trace

7 Antenna

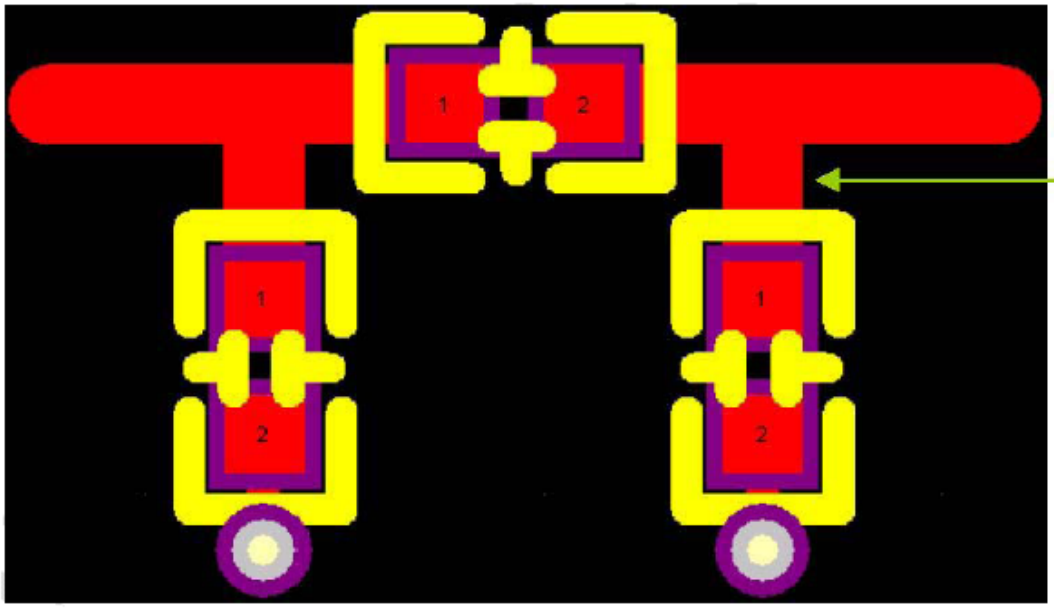
All the high-speed traces should be moved far away from the antenna. For the best radiation performance, check antenna chip vendor for the layout guideline and clearance.

8 Antenna Matching

PCB designer should reserve an antenna matching network for post tuning to ensure the antenna performance in different environments. Matching components should be close to each other. Stubs should also be avoided to reduce parasitic while no shunt component is necessary after tuning.



Correct layout for antenna matching



It will be a stub if a shunt component is not necessary.

Incorrent layut for antenna matching

9 SHIELDING CASE

Magnetic shielding, ferrite drum shielding, or magnetic-resin coated shielding is highly recommended to prevent EMI issues.

10 GENERAL LAYOUT GUIDELINES

Follow these guidelines to obtain good signal integrity and avoid EMI:

1. Place components and route signals using the following design practices:
   - Keep analog and digital circuits in separate areas.
   - Orient adjacent-layer traces so that they are perpendicular to one another to reduce crosstalk.
   - Keep critical traces on internal layers, where possible, to reduce emissions and improve immunity to external noise. However, RF traces should be routed on outside layers to avoid the use of vias on these traces.
   - Keep all trace lengths to a practical minimum. Keep traces, especially RF traces, straight wherever possible. Where turns are necessary, use curved traces or two 45-degree turns. Never use 90-degree turns.
2. Consider the following with respect to ground and power supply planes:
   - Route all supply voltages to minimize capacitive coupling to other supplies. Capacitive coupling can occur if supply traces on adjacent layers overlap. Supplies should be separated from each other in the stack-up by a ground plane, or they should be coplanar (routed on different areas of the same layer).
   - Provide an effective ground plane. Keep ground impedance as low as possible. Provide as much ground plane as possible and avoid discontinuities. Use as many ground vias as possible to connect all ground layers together.
   - Maximize the width of power traces. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.
3. Consider these power supply decoupling practices:
   - Place decoupling capacitors near target power pins. If possible, keep them on the same side as the IC they decouple to avoid vias that add inductance.
   - Use appropriate capacitance values for the target circuit.

11 The other layout guide Information

- High speed interface (i.e. UART/SPI) shall have equal electrical length. Keep them away from noise sensitive blocks.
- Good power integrity of VDDIO will improve the signal integrity of digital interfaces.
- Good return path and well shielded signal can reduce crosstalk, EMI emission and improve signal integrity.
- RF IO is around 50 ohms, reserve Pi or T matching network to have better signal transition from port to port.
- Smooth RF trace help to reduce insertion loss. Do not use 90 degrees turn (use two 45 degrees turns or one miter bend instead).
- Discuss with AzureWave Engineer after you finish schematic and layout job.

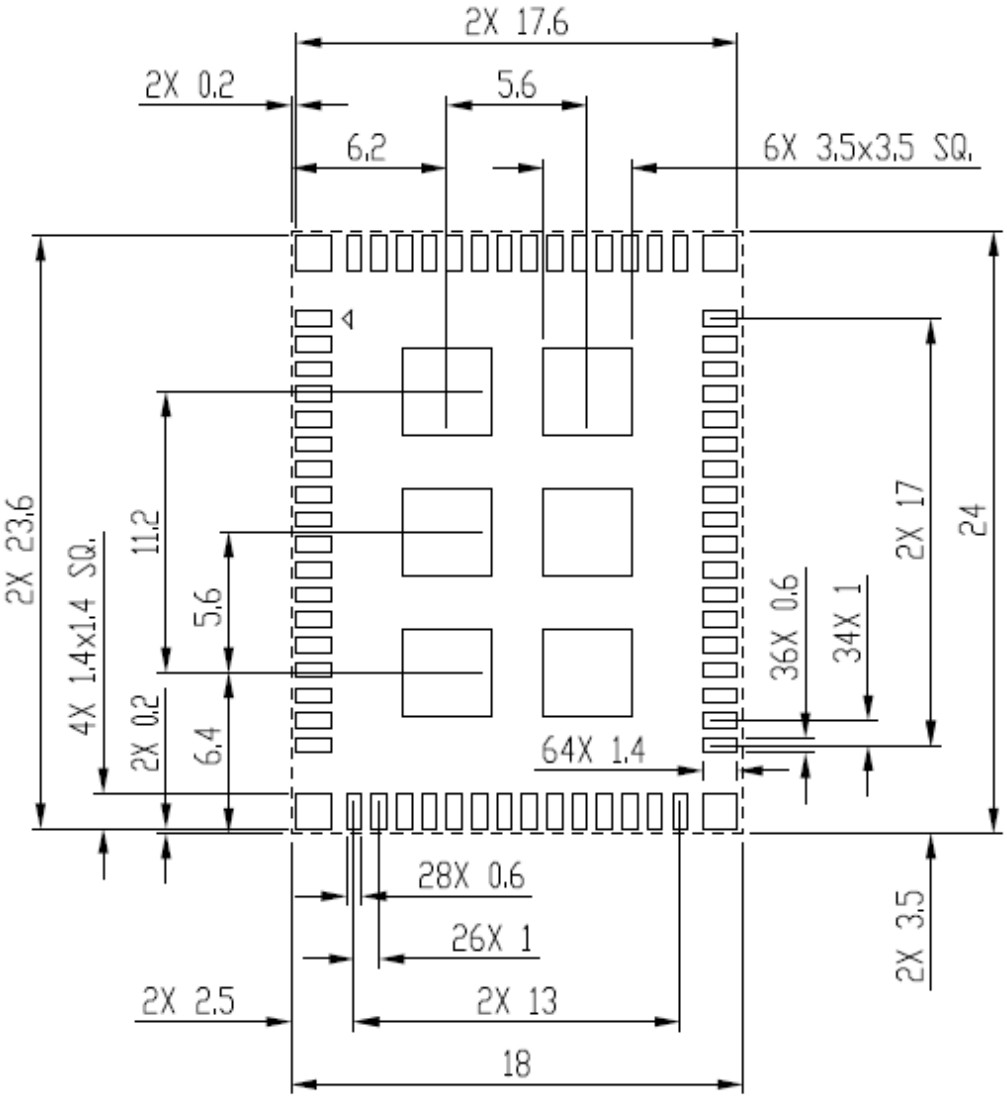
12 LGA module layout footprint recommend

12.1 LGA Module stencil and Pad opening Suggestion

- Stencil thickness：0.1~0.12mm
- Function Pad opening size suggestion: Max. 1:1

PS: This opening suggestion just for customer reference, please discuss with AzureWave's Engineer before you start SMT.

- 18x24mm Solder Printer Opening Reference:



RECOMMENDED PCB LAYOUT (TOP VIEW)

FCC Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This device and its antenna(s) must not be co-located or operating in conjunction with any other antenna or transmitter.

FCC Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

ISED Statement

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:

1. This device may not cause interference.
2. This device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1. L'appareil ne doit pas produire de brouillage;
2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

IC Radiation Exposure Statement:

This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20cm de distance entre la source de rayonnement et votre corps.

This module is intended for OEM integrators under the following conditions:

1. Ensure that the end-user has no manual instructions to remove or install module.
2. This module is certified pursuant to Part 15 rules section 15.247 and RSS-247.
3. This module has been approved to operate with the antenna types listed below, with the maximum permissible gain indicated.

Frequency Band	Antenna Type	Brand	Model Number	Gain(dBi)
902-928MHz	Dipole	Cortec	AN0915-5001BSM	2

4. Label and compliance information

Label of the end product:

FCC

The host product must be labeled in a visible area with the following " Contains FCC ID: TLZ-HM482".
The end product shall bear the following 15.19 statement: This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

ISED

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 6100A-HM482”.
Contient le module d'émission IC: 6100A-HM482

5. Information on test modes and additional testing requirements

This module has been approved under stand-alone configuration.
The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093/RSS-102 and different antenna configurations
The information on how to configure test modes for host product evaluation for different operational conditions for a stand-alone modular transmitter in a host, versus with multiple, simultaneously transmitting modules or other transmitters in a host can be found at KDB Publication 996369 D04.
OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).
IMPORTANT NOTE: In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/ISED authorization is no longer considered valid and the FCC/IC No. cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/ISED authorization.

6. Additional testing, Part 15 Subpart B and ICES-003 disclaimer

Appropriate measurements (e.g. Part 15 Subpart B compliance) and if applicable additional equipment authorizations (e.g. SDoC) of the host product to be addressed by the integrator/manufacturer.
This module is only FCC/ISED authorized for the specific rule parts 15.247/RSS-247 listed on the grant, and the host product manufacturer is responsible for compliance to any other FCC/ISED rules that apply to the host product as being Part 15 Subpart B/ICES-003 compliant.

7. The user manual of the end product should include:

FCC:

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
The antenna(s) used for this transmitter must not transmit simultaneously with any other antenna or transmitter.

ISED:

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada’s licence-exempt RSS(s). Operation is subject to the following two conditions:
1. This device may not cause interference.
2. This device must accept any interference, including interference that may cause undesired operation of the device.
L’émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d’Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L’exploitation est autorisée aux deux conditions suivantes :
1. L’appareil ne doit pas produire de brouillage;
2. L’appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d’en

compromettre le fonctionnement.
ISED Radiation Exposure Statement:
This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.
Cet équipement est conforme aux limites d’exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20cm de distance entre la source de rayonnement et votre corps.
The transmitter module may not be co-located with any other transmitter or antenna.
Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.