AzureWave Technologies, Inc.

AW-CM467-SUR-I

IEEE 802.11 a/b/g/n/ac and Bluetooth 5.0 Module

Datasheet

Rev. B

DF

(For Standard)

Features

Wi-Fi

- Dual band 802.11 a/b/g/n/ac
- Single-stream spatial multiplexing up to 433.3 Mbps
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Security: WEP, WPA/WPA2 (personal), AES (HW), TKIP (HW), CKIP (software support)

Bluetooth

- Qualified for Bluetooth Core Specification 5.0 with all Bluetooth 4.2 optional features
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.

AzureWave Technologies, Inc.

Revision History

Document NO: R2-2467-DST-03

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2021/02/18	DCN020945	● Initial Version	JM.Pang	Chihhao Liao
A	2021/08/18		● 1.3 Specifications Table update	JM.Pang	Chihhao Liao

AzureWave Technologies, Inc.

Table of Contents

1. Introduction

1.1 Product Overview

The Cypress AW-CM467-SUR-I device provides the highest level of integration for embedded and IoT wireless systems with integrated single-stream IEEE 802.11a/b/g/n/ac, MAC/baseband/radio and Bluetooth 5.0 (Basic Rate, Enhanced Data Rate and Bluetooth Low Energy).

AW-CM467-SUR-I supports all rates specified in the IEEE 802.11 a/b/g/n/ac specifications. IEEE 802.11ac's 256-QAM is supported for MCS8 in 20 MHz channels and MCS8/MCS9 in 40 MHz & 80 MHz channels to enable data rates of up to 433.3 Mbps. Included on-chip are 2.4 GHz and 5 GHz power amplifiers and low-noise amplifiers.

The WLAN section supports the following host interface options: an SDIO v3.0 interface that can operate in 4b or 1b mode and a USB 2.0 interface. The Bluetooth section supports USB 2.0, USB 1.1, SDIO and a high-speed 4-wire UART interface. An on-chip USB 2.0 hub provides a shared single USB connection to both WLAN and Bluetooth target devices.

Using advanced design techniques and process technology to reduce active and idle power, the AW-CM467-SUR-I is designed to address the need of mobile devices that require minimal power consumption and compact size. It includes a power management unit (PMU) which simplifies the system power topology and allows for direct operation from a mobile platform battery while maximizing battery life.

The AW-CM467-SUR-I implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms, which ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on an embedded and IoT system is achieved.

1.2 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac Wireless LAN and Bluetooth Module
Major Chipset	Cypress CYW4373E
Host Interface	WiFi + BT ● SDIO + UART *For Host configuration interface, please refer to section 2.3
Dimension	12mm(L) x 12mm(W) x 1.65mm(T)
Form Factor	LGA module, 47 pins
Antenna	1T1R ANT1(Main)：WiFi/Bluetooth → TX/RX
Weight	TBD

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac 1T1R
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Rage	WLAN: 2.4 GHz / 5GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9)
Number of Channels	802.11b: USA, Canada and Taiwan – 1 ~ 11 Most European Countries – 1 ~ 13 Japan – 1 ~ 13 802.11g:

<table>
<tr><td></td><td>USA and Canada – 1 ~ 11
Most European Countries – 1 ~ 13
802.11n:
USA and Canada – 1 ~ 11
Most European Countries – 1 ~ 13
802.11a:
USA – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165</td></tr>
<tr><td>Output Power[1]</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps)
@EVM<35%</td><td>15</td><td>17</td><td>19</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)
@EVM≦-25 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-27 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps)
@EVM≦-25 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-27 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)
@EVM≦-27 dB</td><td>10</td><td>12</td><td>14</td><td>dBm</td></tr>
<tr><td>11ac (VHT20 MCS8)
@EVM≦-30 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
<tr><td>11ac (VHT40 MCS9)
@EVM≦-32 dB</td><td>7</td><td>9</td><td>11</td><td>dBm</td></tr>
<tr><td>11ac (VHT80 MCS9)
@EVM≦-32 dB</td><td>6</td><td>8</td><td>10</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity[1]</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps)</td><td></td><td>-87</td><td>-84</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td></td><td>-73</td><td>-70</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td></td><td>-73</td><td>-70</td><td>dBm</td></tr>
</table>
5G(n/ac packets with LDPC)
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps)</td><td></td><td>-72</td><td>-69</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td></td><td>-70</td><td>-67</td><td>dBm</td></tr>
</table></td></tr>
</table>

	11n (HT40 MCS7)		-68	-65	dBm
	11ac (VHT20 MCS8)		-67	-64	dBm
	11ac (VHT40 MCS9)		-62	-59	dBm
	11ac (VHT80 MCS9)		-59	-56	dBm
Data Rate	802.11b: 1, 2, 5.5, 11Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: MCS0~7 HT20/HT40 802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11ac: MCS0~8 VHT20 802.11ac: MCS0~9 VHT40/VHT80				
Security	● WPA™- and WPA2™- (Personal) support for powerful encryption and authentication ● AES and TKIP acceleration hardware for faster data encryption and 802.11i compatibility ● Wi-Fi Protected Setup (WPS) ● WEP ● CKIP(Software) ● WPA3				

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

Features	**Description**
Bluetooth Standard	Bluetooth 2.1+Enhanced Data Rate (EDR)/BT3.0/BT4.2/BT5.0
Bluetooth VID/PID	N/A
Frequency Rage	2400~2483.5MHz
Modulation	GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)
Output Power[1]	Min / Typ / Max / Unit Basic rate: 6 / 8 / 10 / dBm LE: 6 / 8 / 10 / dBm
Receiver Sensitivity[1]	Min / Typ / Max / Unit DH5: -84 / -81 / dBm 2DH5: -84 / -81 / dBm 3DH5: -76 / -73 / dBm LE: -86 / -83 / dBm

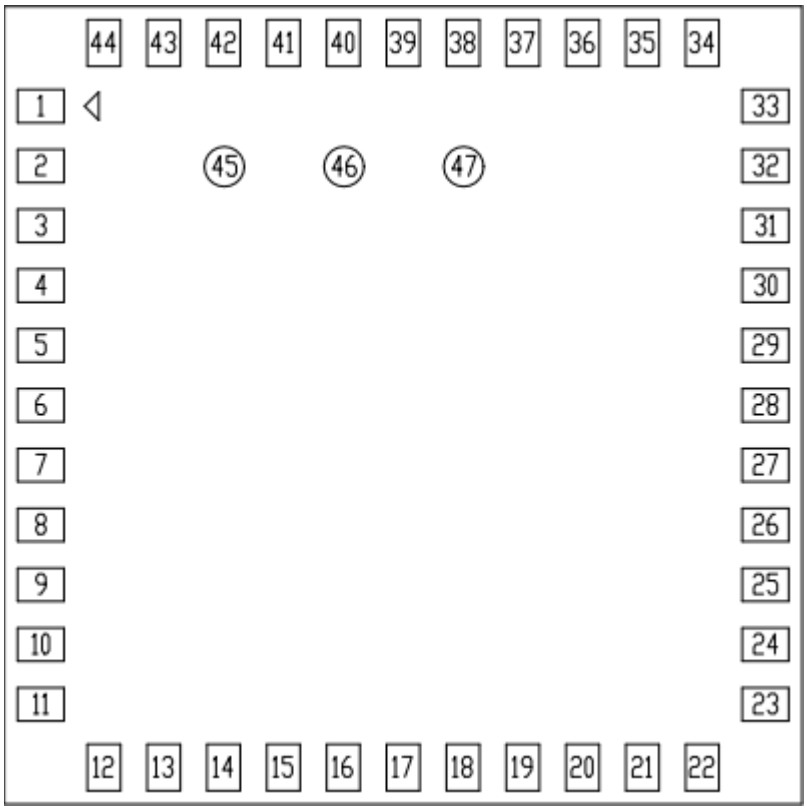
[1] Note: this product is under development, and the RF performance is still being fine-tuned, so the relevant values may be subject to change without any notice

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.2 V– 4.8 V
Operating Temperature	-40°C ~85°C
Operating Humidity	less than 85% R.H.
Storage Temperature	-40°C ~125°C
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	TBD
Changed Device Model	TBD

2. Pin Definition

2.1 Pin Map



AW-CM467-SUR-I Top View Pin Map

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND	Ground.		GND
2	WL_BT_ANT	WLAN/BT RF TX/RX path.		RF
3	GND	Ground.		GND
4	NC	Floating Pin, No connect to anything.		Floating
5	NC	Floating Pin, No connect to anything.		Floating
6	BT_DEV_WAKE	Bluetooth DEV_WAKE.	VDDIO	I/O
7	BT_HOST_WAKE	Bluetooth HOST_WAKE.	VDDIO	I/O
8	NC	Floating Pin, No connect to anything		Floating
9	VBAT	3.3V power pin	3.3V	VCC
10	NC	Floating Pin, No connect to anything.		Floating
11	NC	Floating Pin, No connect to anything.		Floating
12	WL_REG_ON	Used by PMU to power-up or power down the internal CYW4373E regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.	VDDIO	I
13	WL_HOST_WAKE	WL Host Wake.	VDDIO	O
14	SDIO_DATA2	SDIO Data Line 2.	VDDIO	I/O
15	SDIO_DATA3	SDIO Data Line 3.	VDDIO	I/O
16	SDIO_DATA_CMD	SDIO Command Input.	VDDIO	I/O
17	SDIO_DATA_CLK	SDIO Clock Input.	VDDIO	I
18	SDIO_DATA0	SDIO Data Line 0.	VDDIO	I/O
19	SDIO_DATA1	SDIO Data Line 1.	VDDIO	I/O
20	GND	Ground.		GND
21	VIN_LDO_OUT	Internal Buck 1.2V voltage generation pin.	1.4V	O

22	VDDIO	VDDIO supply for WLAN and BT.	1.8V/3.3V	VCC
23	VIN_LDO	Internal Buck 1.2V voltage generation pin.	1.4V	I
24	LPO	External 32K or RTC clock.	0.2~3.3V	I
25	BT_PCM_OUT	PCM data output.	VDDIO	O
26	BT_PCM_CLK	PCM clock; can be master (output) or slave (input).	VDDIO	I/O
27	BT_PCM_IN	PCM data input.	VDDIO	I
28	BT_PCM_SYNC	PCM sync; can be master (output) or slave (input), or SLIMbus data.	VDDIO	I/O
29	STRAP_0	SDIO_PADVDDIO sel	Follow host configuration interface	I
30	NC	Floating Pin, No connect to anything.		Floating
31	GND	Ground.		GND
32	NC	Floating Pin, No connect to anything.		Floating
33	GND	Ground.		GND
34	BT_REG_ON	Used by PMU to power-up or power down the internal CYW4373E regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.	VDDIO	I
35	NC	Floating Pin, No connect to anything.		Floating
36	GND	Ground.		GND
37	NC	Floating Pin, No connect to anything.		Floating
38	NC	Floating Pin, No connect to anything.		Floating
39	RF_SW_CTRL5	Programmable RF switch control lines	3.3V	O
40	NC	Floating Pin, No connect to anything.		Floating
41	BT_UART_RTS	UART request-to-send. Active-low request-to-send signal for the HCI UART interface.	VDDIO	O
42	BT_UART_TXD	UART serial output. Serial data output for the HCI UART interface.	VDDIO	O
43	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.	VDDIO	I
44	BT_UART_CTS	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	VDDIO	I

45	NC	Floating Pin, No connect to anything.		Floating
46	NC	Floating Pin, No connect to anything.		Floating
47	NC	Floating Pin, No connect to anything.		Floating

2.3 Host Configuration Interface Table

Scenario	WLAN	BT	Strap_0 Value
1	SDIO(1.8V)	UART	1
2	SDIO(3.3V)	UART	0

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the VBAT and PA driver supply	-0.5	-	5.5	V
VDDIO	DC supply voltage for digital I/O	-0.5	-	3.9	V
Tj	Maximum junction temperature	-	-	125	°C

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulator	3.2	3.6	4.8	V
VDDIO	DC supply voltage for digital I/O	1.62	1.8/3.3	3.63	V

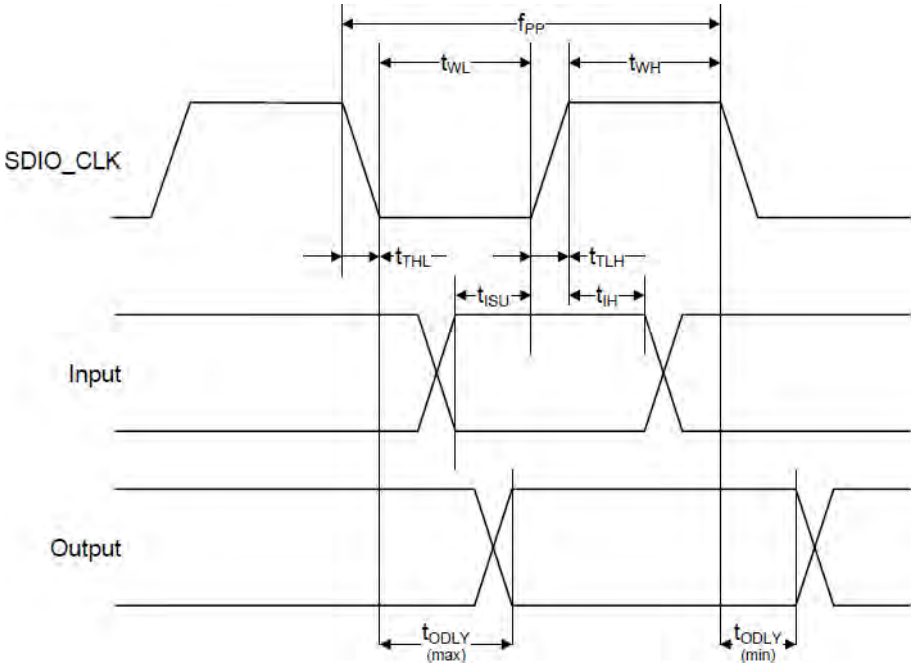
3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Digital I/O pins, VDDIO=1.8V					
V_{IH}	Input high voltage	0.65 × VDDIO	-	-	V
V_{IL}	Input low voltage	-	-	0.35 × VDDIO	V
V_{OH}	Output high voltage	VDDIO – 0.45	-	-	V
V_{OL}	Output Low Voltage	-	-	0.45	V
Digital I/O pins, VDDIO=3.3V					
V_{IH}	Input high voltage	2.00	-	-	V
V_{IL}	Input low voltage	-	-	0.80	V
V_{OH}	Output high voltage	VDDIO – 0.4	-	-	V
V_{OL}	Output low Voltage	-	-	0.40	V

3.4 Host Interface

3.4.1 SDIO Interface

SDIO Bus Timing (Default Mode)

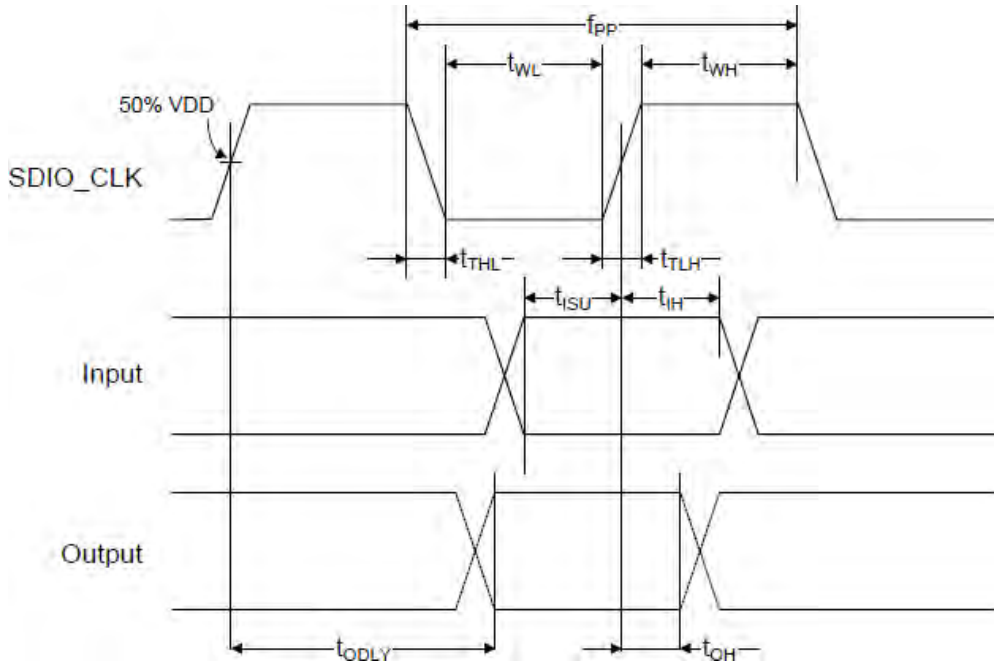


SDIO Bus Timing Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL)					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns

Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

SDIO Bus Timing (High-Speed Mode)



SDIO Bus Timing Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns

Total system capacitance (each line)	CL	–	–	40	pF

3.4.2 UART Interface

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth UART HCI specification: H4 and a custom Extended H4. The default baud rate is 115.2 Kbaud.

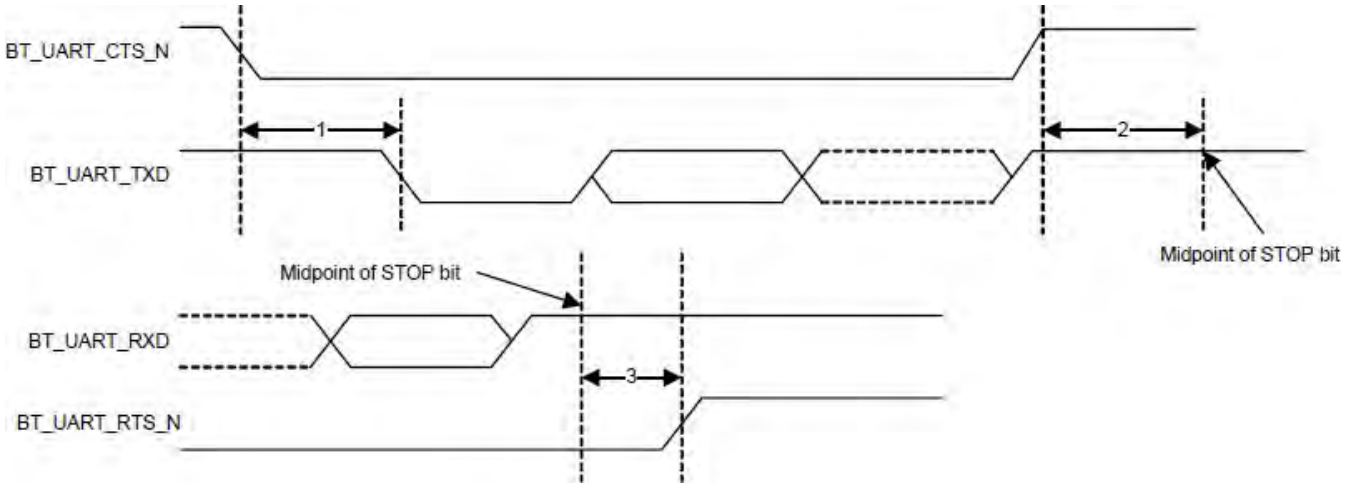
The AW-CM467-SUR-I UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP).

It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-CM467-SUR-I UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

UART Interface Signals

PIN No.	Name	Description	Type
18	BT_UART_TXD	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface	O
19	BT_UART_RXD	Bluetooth UART Series Input. Serial data input for the HCI UART Interface	I
21	BT_UART_RTS_N	Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface	O
17	BT_UART_CTS_N	Bluetooth UART Clear-to-Send. Active-low clear-to-send signal for the HCI UART interface.	I



UART Timing

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

3.5 Power up Timing Sequence

The AW-CM467-SUR-I has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals

- **WL_REG_ON**:

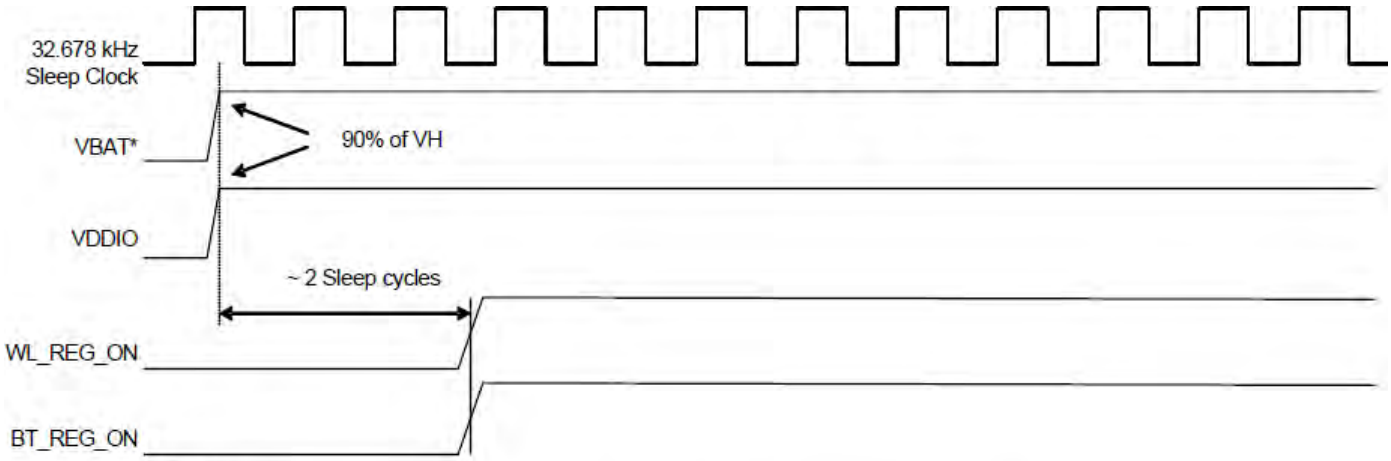
  Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal AW-CM467-SUR-I regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.

- **BT_REG_ON**:

  Used by the PMU (OR-gated with WL_REG_ON) to power up the internal AW-CM467-SUR-I regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

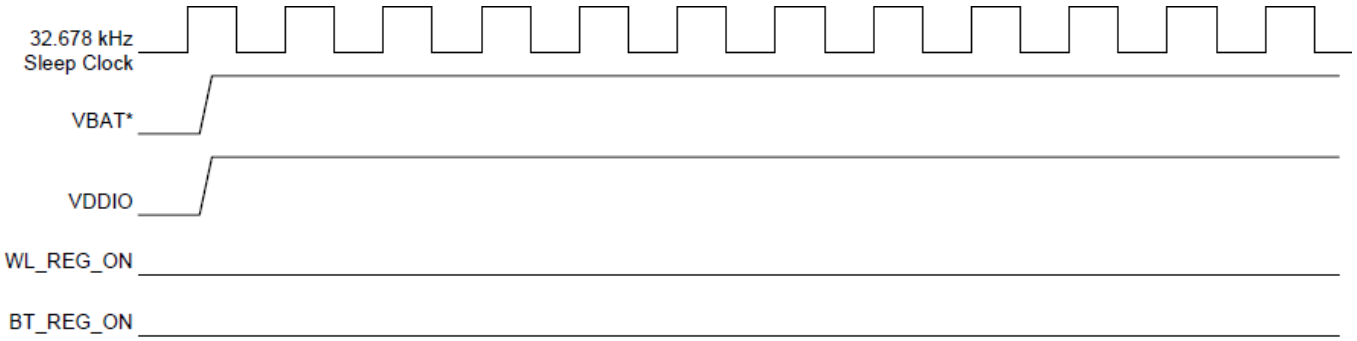
Note:

For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 msec time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.



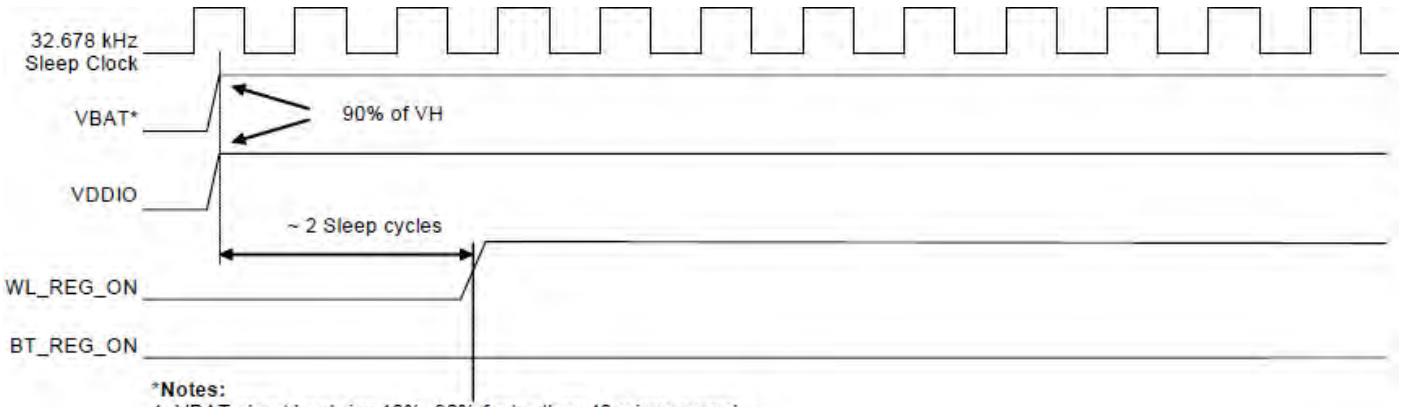
*Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = ON, Bluetooth = ON



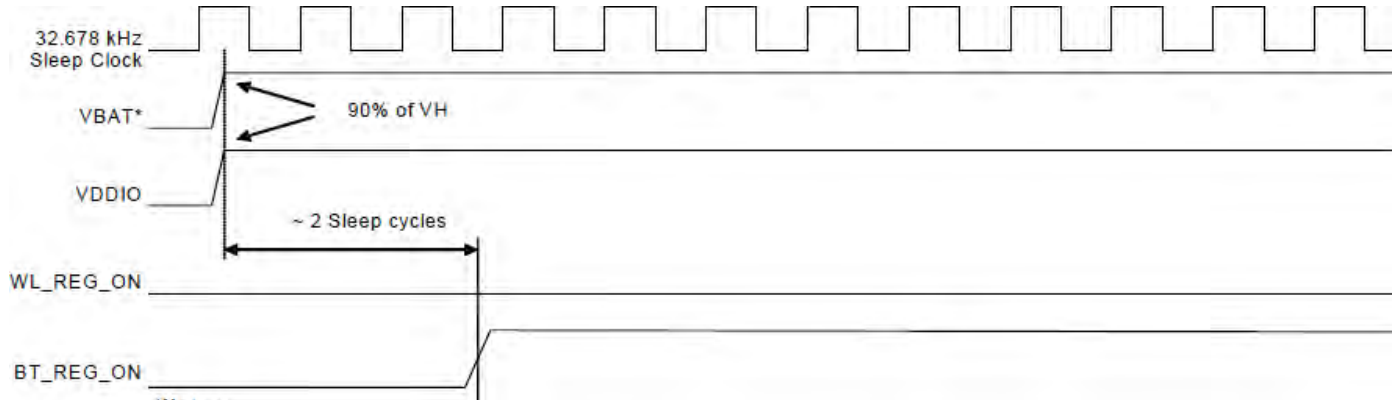
*Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = OFF



*Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = ON, Bluetooth = OFF



*Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = ON

3.6 Power Consumption*

3.6.1 WLAN

TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

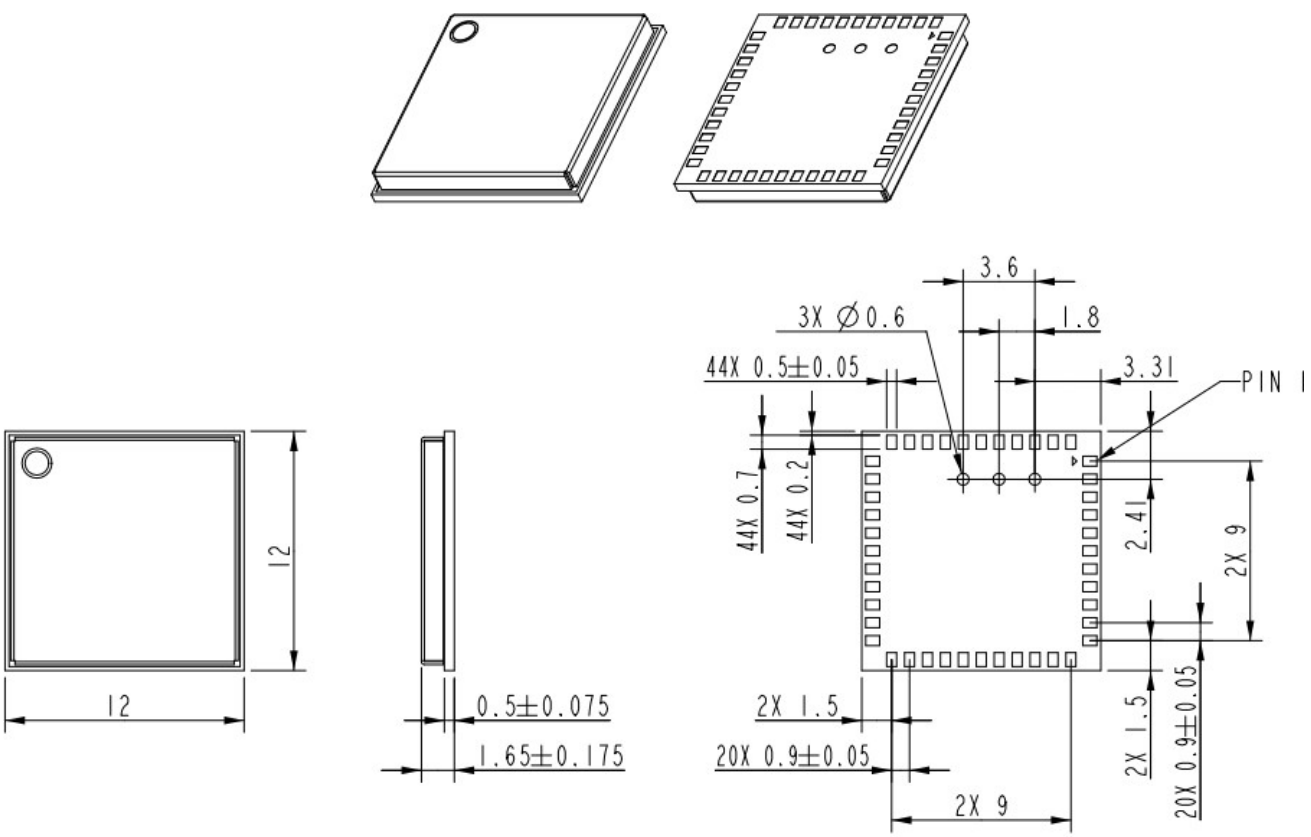
3.6.2 Bluetooth

TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

4. Mechanical Information

4.1 Mechanical Drawing

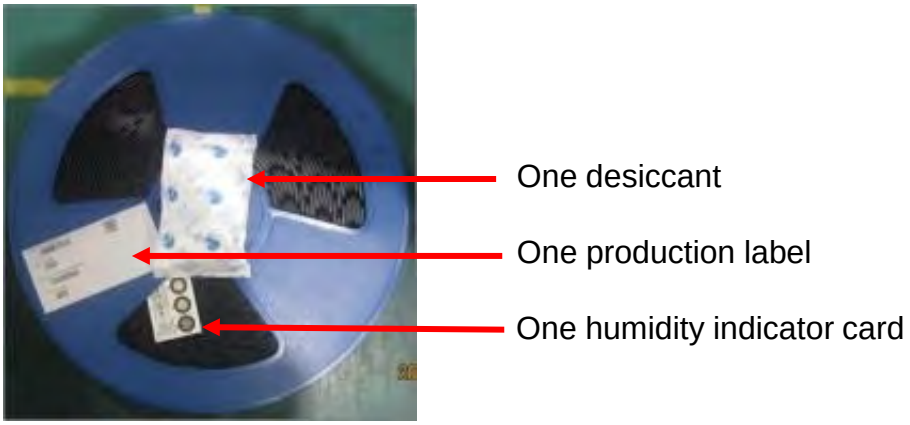


TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

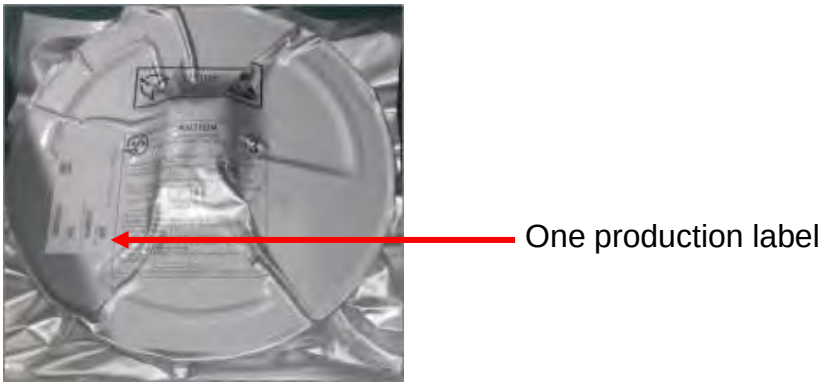
5. Packaging Information

1. One reel can pack 1,500pcs 12x12 LGA modules

2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel



3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag



4. A bag is put into the anti-static pink bubble wrap

5. A bubble wrap is put into the inner box and then one label is pasted on the inner box

One production label

6. **5 inner boxes** could be put into one carton

7. Sealing the carton by AzureWave tape

8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton

Example of carton label	AzureWave P/N: Customer: 由業務提供 Customer P/N: 由業務提供 Customer PO: 由業務提供 Description: AW-XXXXXX QTY: 1200 pcs C/N: N.W. G.W. RoHS COMPLIANT
Example of box label	
Example of production label	

Example of balance label	

Layout Guide

Rev. A

(For Standard)

Revision History

Version	Revision Date	Description	Initials	Approved
A	2021/04/14	● Initial Version	JM.Pang	N.C. Chen
B	2021/09/10	● EVB update	JM.Pang	N.C. Chen

INTRODUCTION

This document provides key guidelines and recommendations to be followed when creating AW-CM467-SUR-I layout. It is strongly recommended that layouts be reviewed by the AzureWave engineering team before being released for fabrication.

The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

- GENERAL RF GUIDELINES
- Ground Layout
- Power Layout
- Digital Interface
- RF Trace
- Antenna
- Antenna Matching
- GENERAL LAYOUT GUIDELINES
- THE OTHER LAYOUT GUIDE INFORMATION

1. GENERAL RF GUIDELINES

Follow these steps for optimal WLAN performance.

1. Control WLAN 50 ohm RF traces by doing the following:

   • Route traces on the top layer as much as possible and use a continuous reference ground plane underneath them.

   • Verify trace distance from ground flooding. At a minimum, there should be a gap equal to the width of one trace between the trace and ground flooding. Also keep RF signal lines away from metal shields. This will ensure that the shield does not detune the signals or allow for spurious signals to be coupled in.

   • Keep all trace routing inside the ground plane area by at least the width of a trace.

   • Check for RF trace stubs, particularly when bypassing a circuit.

2. Keep RF traces properly isolated by doing the following:

   • Do not route any digital or analog signal traces between the RF traces and the reference ground.

   • Keep the balls and traces associated with RF inputs away from RF outputs. If two RF traces are close each other, then make sure there is enough room between them to provide isolation with ground fill.

   • Verify that there are plenty of ground vias in the shield attachment area. Also verify that there are no non-ground vias in the shield attachment area. Avoid traces crossing into the shield area on the shield layer.

3. Consider the following RF design practices:

   • Confirm antenna ground keep-outs.

   • Verify that the RF path is short, smooth, and neat. Use curved traces or microwave corners for all turns; never use 90-degree turns. Avoid width discontinuities over pads. If trace widths differ significantly from component pad widths, then the width change should be mitered. Verify there are no stubs.

   • Do not use thermals on RF traces because of their high loss.

   • The RF traces between AW-CM467-SUR-I WL_BT_ANT pin and antenna must be made using 50Ω controlled-impedance transmission line.

2. Ground Layout

Please follow general ground layout guidelines. Here are some general rules for customers' reference.

- The layer 2 of PCB should be a complete ground plane. The rule has to be obeyed strictly in the RF section while RF traces are on the top layer.
- Each ground pad of components on top layer should have via drilled to PCB layer 2 and via should be as close to pad as possible. A bulk decoupling capacitor needs two or more.
- Don't place ground plane and route signal trace below printed antenna or chip antenna to avoid destroying its electromagnetic field, and there is no organic coating on printed antenna. Check antenna chip vendor for the layout guideline and clearance.
- Move GND vias close to the pads.

3. Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

- A 4.7uF capacitor is used to decouple high frequency noise at digital and RF power terminals. This capacitor should be placed as close to power terminals as possible.
- In order to reduce PCB's parasitic effects, placing more via on ground plane is better.

4. Digital Interface

Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

- The digital interface to the module must be routed using good engineering practices to minimize coupling to power planes and other digital signals.
- The digital interface must be isolated from RF trace.

5. RF Trace

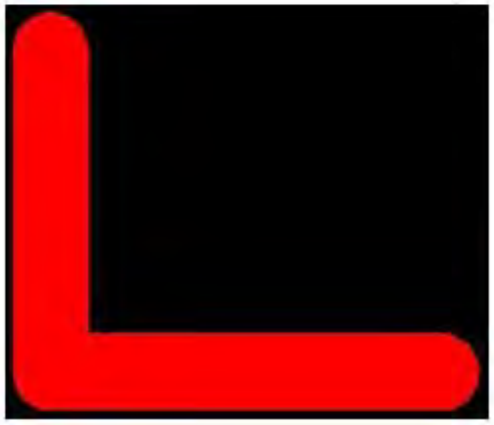
The RF trace is the critical to route. Here are some general rules for customers' reference.

- The RF trace impedance should be 50Ω between ANT port and antenna matching network.
- The length of the RF trace should be minimized.
- To reduce the signal loss, RF trace should laid on the top of PCB and avoid any via on it.
- The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.
- The RF trace must be isolated with aground beneath it. Other signal traces should be isolated

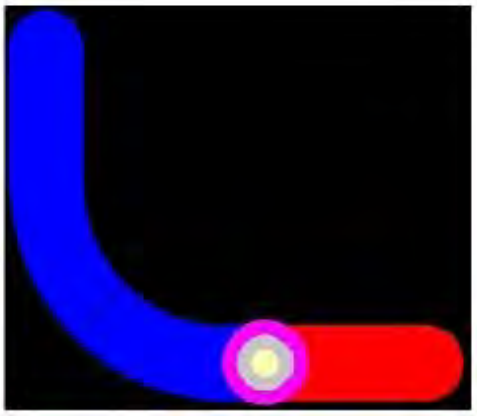
from the RF trace either by ground plane or ground vias to avoid coupling.

•To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

Correct RF trace



Right-angled corner



Via on RF trace

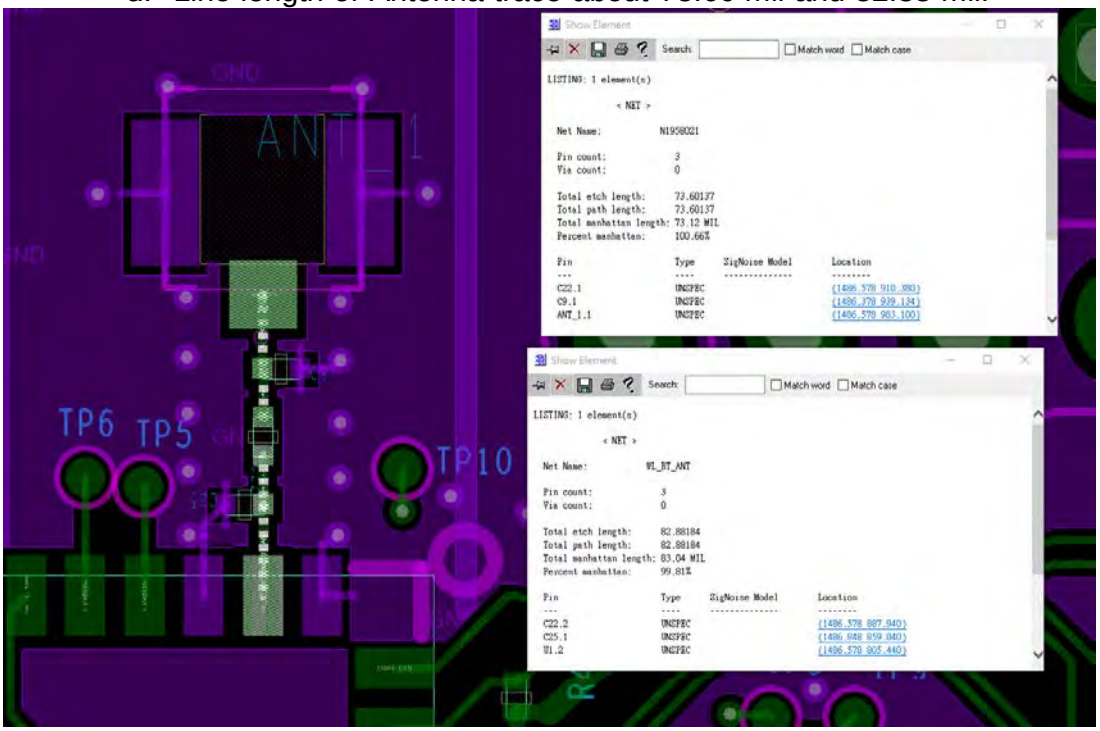
Incorrect RF trace

If the customers have any problem in calculation of trace impedance, please contact AzureWave.

AW-CM467 RF trace should be follow the rules as below

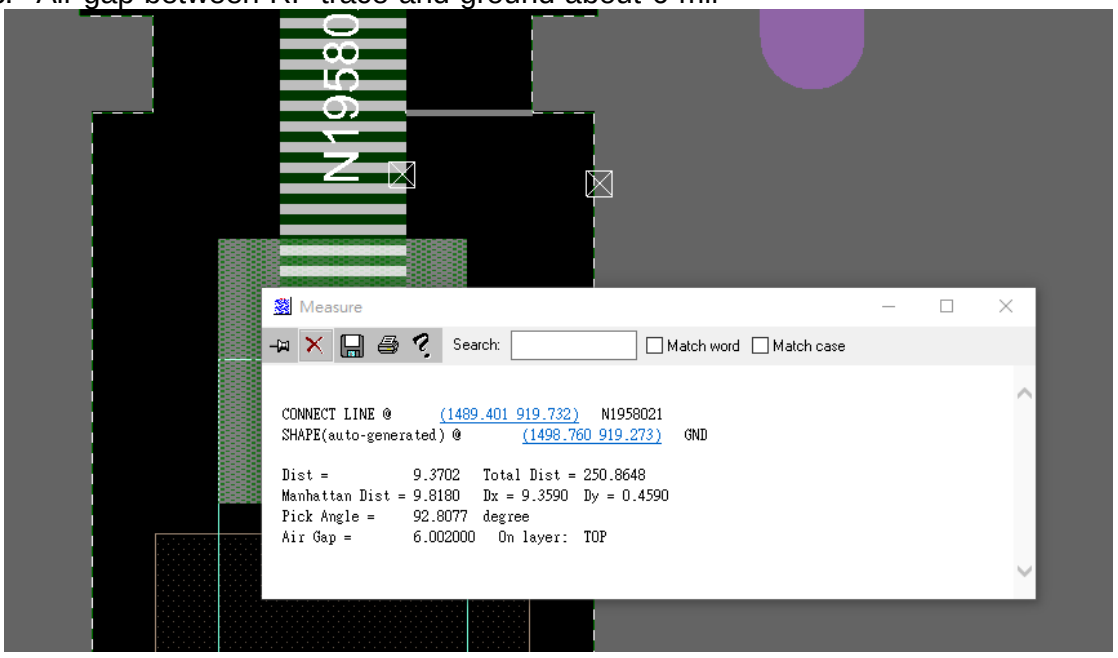
For MHF1 connector:

a. Line length of Antenna trace about 73.60 mil and 82.88 mil.



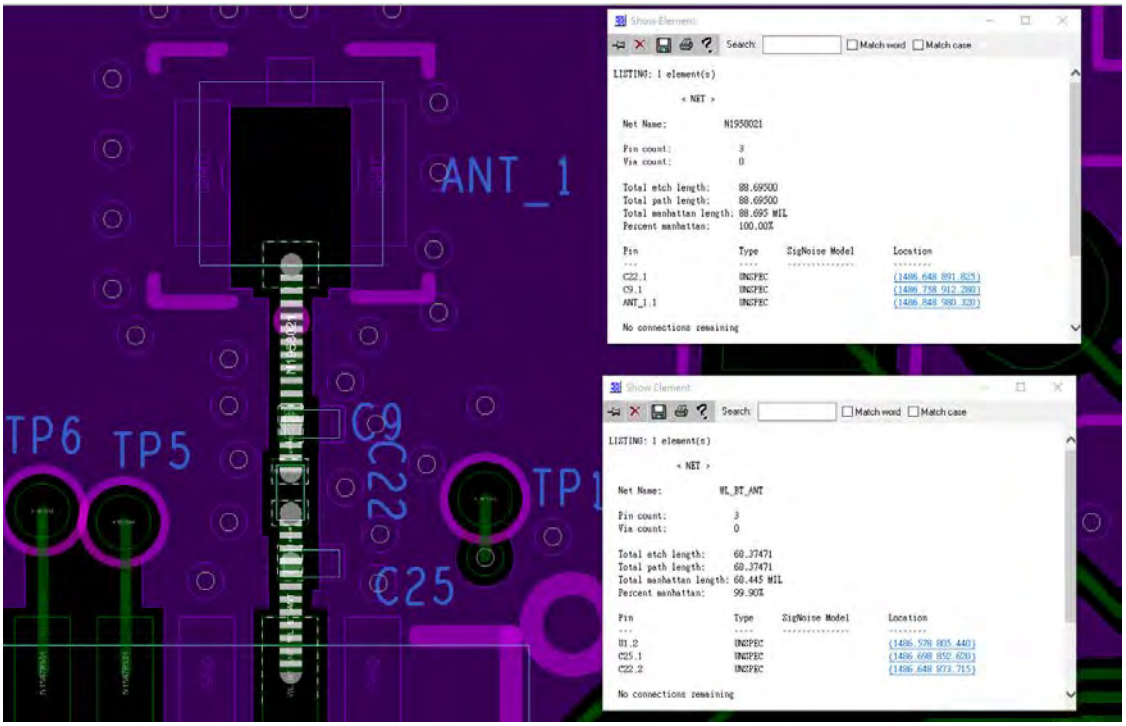
b. Line width of Antenna trace about 6 mil

c. Air gap between RF trace and ground about 6 mil



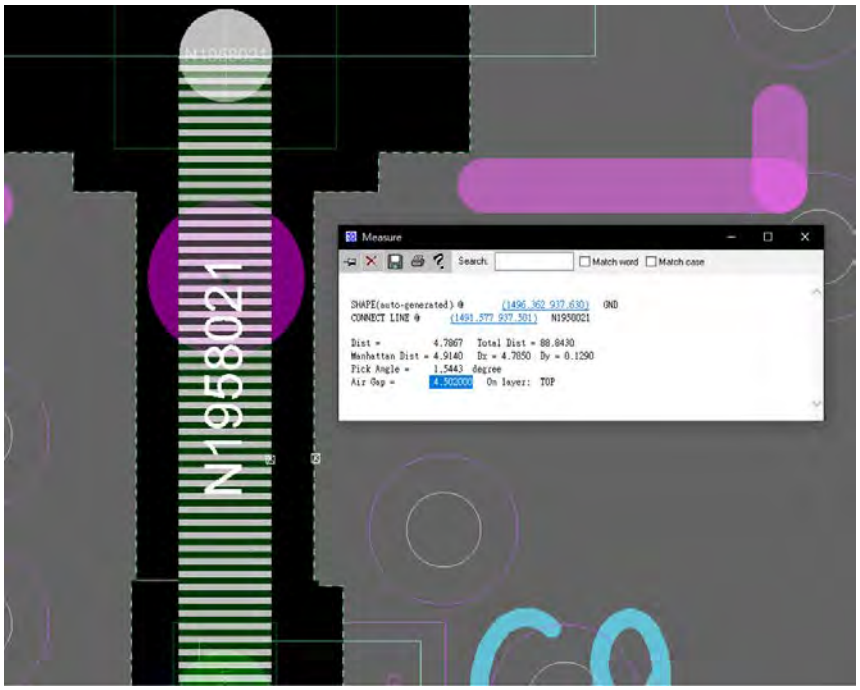
For MHF4 connector:

a. Line length of Antenna trace about 88.70 mil and 68.37 mil.



b. Line width of Antenna trace about 10 mil

c. Air gap between RF trace and ground about 4.5 mil

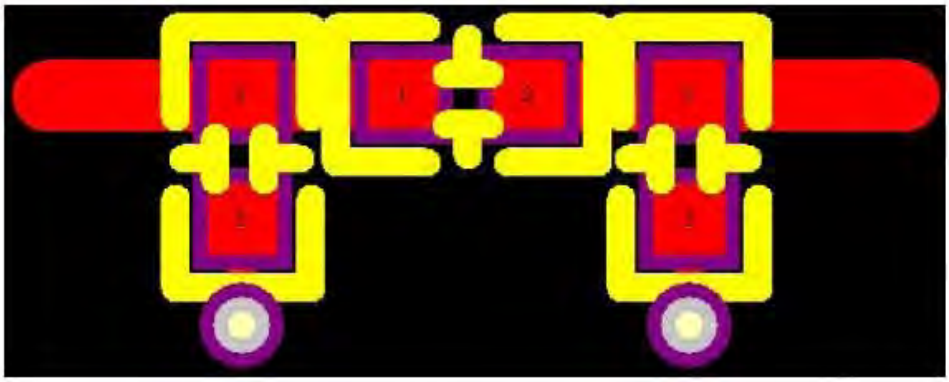


6. Antenna

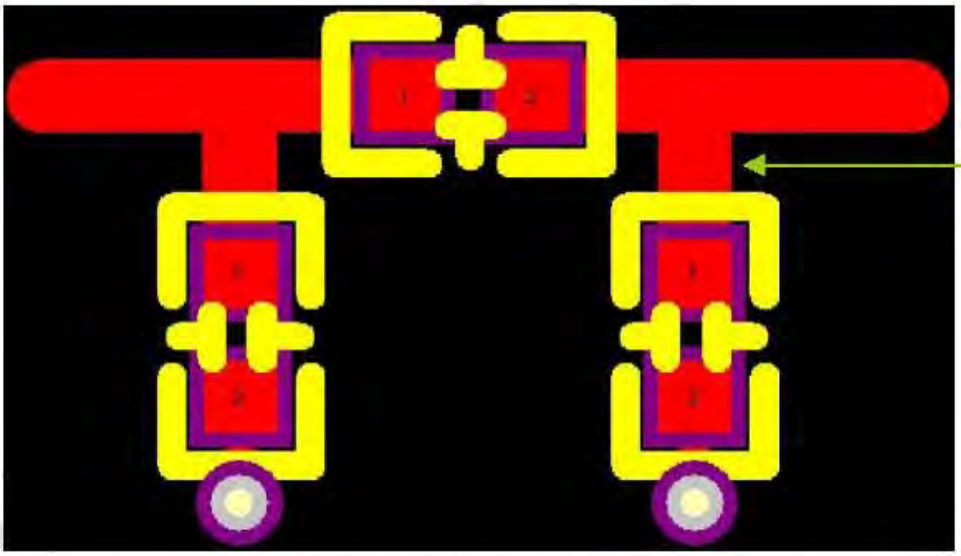
All the high-speed traces should be moved far away from the antenna. For the best radiation performance, check antenna chip vendor for the layout guideline and clearance.

7. Antenna Matching

PCB designer should reserve an antenna matching network for post tuning to ensure the antenna performance in different environments. Matching components should be close to each other. Stubs should also be avoided to reduce parasitic while no shunt component is necessary after tuning.



Correct layout for antenna matching



Incorrent layut for antenna matching

8. SHIELDING CASE

Magnetic shielding, ferrite drum shielding, or magnetic-resin coated shielding is highly recommended to prevent EMI issues.

9. GENERAL LAYOUT GUIDELINES

Follow these guidelines to obtain good signal integrity and avoid EMI:

1. Place components and route signals using the following design practices:
   - Keep analog and digital circuits in separate areas.
   - Identify all high-bandwidth signals and their return paths. Treat all critical signals as current loops. Check each critical loop area before the board is built. A small loop area is more important than short trace lengths.
   - Orient adjacent-layer traces so that they are perpendicular to one another to reduce crosstalk.
   - Keep critical traces on internal layers, where possible, to reduce emissions and improve immunity to external noise.

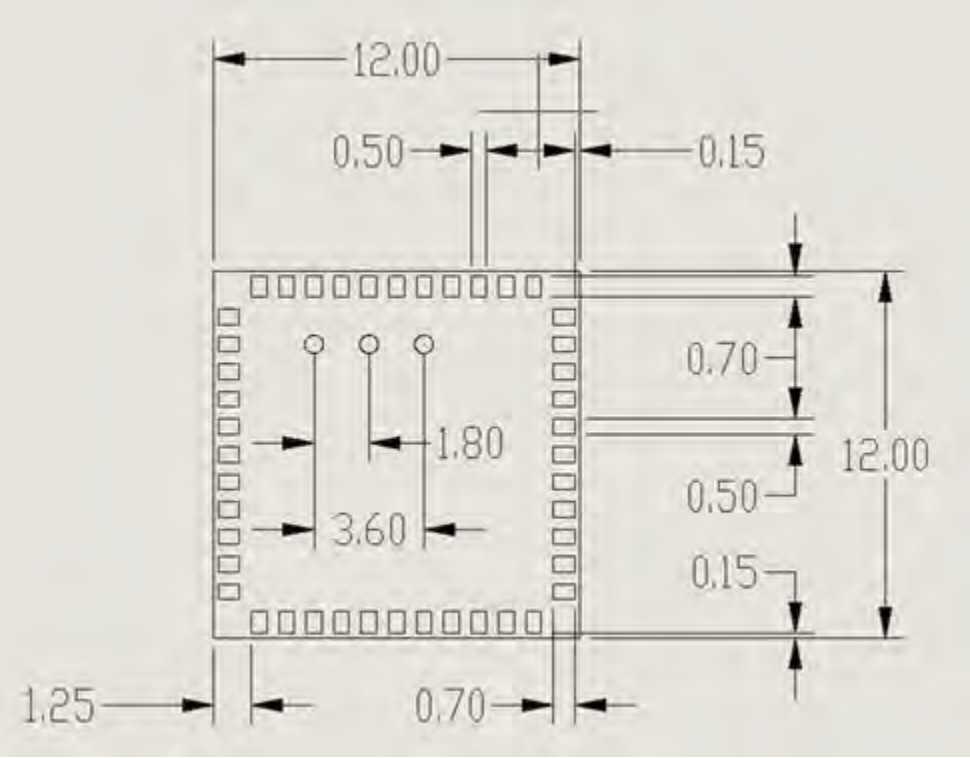
     However, RF traces should be routed on outside layers to avoid the use of vias on these traces.
   - Keep all trace lengths to a practical minimum. Keep traces, especially RF traces, straight wherever possible. Where turns are necessary, use curved traces or two 45-degree turns. Never use 90-degree turns.
2. Consider the following with respect to ground and power supply planes:
   - Route all supply voltages to minimize capacitive coupling to other supplies. Capacitive coupling can occur if supply traces on adjacent layers overlap. Supplies should be separated from each other in the stack-up by a ground plane, or they should be coplanar (routed on different areas of the same layer).
   - Provide an effective ground plane. Keep ground impedance as low as possible. Provide as much ground plane as possible and avoid discontinuities. Use as many ground vias as possible to connect all ground layers together.
   - Maximize the width of power traces. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.
3. Consider these power supply decoupling practices:
   - Place decoupling capacitors near target power pins. If possible, keep them on the same side as the

IC they decouple to avoid vias that add inductance. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it by a copper trace. Instead, make the connection directly to the associated planes using vias.

• Use appropriate capacitance values for the target circuit, and consider each capacitor's self-resonant frequency.

10. LGA Module stencil and Pad opening Suggestion

Stencil thickness：0.10~0.12mm
Function Pad opening size suggestion: Max. 1:1
PS: This opening suggestion just for customer reference, please discuss with AzureWave's Engineer before you start SMT.



Example:

11. The other layout guide Information

• Make sure every power traces have good return path (ground path).

• Connect the input pins of unused internal regulators to ground.

• Leave the output pins of unused internal regulators floating.

• High speed interface (i.e. UART/SDIO/HSIC) shall have equal electrical length. Keep them away from noise sensitive blocks.

• Good power integrity of VDDIO will improve the signal integrity of digital interfaces.

• Good return path and well shielded signal can reduce crosstalk, EMI emission and improve signal integrity.

• RF IO is around 50 ohms, reserve Pi or T matching network to have better signal transition from port to port.

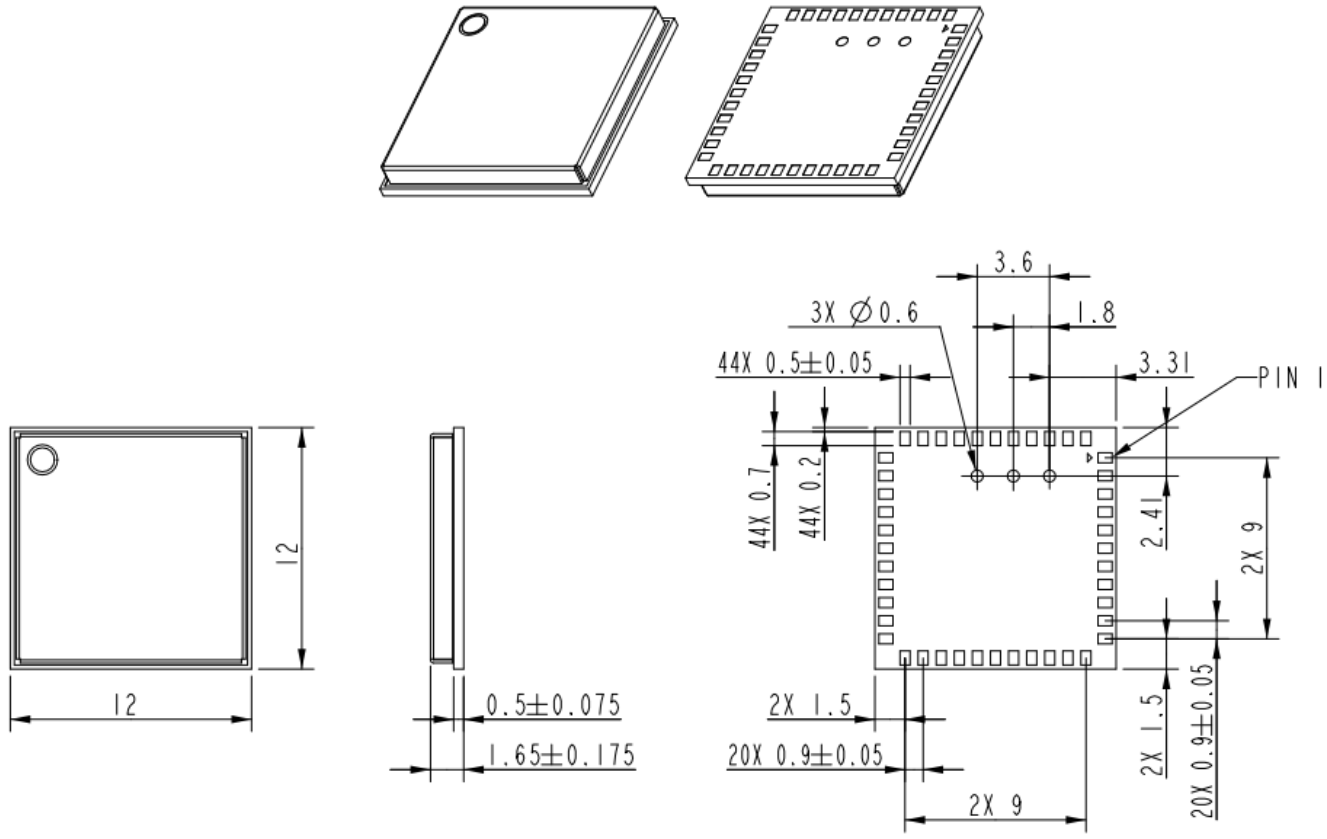
• Smooth RF trace help to reduce insertion loss. Do not use 90 degrees turn (use two 45 degrees turns or one miter bend instead).

• Well arranged ground plane near antenna and antenna itself will help to reduce near field coupling between other RF sources (e.g. GSM/CDMA … antennas).

• Discuss with AzureWave Engineer after you finish schematic and layout job.

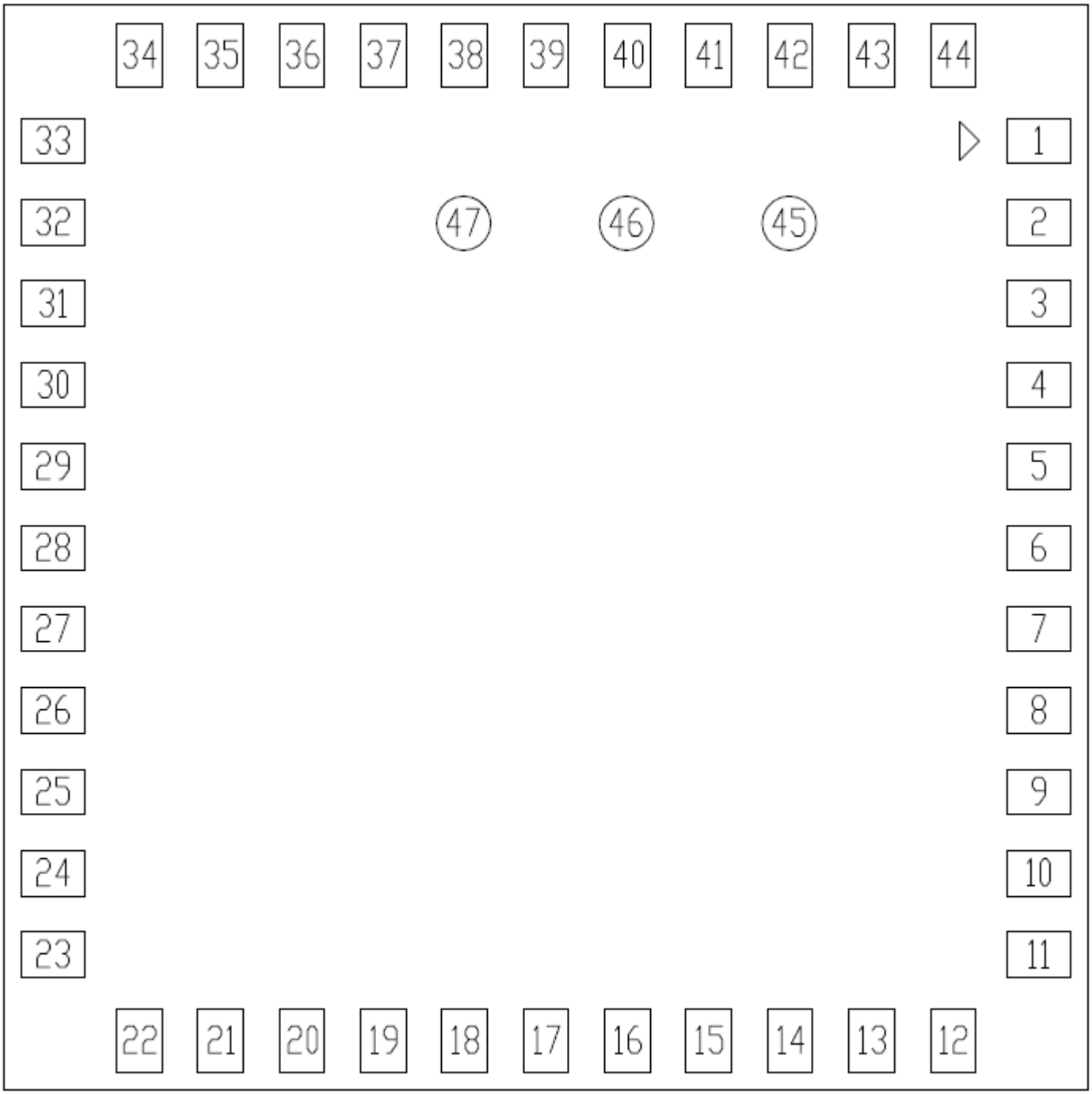
12. Mechanical Drawing

•Package Outline Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

•**Bottom View of PCB Layout Foot Print**



PIN DEFINED(BOTTOM VIEW)

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:

This module is intended for OEM integrator. This module is only FCC authorized for the specific rule parts listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Additional testing and certification may be necessary when multiple modules are used.

20cm minimum distance has to be able to be maintained between the antenna and the users for the host this module is integrated into. Under such configuration, the FCC radiation exposure limits set forth for an population/uncontrolled environment can be satisfied.

Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following " Contains TX FCC ID: TLZ-CM467".

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received,

including interference that may cause undesired operation.

Ant.	Brand	Model Name	Antenna Type	Gain (dBi)	
				WLAN 2.4GHz/Bluetooth	WLAN 5GHz
1	Nienyi	NYS4939	PCB	3.58	3.89
2	Genesis	650-10045-01	PCB	2.5	3.85
3	Lynwave	5-PP005737	PCB	4.2	3.6
4	Maglayers	MSA-4008-25GC1-A1	PIFA	2.98	5.16
5	Maglayers	MSA-4008-25GC1-A2	PIFA	2.98	5.16

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:
(1) This device may not cause interference.
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil contient des émetteurs / récepteurs exempts de licence qui sont conformes au (x) RSS (s) exemptés de licence d'Innovation, Sciences et Développement économique Canada. L'opération est soumise aux deux conditions suivantes:
(1) Cet appareil ne doit pas provoquer d'interférences.
(2) Cet appareil doit accepter toute interférence, y compris les interférences susceptibles de provoquer un fonctionnement indésirable de l'appareil.

This radio transmitter [6100A-CM467] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Le présent émetteur radio (6100A-CM467) a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal d'antenne. Les types d'antennes non inclus dans cette liste qui ont un gain supérieur au gain maximal indiqué pour tout type listé sont strictement interdits pour une utilisation avec cet appareil.

Ant.	Brand	Model Name	Antenna Type	Gain (dBi)	
				WLAN 2.4GHz/Bluetooth	WLAN 5GHz
1	Nienyi	NYS4939	PCB	3.58	3.89
2	Genesis	650-10045-01	PCB	2.5	3.85
3	Lynwave	5-PP005737	PCB	4.2	3.6
4	Maglayers	MSA-4008-25GC1-A1	PIFA	2.98	5.16
5	Maglayers	MSA-4008-25GC1-A2	PIFA	2.98	5.16

The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.
les dispositifs fonctionnant dans la bande 5150-5250 MHz sont réservés uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux.

The maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall be such that the equipment still complies with the e.i.r.p. limit.
le gain maximal d'antenne permis pour les dispositifs utilisant les bandes 5250-5350 MHz et 5470-5725 MHz doit se conformer à la limite de p.i.r.e.

The maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits specified for point-to-point and non-point-to-point operation as appropriate.
le gain maximal d'antenne permis (pour les dispositifs utilisant la bande 5725-5850 MHz)
doit se conformer à la limite de p.i.r.e. spécifiée pour l'exploitation point à point et non point à point, selon le cas.

For indoor use only.
Pour une utilisation en intérieur uniquement.

IMPORTANT NOTE:
This module is intended for OEM integrator. The OEM integrator is responsible for the compliance to all the rules that apply to the product into which this certified RF module is integrated. Additional testing and certification may be necessary when multiple modules are used.

20cm minimum distance has to be able to be maintained between the antenna and the users for the host this module is integrated into. Under such configuration, the IC RSS-102 radiation exposure limits set forth for an population/uncontrolled environment can be satisfied.

Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

USERS MANUAL OF THE END PRODUCT:
In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the IC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment. Operation is subject to the following two conditions: (1) this device may not cause harmful interference (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following " Contains IC: 6100A-CM467". The Host Model Number (HMN) must be indicated at any location on the exterior of the end product or product packaging or product literature which shall be available with the end product or online.

5GHz band (W52, W53): Indoor use only (except communicate to high power radio)

取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。低功率射頻器材之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。前述合法通信，指依電信管理法規定作業之無線電通信。低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

應避免影響附近雷達系統之操作。

本模組於取得認證後將依規定於模組本體標示審驗合格標籤，並要求平台廠商於平台上標示「本產品內含射頻模組 CC XX xx LP yyy Z z。