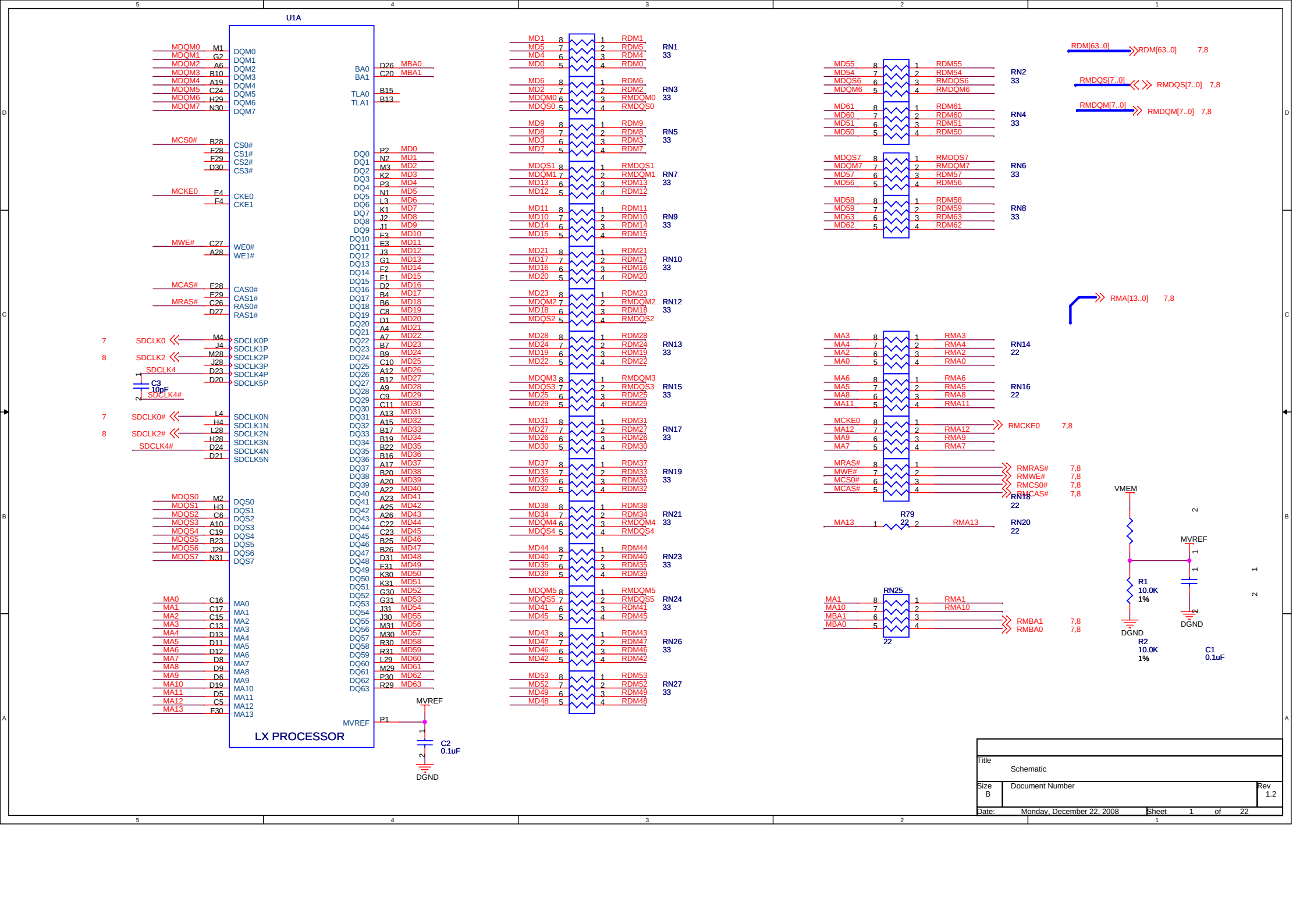

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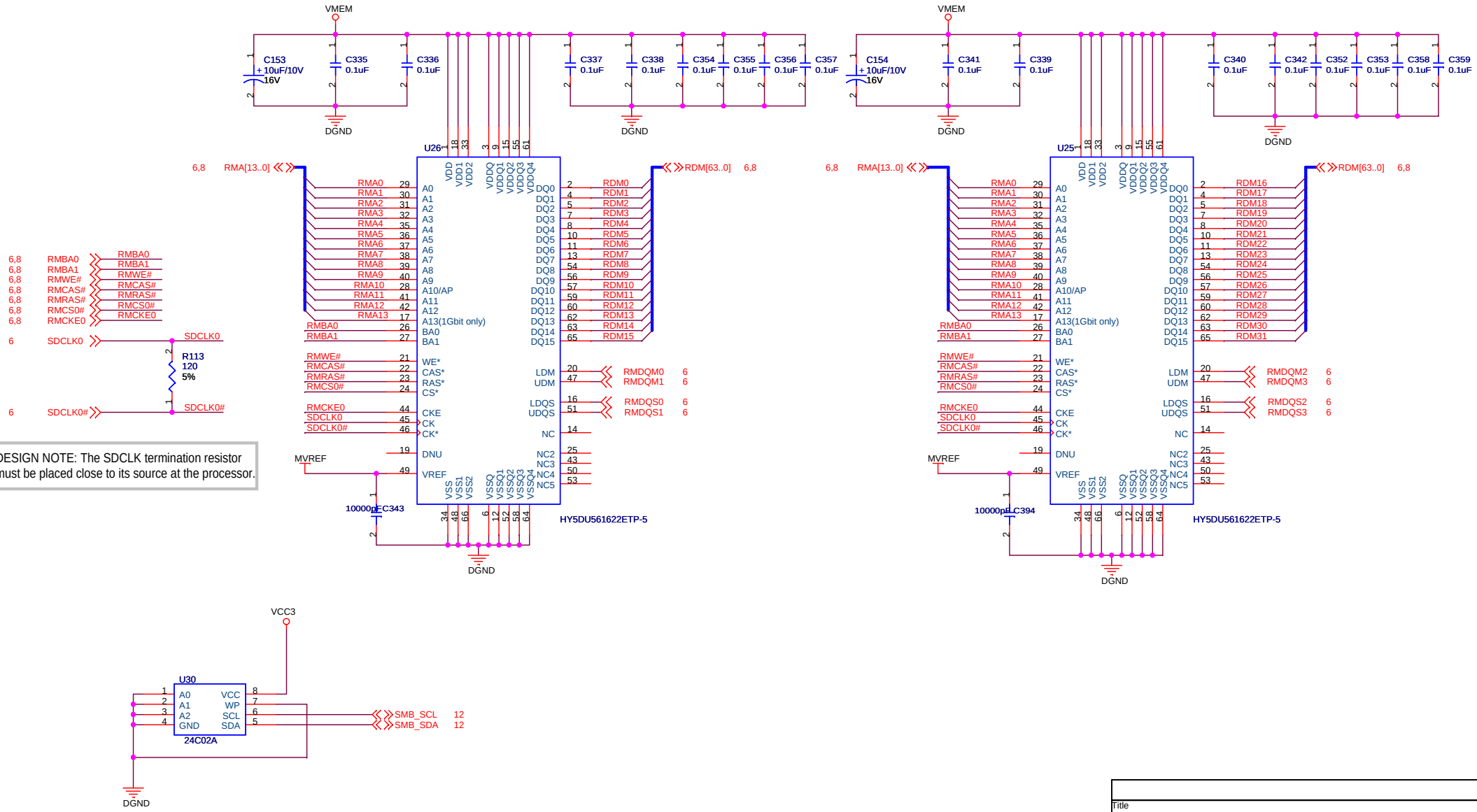
DESIGN NOTE: Signal ordering of the data bus has not been optimized in this schematic.
A preliminary layout would be required.



Title	Schematic	
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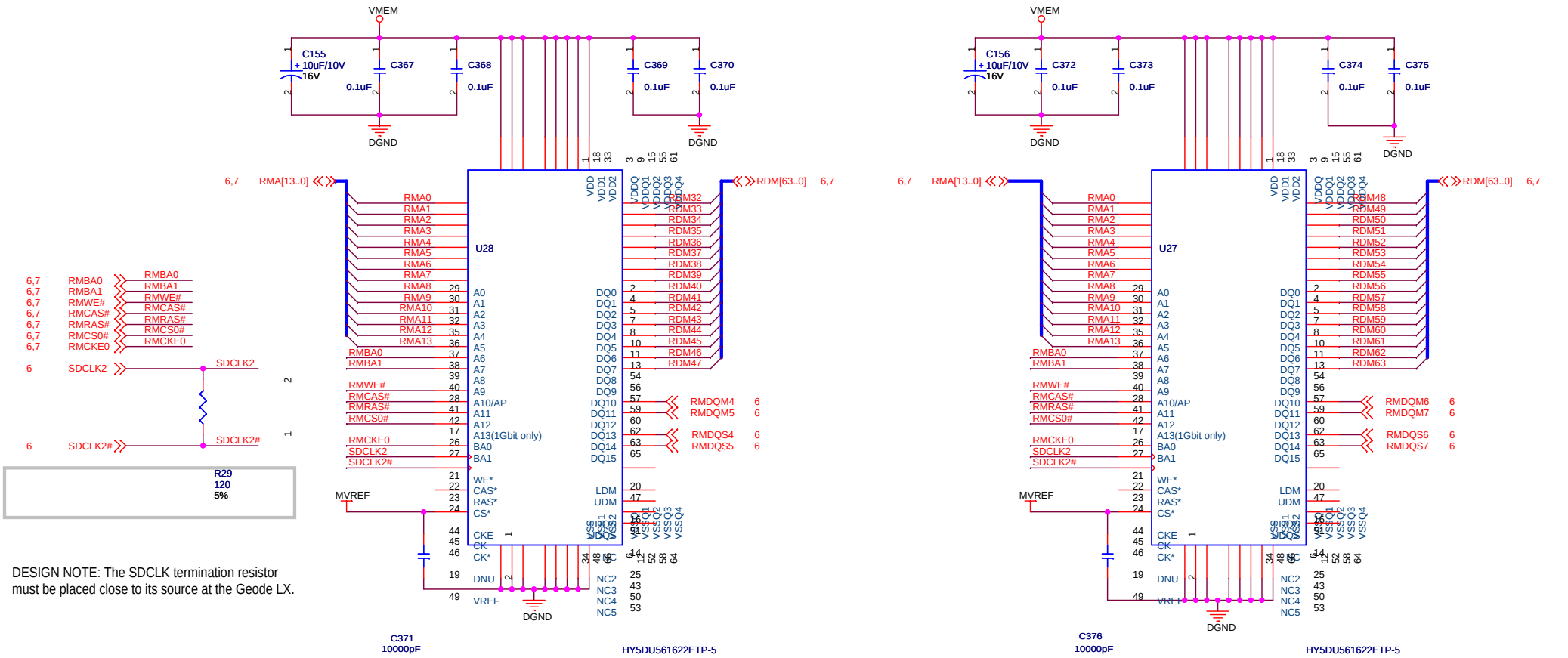

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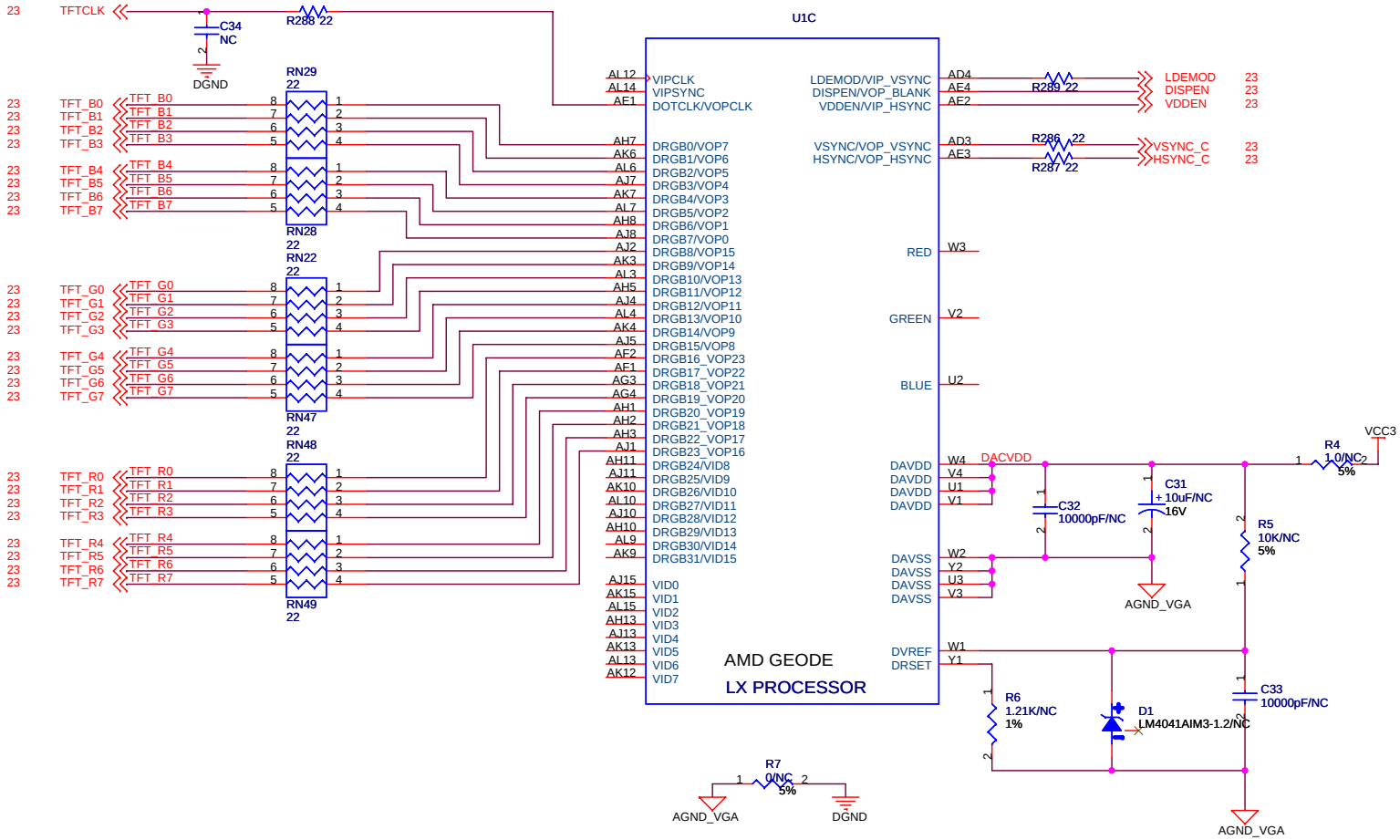

DESIGN NOTE: AGND_VGA should be an island with single point connection to the full ground plane to reduce noise content. Zero ohm resistor can be removed as long as above condition is met.

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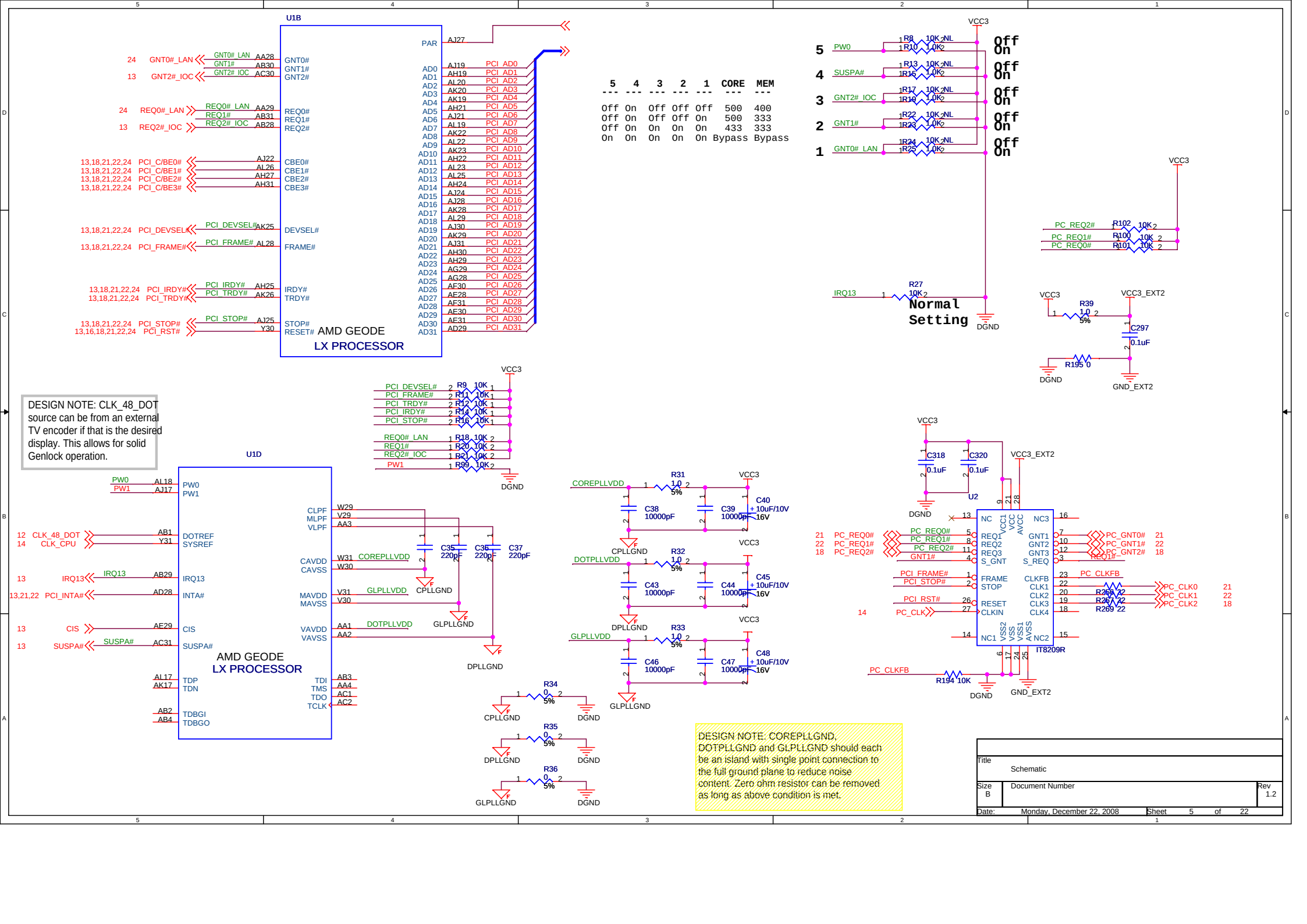
U1B
AMD GEODE
LX PROCESSOR
U1D
AMD GEODE
LX PROCESSOR
5 4 3 2 1 CORE MEM
Off On Off Off Off 500 400
Off On Off Off On 500 333
Off On On On On 433 333
On On On On On Bypass Bypass
Normal Setting
DESIGN NOTE: CLK_48_DOT source can be from an external TV encoder if that is the desired display. This allows for solid Genlock operation.
DESIGN NOTE: COREPLLGND, DOTPLLGND and GLPLLGND should each be an island with single point connection to the full ground plane to reduce noise content. Zero ohm resistor can be removed as long as above condition is met.
IT8209R
Title
Schematic
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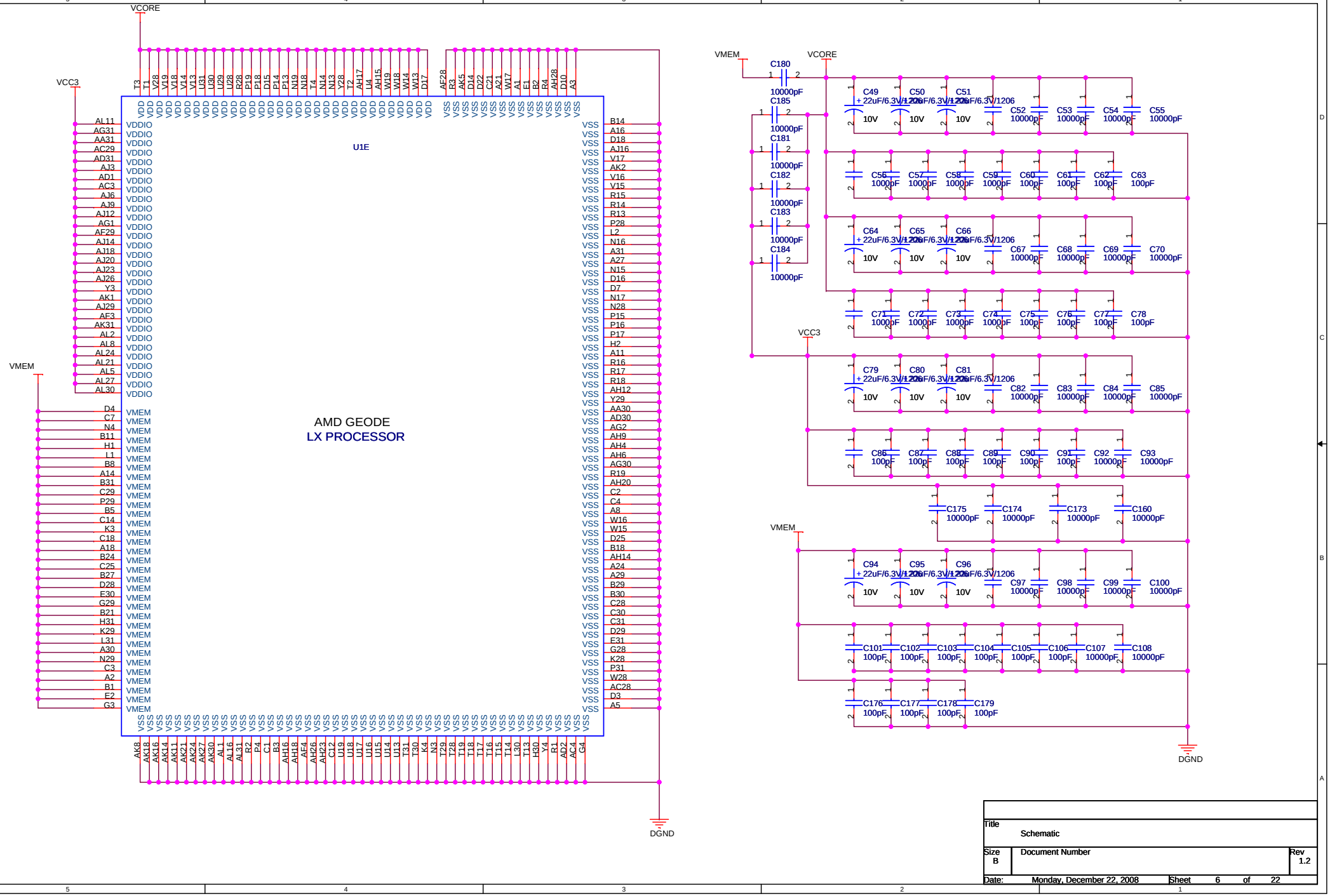

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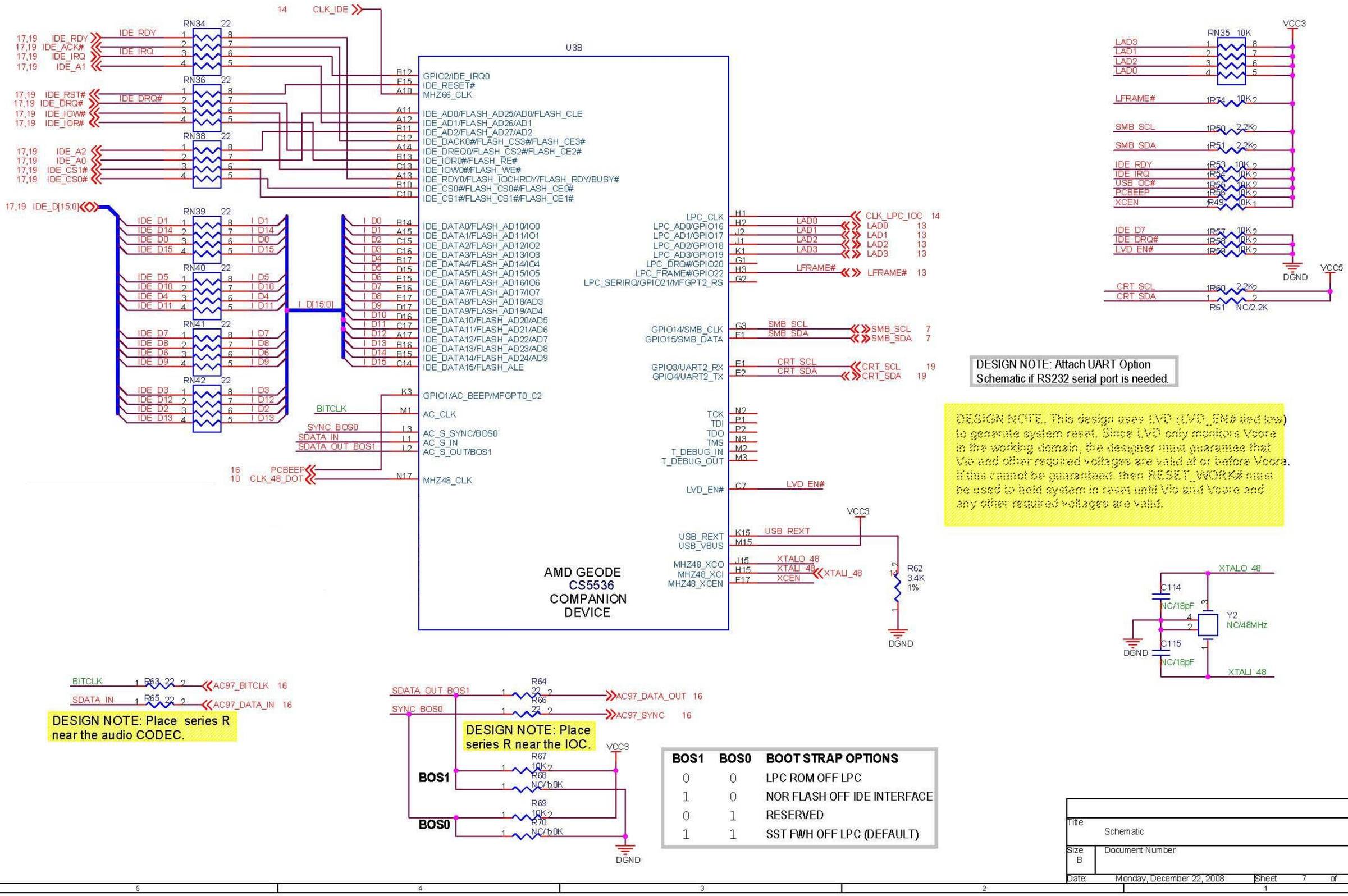

BOS1	BOS0	BOOT STRAP OPTIONS
0	0	LPC ROM OFF LPC
1	0	NOR FLASH OFF IDE INTERFACE
0	1	RESERVED
1	1	SST FWH OFF LPC (DEFAULT)

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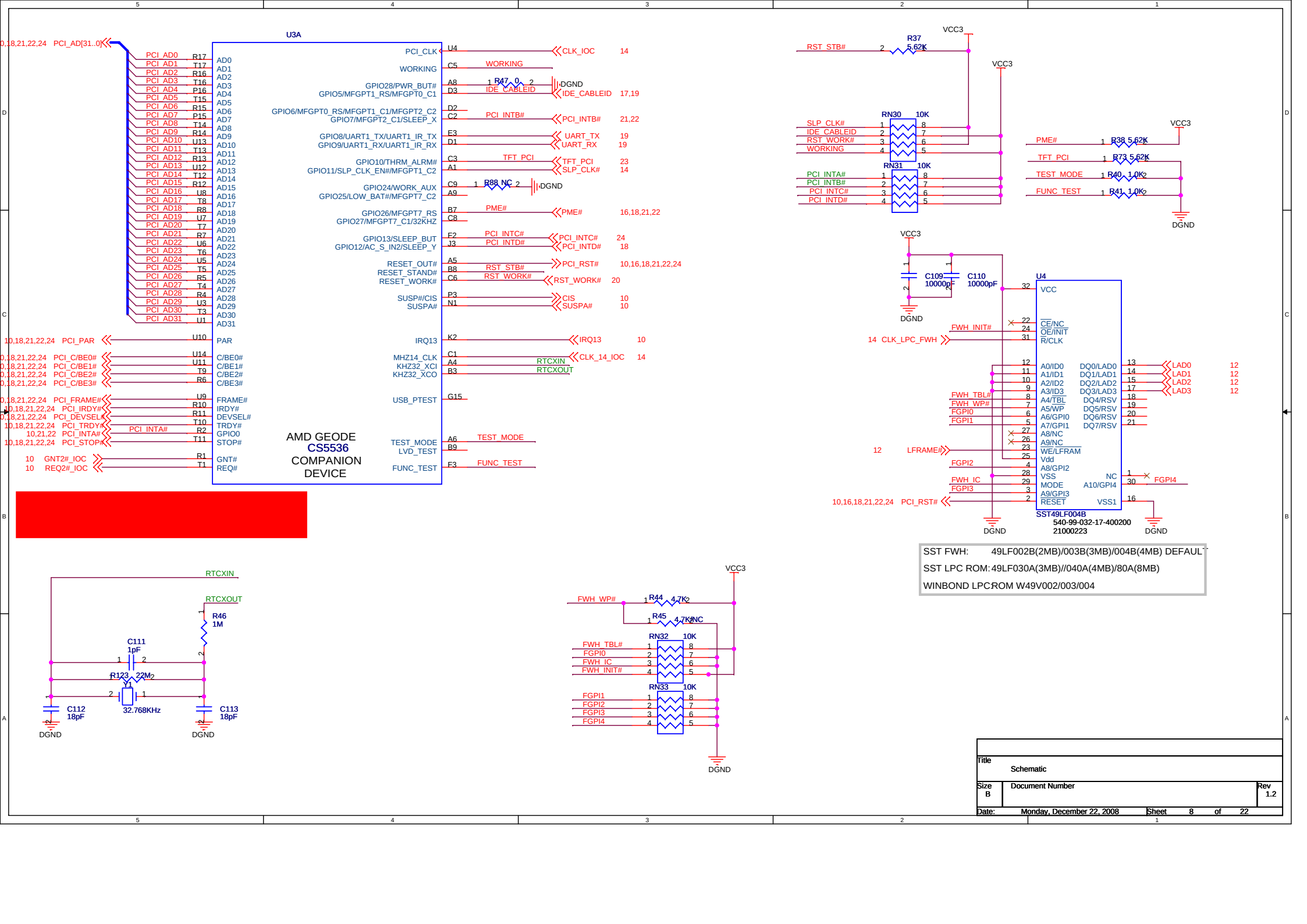
U3A
AMD GEODE
CS5536
COMPANION
DEVICE
PCI_AD[31..0]
PCI_PAR
PCI_C/BE0#
PCI_C/BE1#
PCI_C/BE2#
PCI_C/BE3#
PCI_FRAME#
PCI_IRDY#
PCI_DEVSEL#
PCI_TRDY#
PCI_INTA#
PCI_STOP#
GNT2#_IOC
REQ2#_IOC
PCI_CLK
WORKING
IDE_CABLEID
PCI_INTB#
UART_TX
UART_RX
TFT_PCI
SLP_CLK#
PME#
PCI_INTC#
PCI_INTD#
PCI_RST#
RST_STB#
RST_WORK#
CIS
SUSPA#
IRQ13
CLK_14_IOC
RTCXIN
RTCXOUT
TEST_MODE
FUNC_TEST
CLK_IOC
R88 NC
R47 0
RST_STB
VCC3
R37 5.62K
RN30 10K
RN31 10K
R38 5.62K
R73 5.62K
R40 1.0K
R41 1.0K
C109 10000pF
C110 10000pF
U4
SST49LF004B
540-99-032-17-400200
21000223
SST FWH: 49LF002B(2MB)/003B(3MB)/004B(4MB) DEFAUL
SST LPC ROM: 49LF030A(3MB)//040A(4MB)/80A(8MB)
WINBOND LPC ROM W49V002/003/004
R46 1M
C111 1pF
R123 22M
Y1 32.768KHz
C112 18pF
C113 18pF
R44 4.7K
R45 4.7K NC
RN32 10K
RN33 10K
DGND
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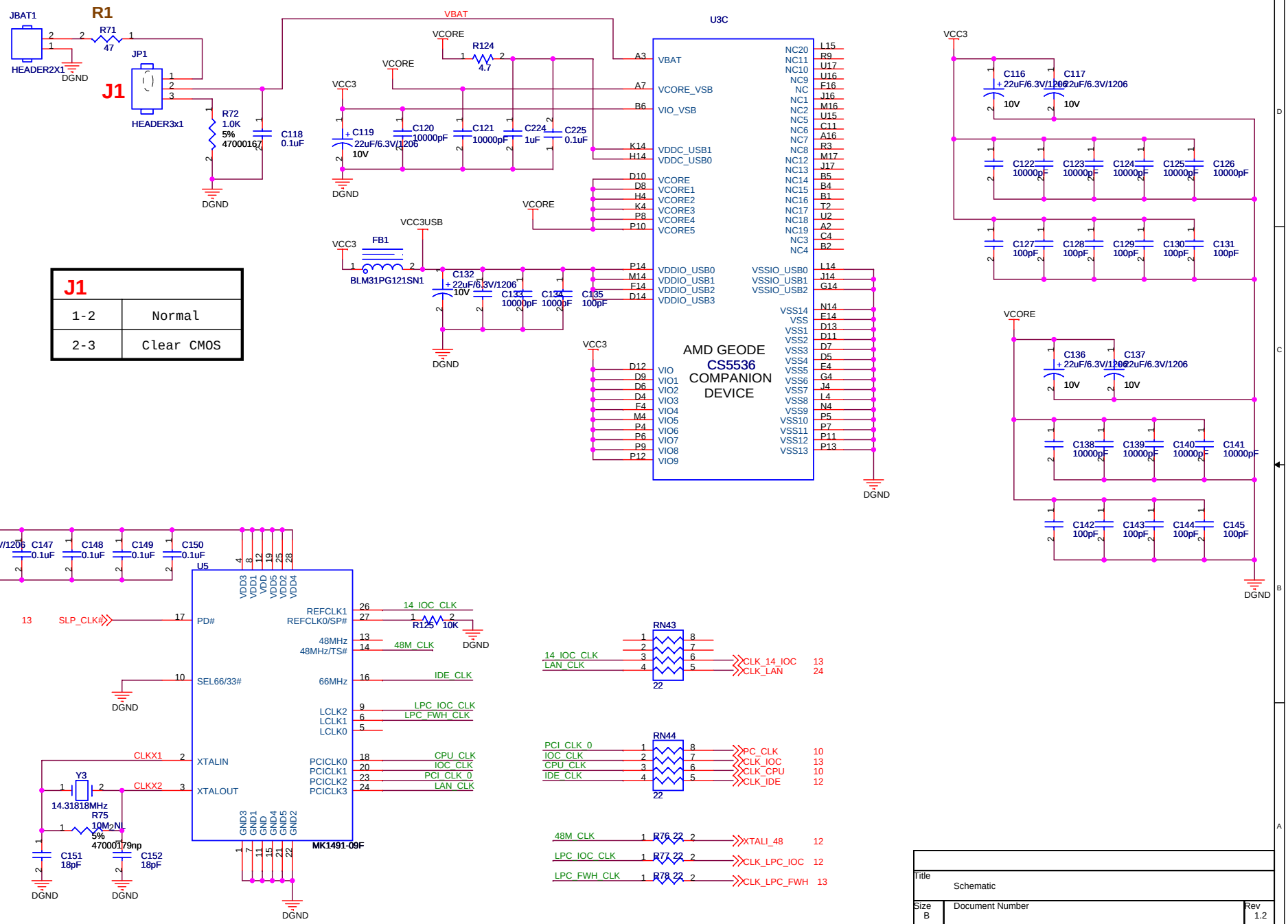
DESIGN NOTE: Without UL approval of the internal VBAT circuity, a 47 ohm resistor (R1) is required. UL approval is in process and is expected. With UL approval R1 can be removed.

J1	
1-2	Normal
2-3	Clear CMOS



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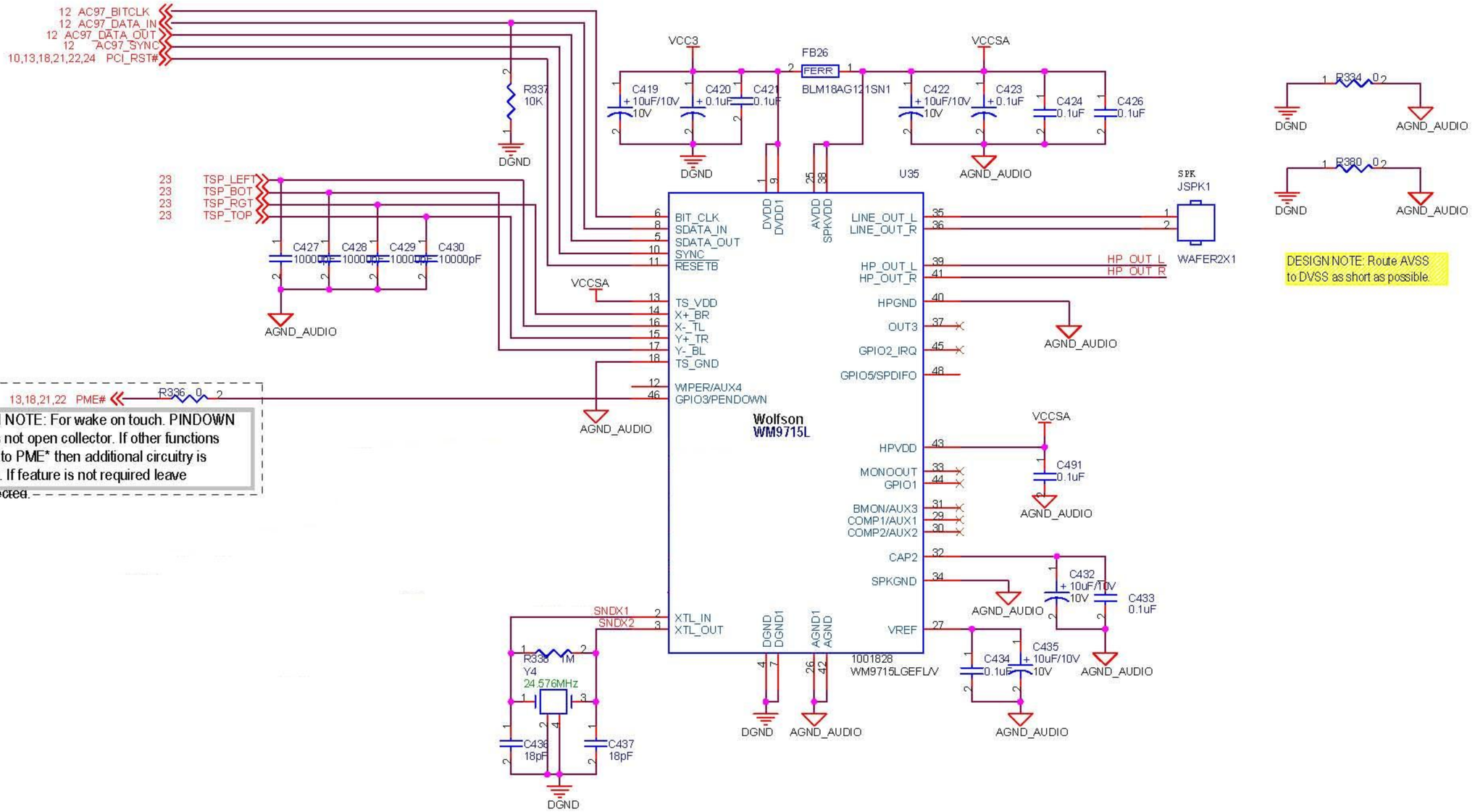

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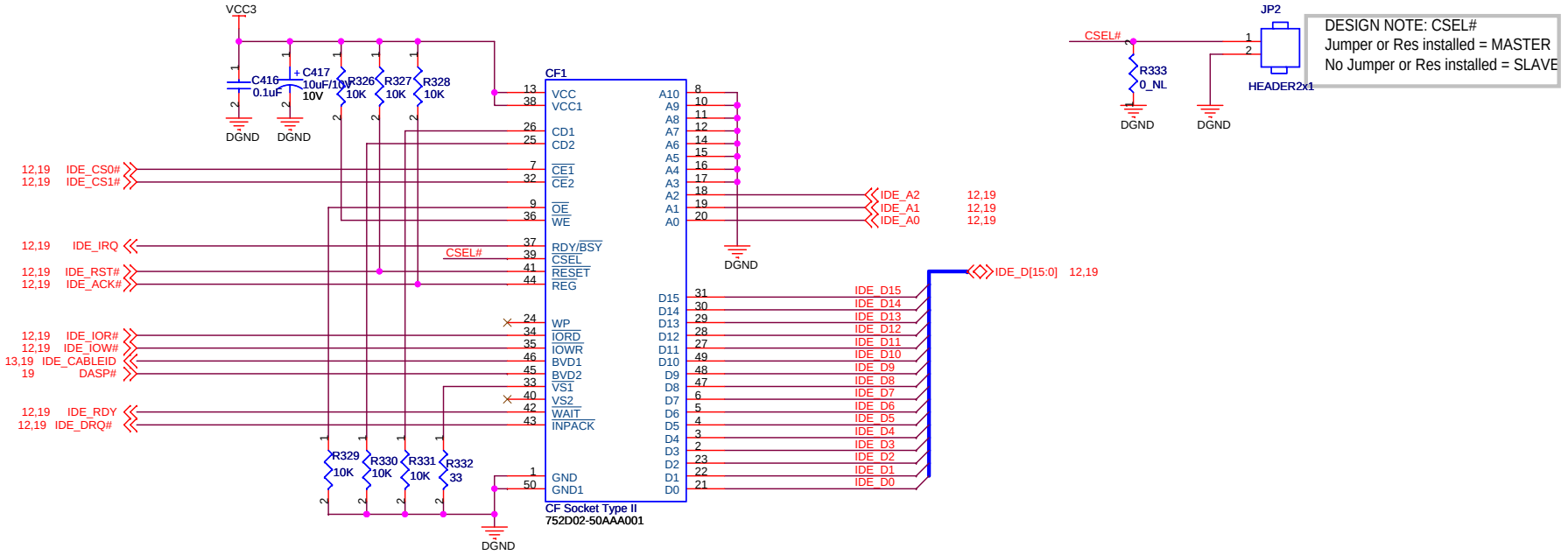
COMPACT FLASH CONNECTOR
Master/Slave (Type II)



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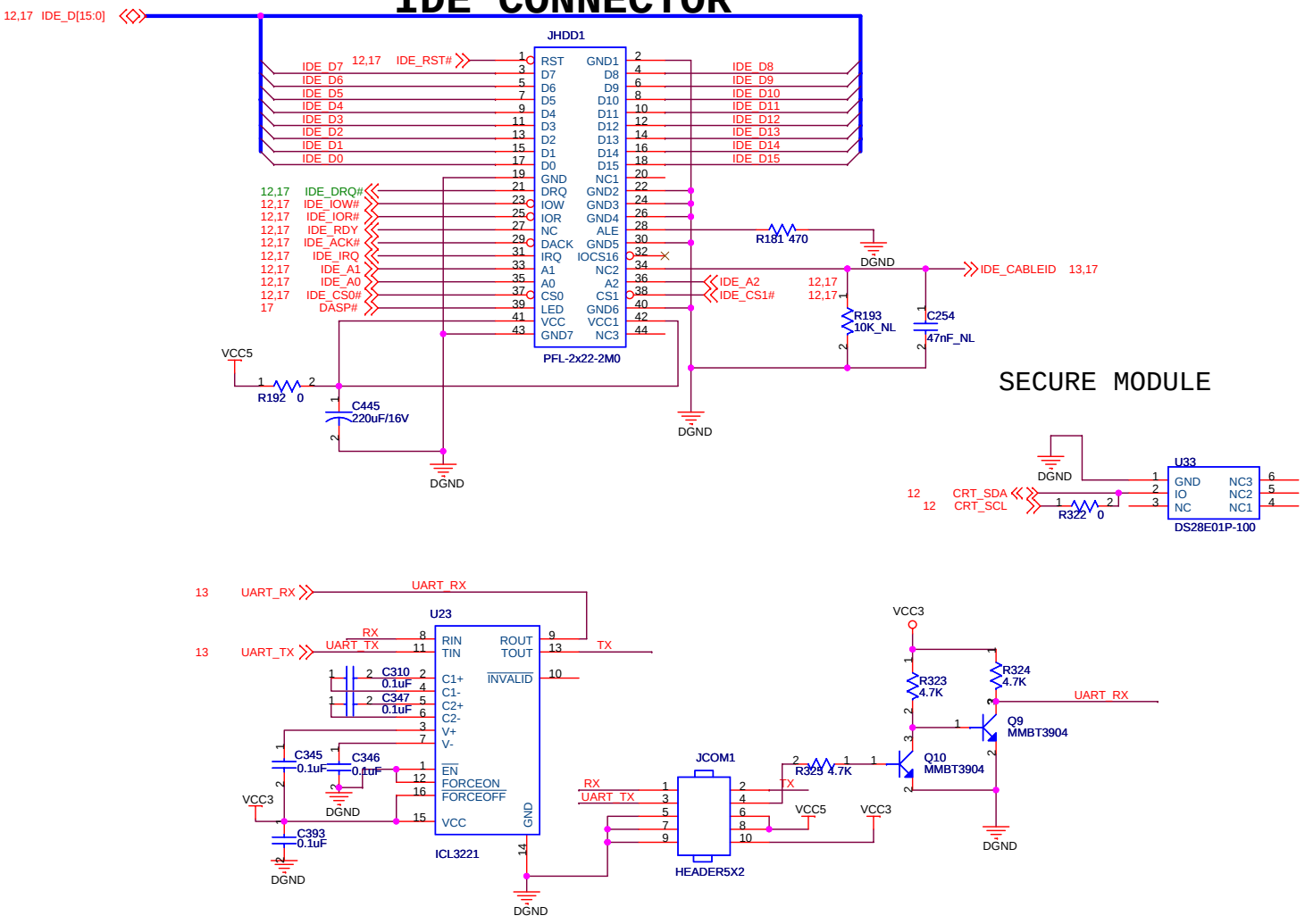
IDE CONNECTOR



Notes:If place U23, do not place R324 and Q9.

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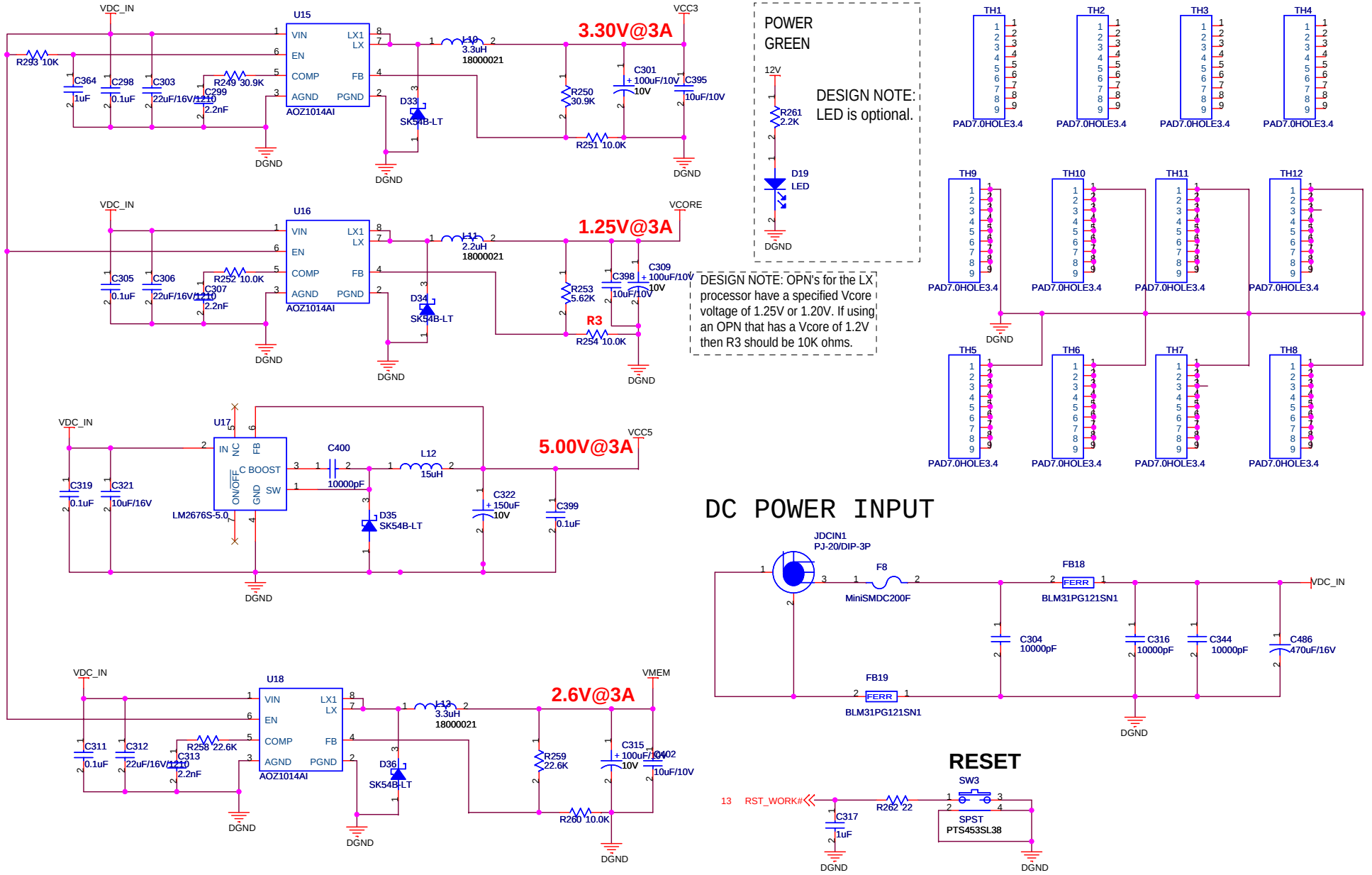

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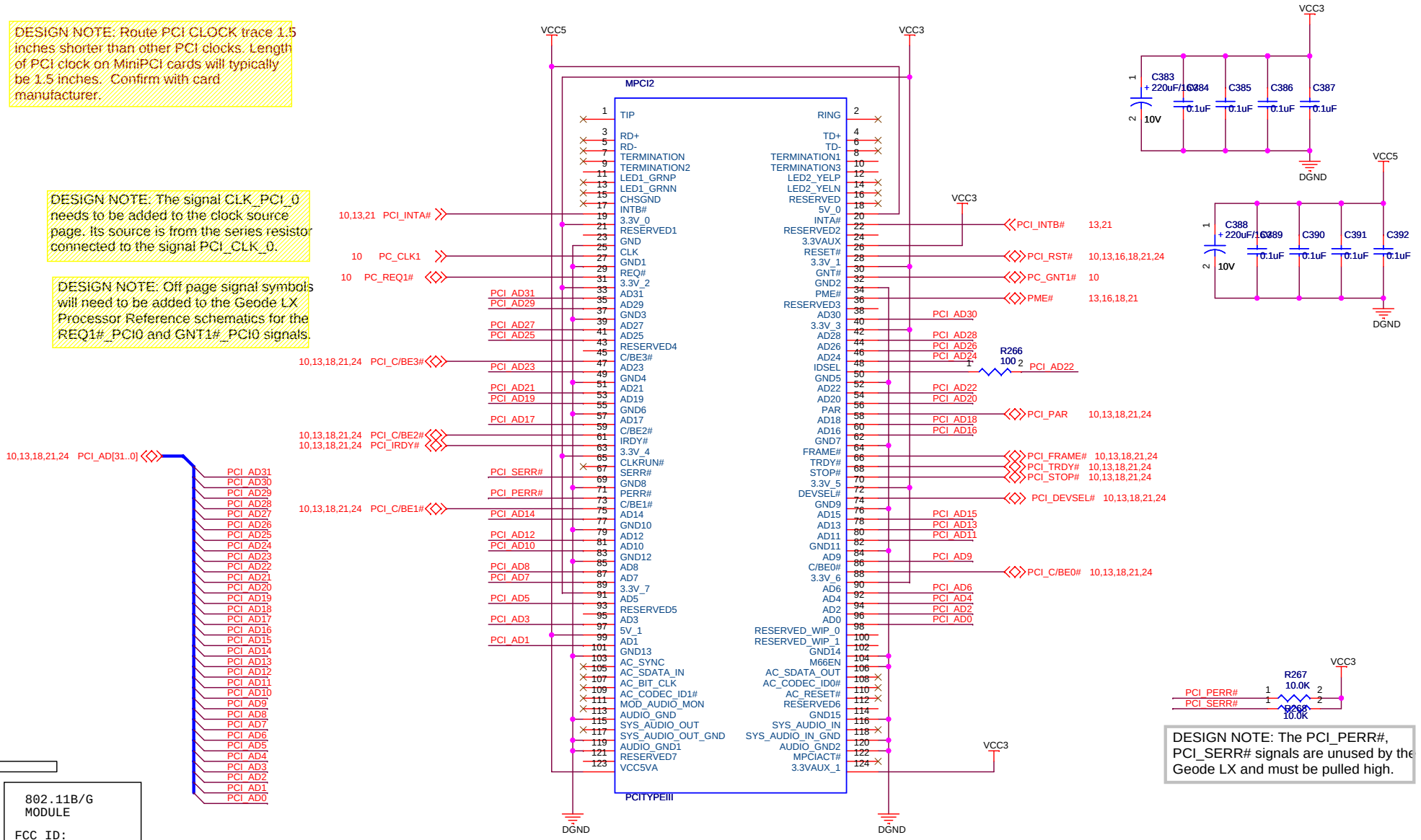
DESIGN NOTE: Route PCI CLOCK trace 1.5 inches shorter than other PCI clocks. Length of PCI clock on MiniPCI cards will typically be 1.5 inches. Confirm with card manufacturer.

DESIGN NOTE: The signal CLK_PCI_0 needs to be added to the clock source page. Its source is from the series resistor connected to the signal PCI_CLK_0.

DESIGN NOTE: Off page signal symbols will need to be added to the Geode LX Processor Reference schematics for the REQ1#_PCI0 and GNT1#_PCI0 signals.



DESIGN NOTE: The PCI_PERR#, PCI_SERR# signals are unused by the Geode LX and must be pulled high.

DESIGN NOTE: Consult MiniPCI card manufacturer for any special design or layout considerations of MiniPCI slot to accomidate a particular MiniPCI card.

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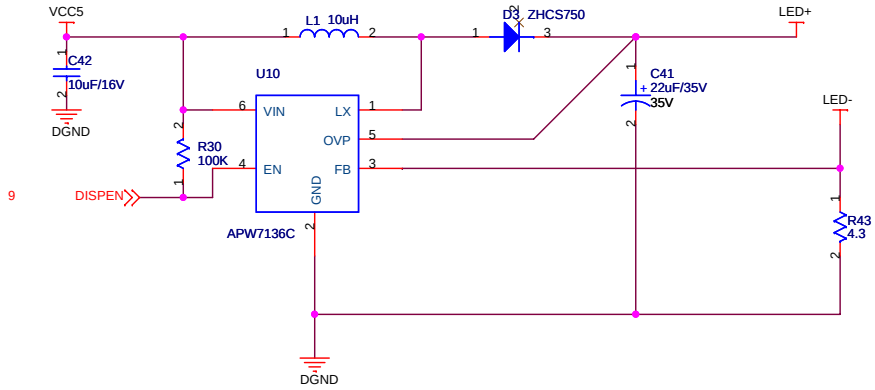
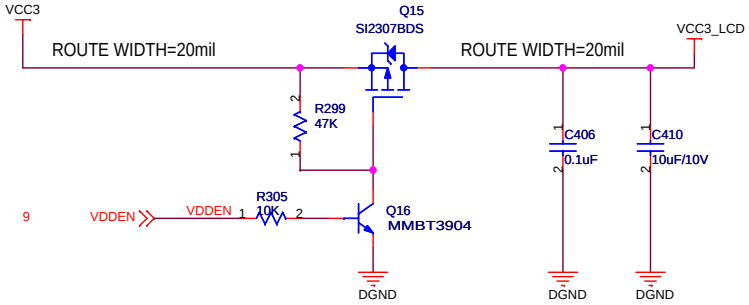
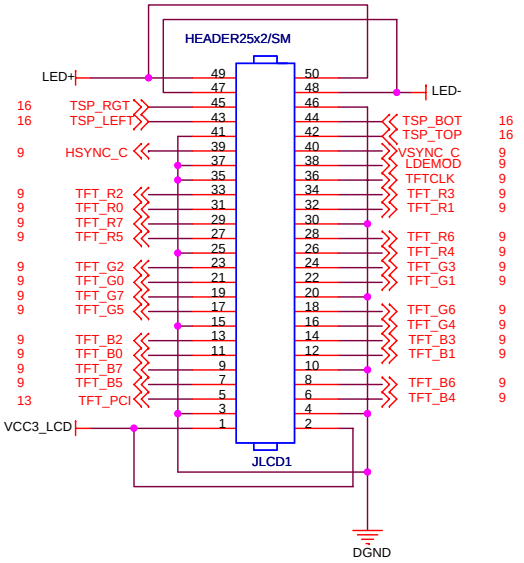




TFT Connector



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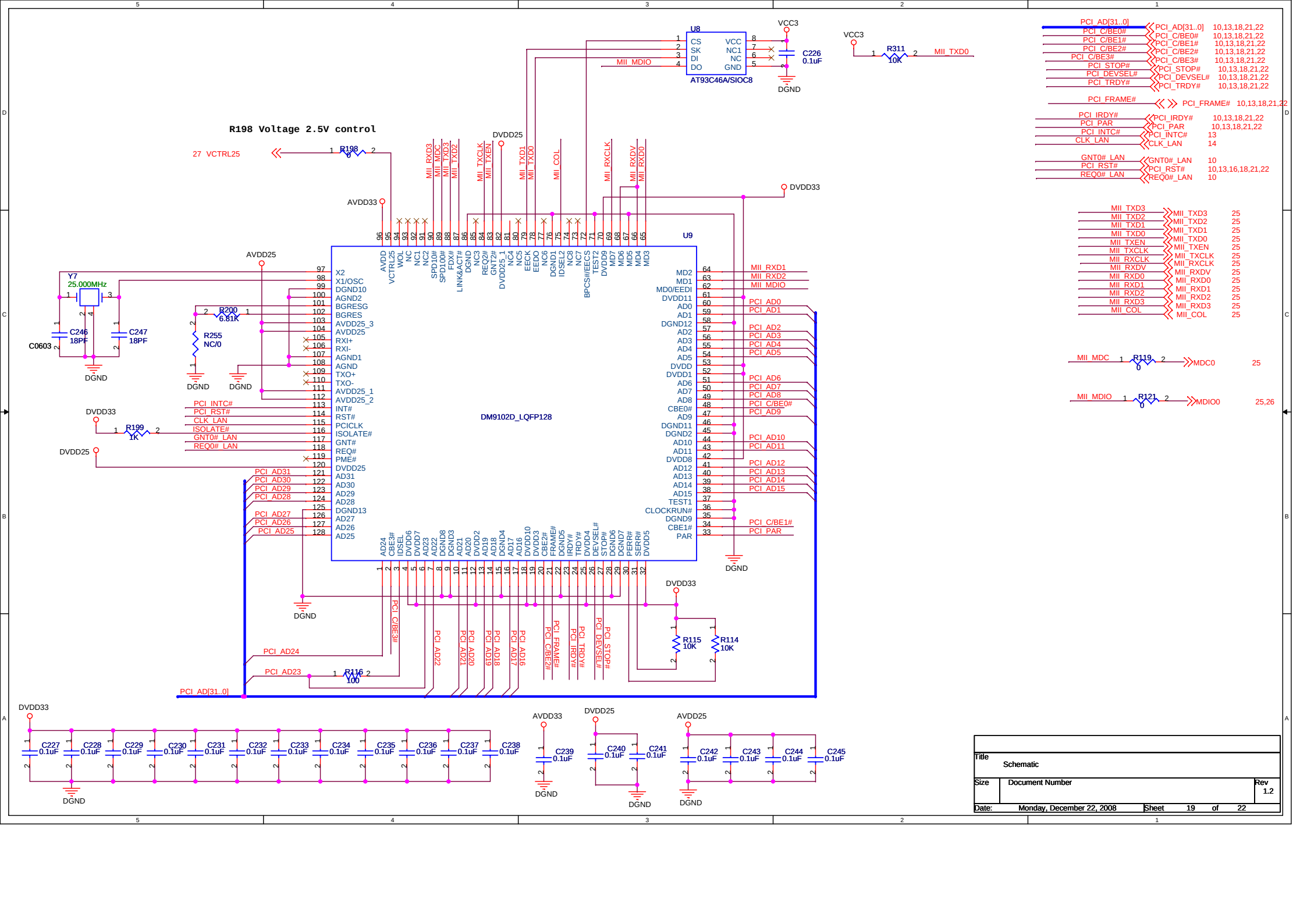
R198 Voltage 2.5V control
U8
AT93C46A/SIOC8
U9
DM9102D_LQFP128
VCC3
DVDD25
DVDD33
AVDD33
AVDD25
DGND
Y7
25.000MHz
C246 18PF
C247 18PF
C0603
R200 6.81K
R255 NC/0
R199 1K
R116 100
R311 10K
R115 10K
R114 10K
C226 0.1uF
R119 0
R121 0
27 VCTRL25
MII_MDIO
MII_TXD0
PCI_AD[31..0]
PCI_C/BE0#
PCI_C/BE1#
PCI_C/BE2#
PCI_C/BE3#
PCI_STOP#
PCI_DEVSEL#
PCI_TRDY#
PCI_FRAME#
PCI_IRDY#
PCI_PAR
PCI_INTC#
CLK_LAN
GNT0#_LAN
PCI_RST#
REQ0#_LAN
MII_TXD3
MII_TXD2
MII_TXD1
MII_TXD0
MII_TXEN
MII_TXCLK
MII_RXCLK
MII_RXDV
MII_RXD0
MII_RXD1
MII_RXD2
MII_RXD3
MII_COL
MII_MDC
MDC0
MDIO0
C227 0.1uF
C228 0.1uF
C229 0.1uF
C230 0.1uF
C231 0.1uF
C232 0.1uF
C233 0.1uF
C234 0.1uF
C235 0.1uF
C236 0.1uF
C237 0.1uF
C238 0.1uF
C239 0.1uF
C240 0.1uF
C241 0.1uF
C242 0.1uF
C243 0.1uF
C244 0.1uF
C245 0.1uF
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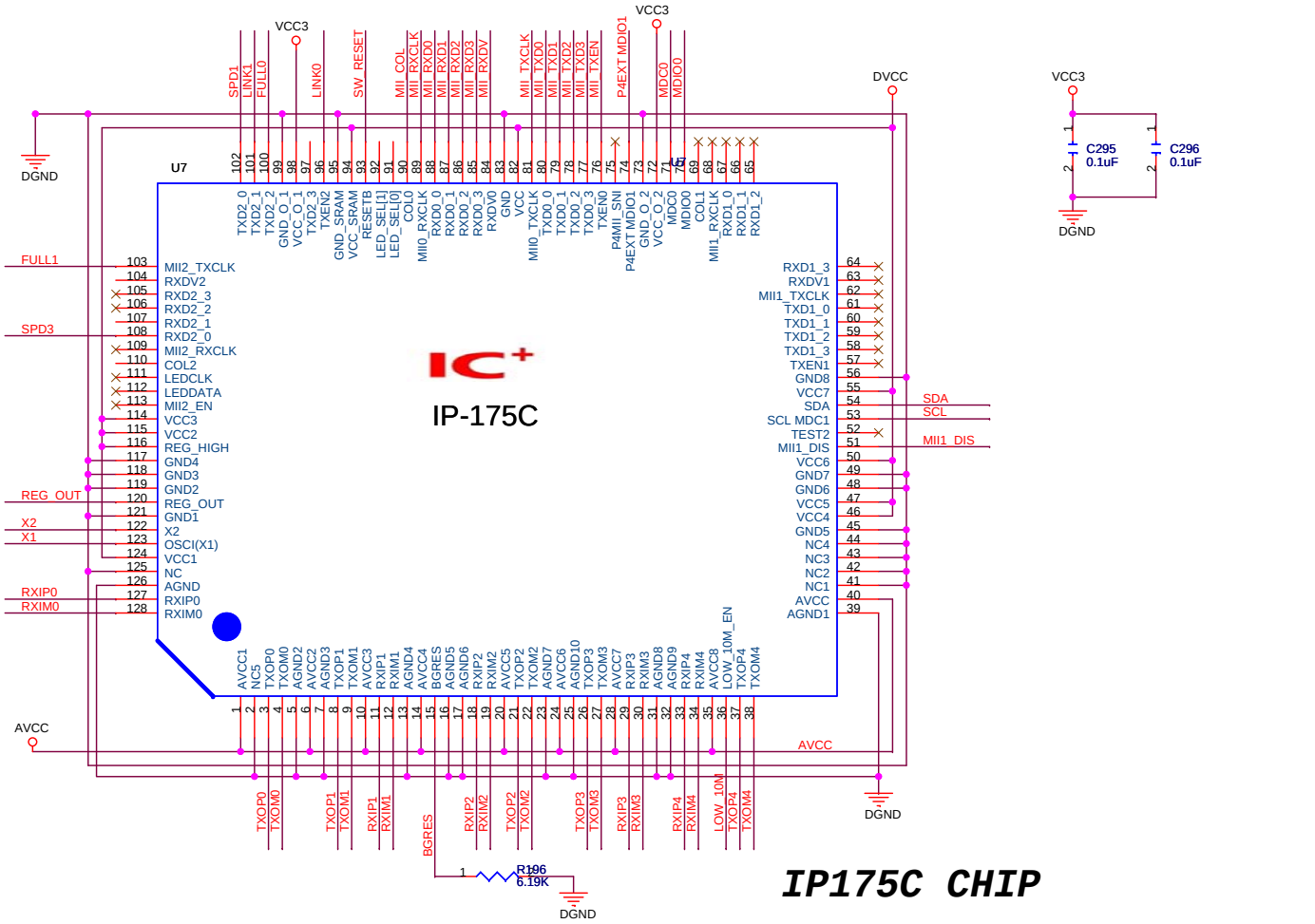
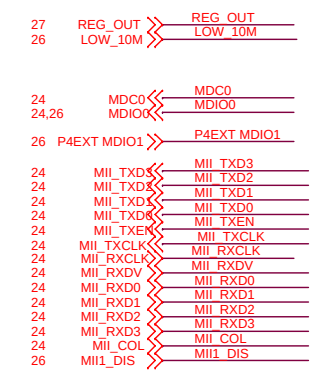
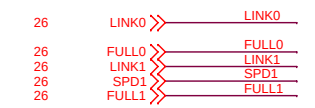
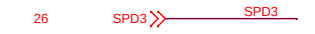
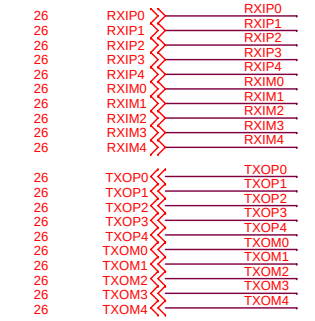


IP175C CHIP

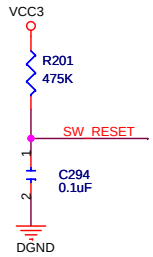




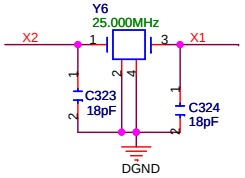




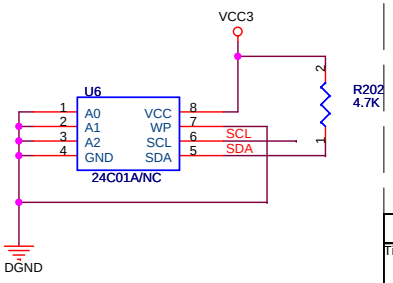
Signal Connect



RESET



CLOCK



EEPROM

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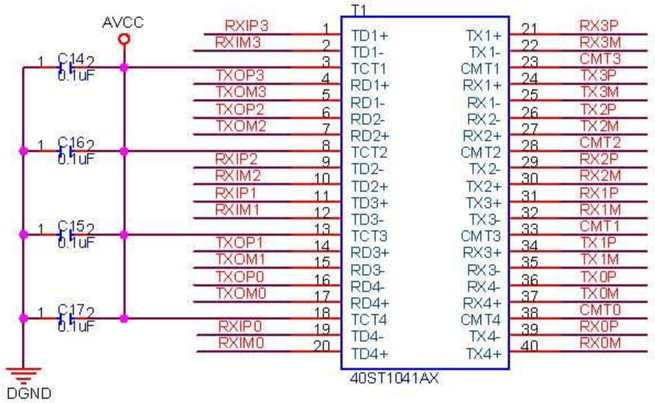

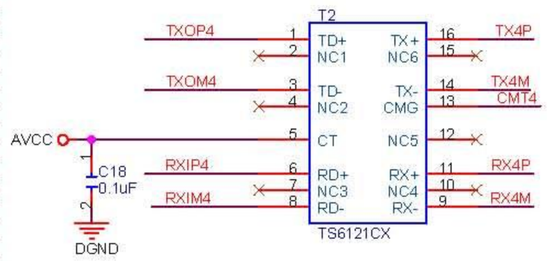

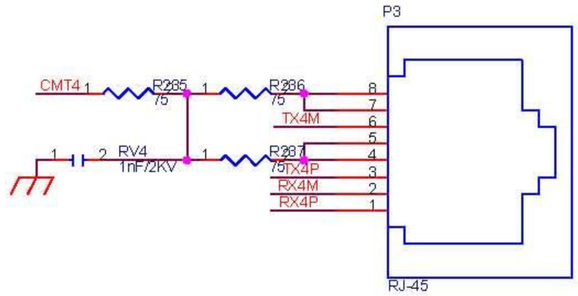

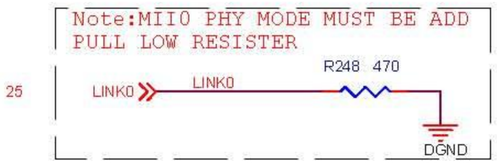

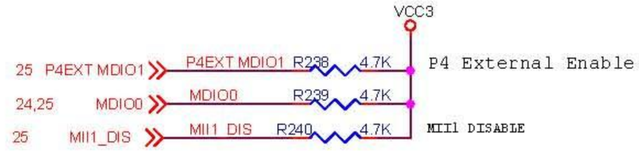

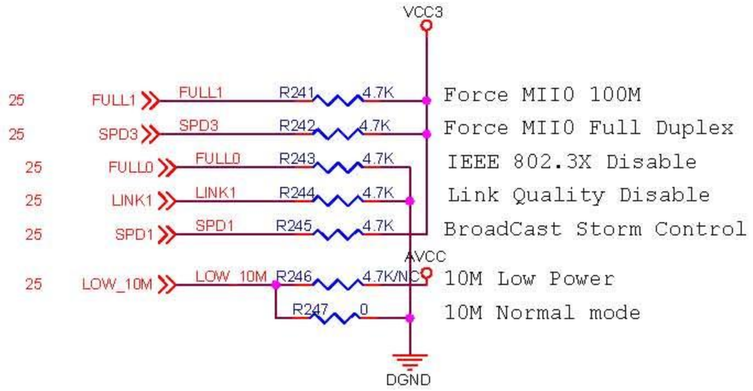

MDIX

TRANSFORMER&RJ45 CIRCUITS

Option Setting

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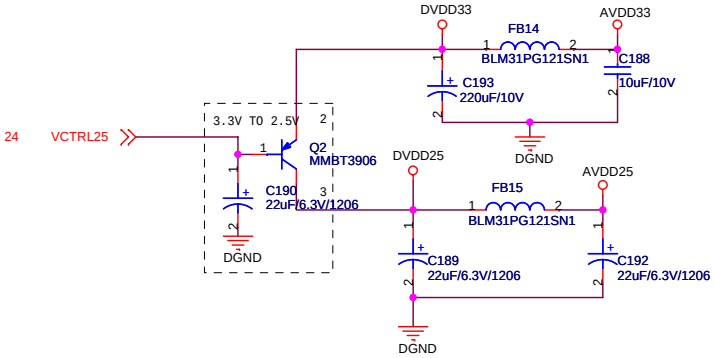

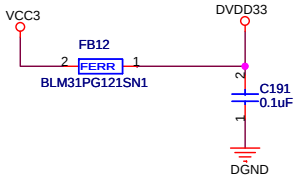

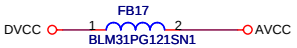

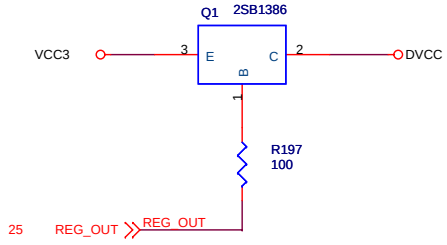

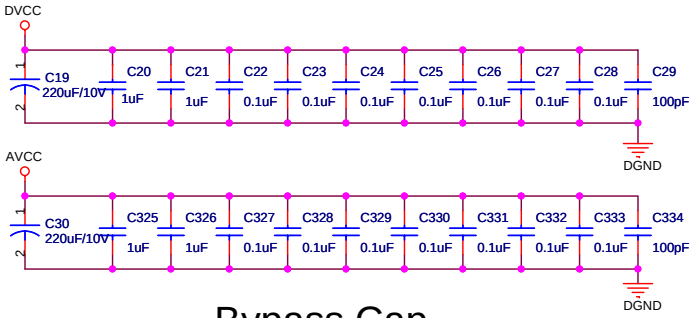

Bypass Cap.

POWER CIRCUITS

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