Datasheet

Scope

This technical document contains 3ALogics 13.56MHz Multi-Protocol Reader IC (TRH033M-S) features and structure.

Related 3ALogics Document

TRH03XM-S Cookbook

Firmware User Manual

Application

Access Control / Home Network & Digital Door Lock

POS Terminal / Public Transportation

Electronic Library / Intelligent Toys

E-Parking / Product Authentication

Distribution, Logistics

Revision history

Date	Version	CR	Revisor	Description
2009. 05. 26	0.1	01	S.H Chun S.W Kim W.C Kang	Preliminary version release
2010. 01. 06	1.0	02	S.H Chun S.W Kim W.C Kang	1.0 version release (Register description addition)
2010. 09. 30	1.0a	03	S.W Kim	Misprint modification
Dept. Manger : Sung Hun Chun **Authors :** Sung Hun Chun Sung Wan Kim Woo Cheol Kang(Jerry Kang)				**Title :** TRH033M-S Datasheet **Contents :** Chapter 1 ~ 14 Page : 98

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Contact

3ALogics Inc.
7th Floor, Hyundai-office Bldg., 9-4, Sunae-dong.
Bundang-gu, Seongnam-si, Gyeonggi-do, 463-783,Korea

TEL : (82)-(31)-715-7117
FAX : (82)-(31)-719-7551

homepage: http://www.3ALogics.com
E-mail : rfid@3ALogics.com

Printed in the Republic of Korea.

Document Contents

Chapter1 Introduction

1.1 Features

Basic information

- 13.56MHz Multi-protocol RFID Reader chip
- 3.3V operation voltage, 32pin LQFP Package
- Internal Card detector (include internal OSC: 50kHz)

Supported Protocols:

- ISO/IEC 14443 A/B Type, ISO/IEC 15693
- I-CODE (NXP), Tag-it (Texas Instrument), Jewel (Innovision), Felica (Sony)

Performs Analog and Digital mixed operation as standards indicated

- Modulation/Demodulation, Encoding/Decoding
- Framing and Collision Detection for Anti-collision
- Automatic Data integrity check

Functions for microprocessor interface

- 128 bytes FIFO buffer for immediate data storage
- 4 types of Parallel interface and SPI Serial interface
- Configurable interrupt can inform event to microprocessor
- Configurable and Adjustable timer function can cooperated with transceive state and interrupt

Power consumption minimization

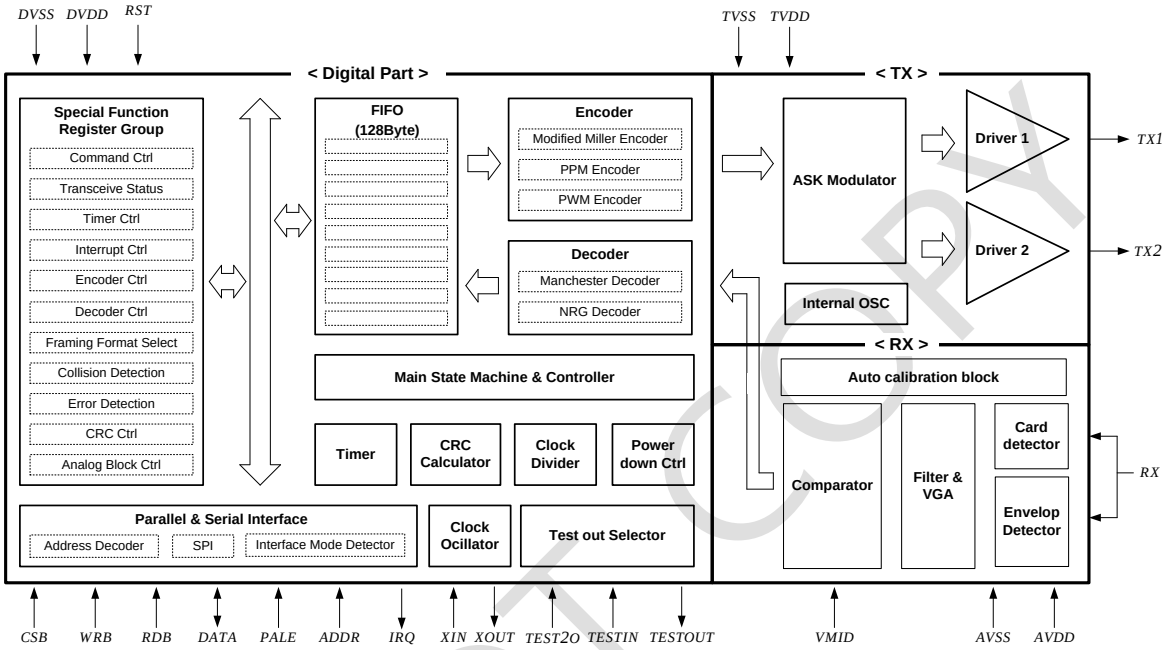
- Hardware/Software power down function
- Minimized leakage and stand-by current

Other functions

- Receiver auto calibration function (Offset cancellation)
- Transmit power and modulation index configuration
- Two Transmit drivers can be configured
- Adjustable receiver sensitivity depends on noise condition
- Data rate and pulse width configuration according to protocol standards
- Test pins for operation check, Supported Active communication

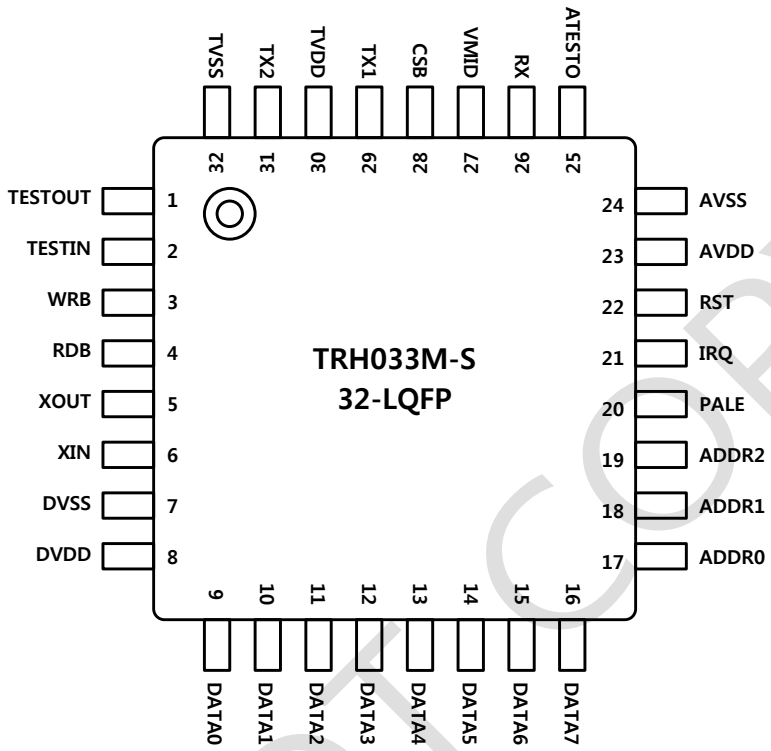
1.2 Block Diagram

Picture 1-1 displays TRH033M-S block diagram that is divided by digital and analog parts.



Picture 1-1 TRH033M-S Block Diagram

1.3 Pin Diagrams



Picture 1-2 TRH033M-S Pin Diagrams

1.4 Pin Description

Table 1-1 TRH033M-S Pin Map

Number	Pin Name	Description	Direction
1	TESTOUT	Test Output (for factory test)	Output
2	TESTIN	Test Input (for factory test)	Input
3	WRB	Write Bar (Active low)	Input
4	RDB	Read Bar (Active low)	Input
5	XOUT	Crystal Oscillator Output	Output
6	XIN	Crystal Oscillator Input	Input
7	DVSS	Digital Ground	Ground
8	DVDD	Digital Power	Power
9-16	DATA <0:7>	8-Bit Data Bus	Inout
17-19	ADDR <0:2>	3-bit Address Bus	Input
20	PALE	Positive Address Latch Enable (Active High)	Input
21	IRQ	Interrupt Request	Output
22	RST	Reset (Active High)	Input
23	AVDD	Analog Power	Power
24	AVSS	Analog Ground	Ground
25	ATESTO	Analog Test Output	Output
26	RX	Receiver Input (Analog)	Input
27	VMID	Receive Reference Voltage (Analog)	Output
28	CSB	Chip Select Bar (Active Low)	Input
29	TX1	Transmit Driver #1 (Analog)	Output
30	TVDD	Transmitter Power	Power
31	TX2	Transmit Driver #2 (Analog)	Output
32	TVSS	Transmitter Ground	Ground

1.5 Special Function Register Group

Table 1-2 TRH033M-S Special Function Register Group 1

Address	Name	Value							
0x00	PAGE	UsePage	0	0	0	0	PageSelect		
0x01	COMMAND	0	0	Command					
0x02	FIFODATA	FIFOData							
0x03	STATUS1	CdOut	ModemState			IRQ	ERR	HiAlert	LoAlert
0x04	FIFOLENGTH	FIFOLength							
0x05	STATUS2	TRunning	0	0	0	0	RxLastBits		
0x06	IEN	SetIEn	DtcIEn	TimerIEn	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn
0x07	IRQ	SetIRq	DtcIRq	TimerIRq	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq
0x08	RFU								
0x09	CONTROL	IrqPinInv	0	UseCRC	PowerDown	0	TStopNow	TStartNow	FlushFIFO
0x0A	ERRFLAG	FelCRC3	FelCRC2	FelCRC1	FIFOOvfl	CRCErr	0	ParityErr	CollErr
0x0B	COLLPOS	CollPos							
0x0C	TIMERVALUE	TimerValue							
0x0D	CRCRESULTLSB	CRCResultLSB							
0x0E	CRCRESULTMSB	CRCResultMSB							
0x0F	BITFRAME	0	RxAlign			0	TxLastBits		
0x11	TXCONTROL	TxPwdn	ModulatorSource		F100ASK	TX2Inv	TX2Cw	TX2RFEn	TX1RFEn
0x12	CWCONDUCTANCE	0	0	ExtraD	CwConductance				
0x13	MODCONDUCTANCE	0	0	ModConductance					
0x14	PROTOCOLSET	15693RxL	SpiMISOz	Fel424k	15693Anti	ProtocolSet			
0x15	MODWIDTH	0	0	ModWidth					
0x16	OFFWIDTH	TagItOFFWidthValue							
0x17	BFRAMING	Noguard	0	EOFWidth	CharSpacing			SOFWidth	
0x18	RFU								
0x19	RXCONTROL1	RxPwdn	VmidPwdn	RxForce	ComRefOff	0	VGAGain		
0x1A	RFU								
0x1B	RATE14443	0	0	0	LastpInv	Speed14443Tx		Speed14443Rx	
0x1C	RXTHRESHOLD	HysRangeCon		ComRefVolCon					
0x1D	JEWELCTRL	OneByteIns	0	RRDDSet				DRD	
0x1E	ETCCTRL	0	0	ZrAftColl	0	0	0	Dcdsrc	RxInv
0x1F	TAGITCTRL	0	TerrFlag	TadFlag	LockStatus		0	Tmask	TAddrSet
0x21	RXWAIT	0	0	RxWait					
0x22	REDUNDANCY	0	CRCWr	0	0	RxCRCEn	TxCRCEn	ParityOdd	ParityEn

1.6 Special Function Register Group (Continue)

Table 1-3 TRH033M-S Special Function Register Group 2

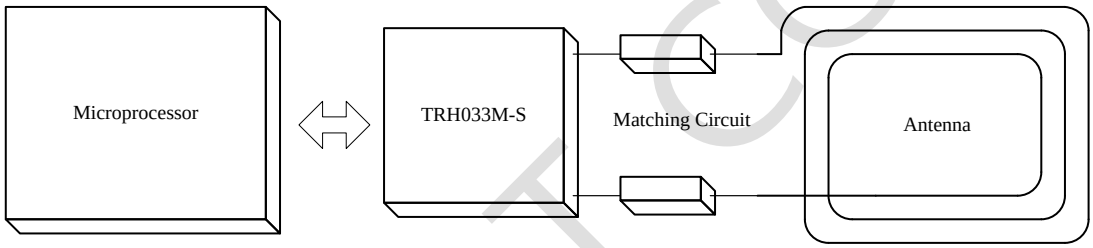
Address	Name	Value							
0x23	CRCPRESETLSB	CRCPresetLSB							
0x24	CRCPRESETMSB	CRCPresetMSB							
0x25	CALOFFSET	CardOffset				ReceiverOffset			
0x26	TESTOUTSEL	0	0	0	0	TestSel			
0x27	RFU								
0x29	FIFOLEVEL	0	0	WaterLevel					
0x2A	TIMERCLK	0	0	TRestart	TPreScaler				
0x2B	TCONTROL	0	0	0	0	TStopRxEnd	TStopRxBe	TStartTxEnd	TStartTxBe
0x2C	TRELOADVALUE	TimerReloadValue							
0x2D	DETECTCTRL	0	IrqClrEn	0	0	SelCalClk		DTCTX2En	DTCTX1En
0x2E	CALIR	CalibrationInstruction							
0x2F	DTCASTATR	DetectorStartTimerReload							
0x31	RFU								
0x32	DETECTLEVEL	AtestOutSel		CdRefVolCon					
0x33	CARDDTCREG	BgrR	RcvInv	CdInv	CdPwdn	IoscPwdn	1	0	CdOutR
0x34	FELPREAMBLE	0	0	FelicaPreambleCount					
0x35	DETECTIR	DetectInstruction							
0x36	DTRELOADH	DetectionTimerReloadHigh							
0x37	DTRELOADL	DetectionTimerReloadLow							
0x38	RFU								
0x39	MCLKONCNT	MainOscOnTimeCount							
0x3B	DTCTIMERV	DetectorTimerValue							
0x3C	RFONCNT	DetectorRFOnTimer							
0x3D	RFU								
0x3E	CARDDTCREG2	0	0	CdScanR					

Chapter2 TRH033M-S Functionality

2.1 Introduction

This chapter will explain RFID communication process and role of TRH033M-S instead of detailed functions of TRH33M-S.

2.2 RFID Reader



Picture 2-1 RFID Reader

Picture 2-1 displays 13.56MHz RFID reader structure using TRH033M-S. As displayed on picture, TRH033M-S is placed between antenna and microprocessor. TRH033M-S, from microprocessor, receives both command and data per each protocol format to tag through antenna. Receiving process works conversely. TRH033M-S converts data from the antenna by digitizing, and microprocessor verifies data received from TRH033M-S. Therefore, microprocessor communicates with RFID tag through TRH033M-S. In other words, TRH033M-S provides wireless communication interface between microprocessor and RFID tag.

2.3 Role of TRH033M-S

2.3.1 Modulation / Demodulation

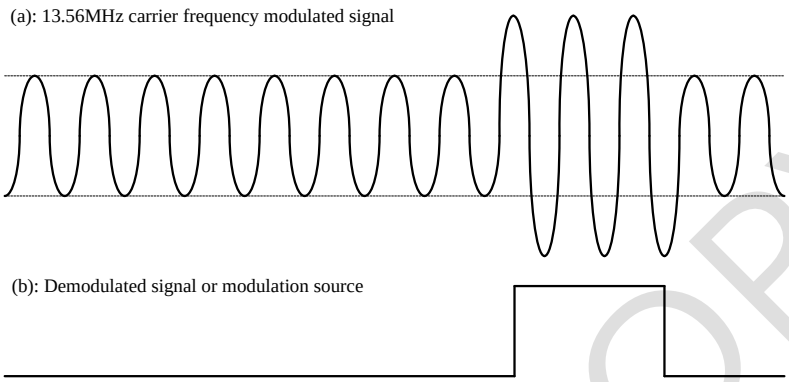
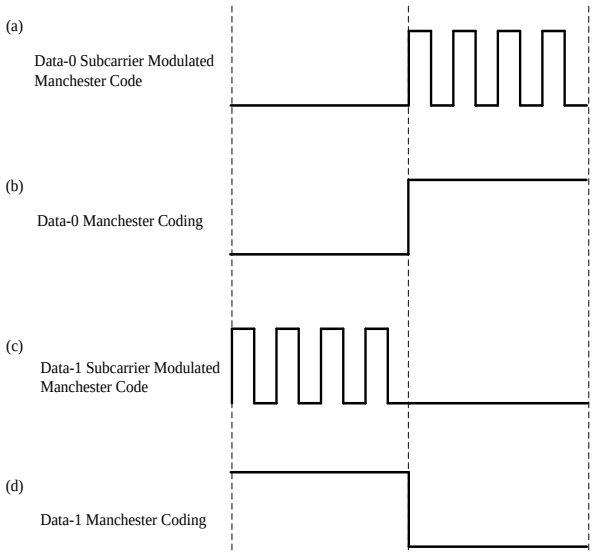


그림 2-2 Modulation / Demodulation

Key functions of TRH033M-S are modulation and demodulation. Modulation is sending data through carrier (as seen on picture 2-2 from (b) to (a)). Demodulation is conversely receiving signal (such as (a) on picture 2-2) by removing carrier and converting to (b). Therefore, modulation occurs in transmit mode (TX) and demodulation occurs in receiving mode (RX).

2.3.2 Encoding / Decoding



Picture 2-3 Encoding / Decoding

Picture 2-3 is an example of ISO/IEC 14443A type tag and reader encoding/decoding signal. Encoding/decoding process differs by different protocol used; therefore, detailed information should follow standard specification.

In RFID system, the sub-carrier(Picture 2-3) is usually used before sending coding data as carrier signal.

The decoder of TRH033M-S determines picture 2-3(b) under elimination process of sub-carrier as data 0 and picture 2-3(d) as data 1.

The completed data are stored in FIFO. In case of encoding, conversely, transmit data value stored in FIFO will impact the shape as seen on picture 2-3(a) and picture 2-3(c). All these processes will be performed automatically when user selects protocol type in TRH033M-S.

2.3.3 Framing

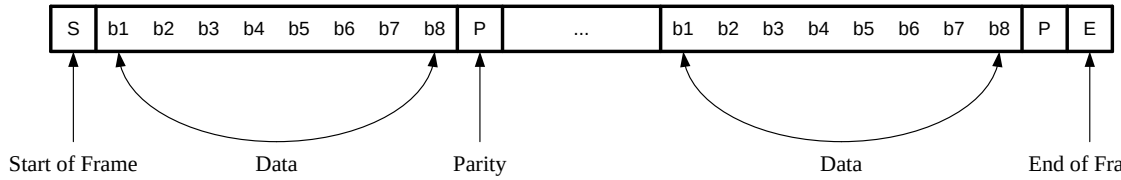


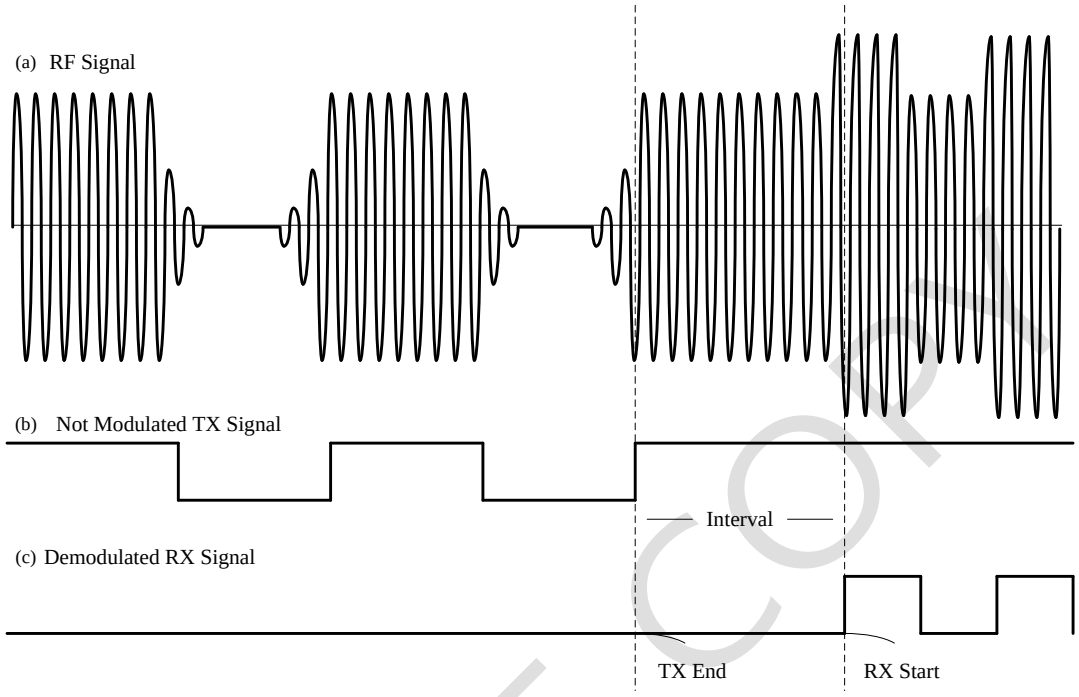
그림 2-4 Framing

Picture 2-4 displays ISO 14443A frame structure. Framing means simply making frame. Frame is data transmission unit in communication and word 'packet' is used very frequently. Frame structure differs based on each protocol, and TRH033M performs framing once user selects protocol type. Frame structure is simply divided into SOF (Start Of Frame) and EOF (End of Frame). For ISO14443A, parity is included after 8-bit data for data integrity.

2.3.4 Data integrity

Data integrity signifies data error status during transmitting/receiving. To check data integrity, ordinary protocols during transmit/receiving mode attaches surplus data for error checking. CRC is one of the major errors checking method. TRH033M has hardware check capability for CRC, parity error status check for data integrity during wireless interface. As other features, error checking is performed automatically by setting couple of features and result is sent to microprocessor through register.

2.3.5 Timer and Interrupt



Picture 2-5 Status of Tx/Rx signal

Interrupt and timer instruction is not fixed. Thus, user can freely utilize timer and interrupt in various methods. User can improve program efficiency by using timer and interrupt. The following is an example of program using interrupt and timer.

Picture 2-5 is end of TX and beginning of RX in RFID communication. Picture 2-5(a) is analog signal waveform from antenna, and picture 2-5(b) is a signal transmitting from digital part to analog part for modulation after encoding. Picture 2-5(c) is a received signal from analog part after demodulation. As seen on picture 2-5, there is a time delay between ending TX and beginning RX. Also TX and RX do not occur normally because it is not possible to receive response when tag is outside of antenna recognition distance. Therefore, software is developed for normal transmission, TRH033M-S will idle waiting for receiving signal when no response from tag. Therefore, timer and interrupt can be used more usefully in case of failing in receiving signal after transmission.

From above example using receiving interrupt and timer interrupt, if completing receiving it activates receiving interrupt. If signal is not received, the timer has to be set for interrupt not to occur after given time. Setting methods are as followed.

Set from IEN(0x06) to use timer interrupt and receive interrupt and set *TimerReloadValue* flag of TRELOADVALUE(0x2C) to applicable distance Interval as Picture 2-5. Lastly, set TCONTOL(0x2B) register to *TStartTxEnd*, thereafter, set the timer to count after signal transmission. From microprocessor normal completion of transmitting and receiving can be determined very simply by type of interrupt generated after completion of transmitting and receiving.

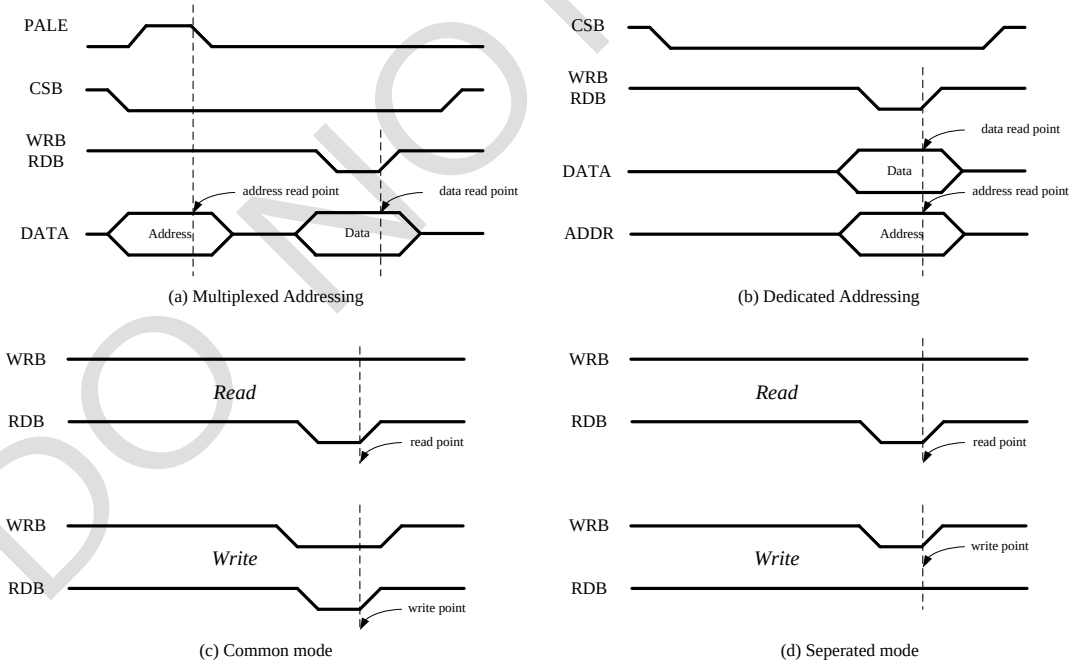
Chapter3 Host Interface

3.1 Introduction

Host typically means microprocessor. TRH033M-S supports 4 types of parallel interface and SPI serial interface to host.

3.2 Parallel Interface

TRH033M-S supports total of 4 types of parallel interface. All 4 interfaces support 8 bit data bus differentiated by read/write execution methods and allotted address methods. User can select any one of 4 interfaces that is more convenient and efficient. Picture 3-1 displays 4 interface types supported by TRH033M-S.



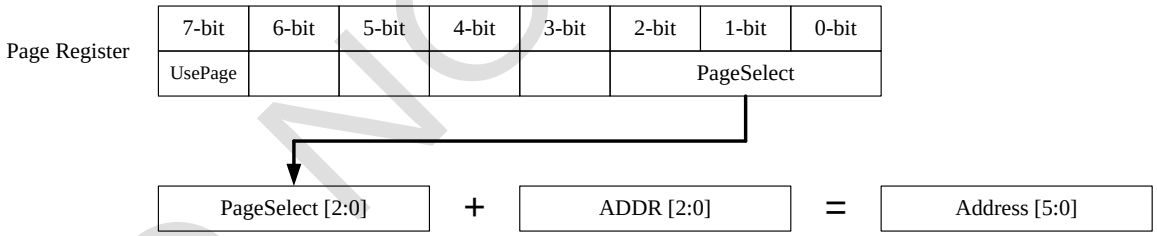
Picture 3-1 Shape of TRH033M-S supported microprocessor interface

There is 2 ways to delivery address. Picture 3-1(a) and picture 3-1(b) display the difference of Multiplexed Addressing and Dedicated Addressing. When using Multiplexed Addressing (Picture 3-1(a)), address is delivered through data bus. When address is read is determined by PALE pin. Dedicated Addressing is used by dividing data bus and address bus. Instead of using PALE pin, address is controlled by WRB and RDB pin.

Picture 3-1(c) and picture 3-1(d) are differences of Common Mode control method and Separated Mode control method. Differences of two methods are how to designate Read and Write using two pins, WRB and RDB In Common mode, WRB value being High implies Read and Low value implies Write. Also in Common Mode, Read/Write point is indicated when RDB falls to Low value in either Read/Write situation. For Separate Mode, Read/Write is allotted in each pin. WRB falling to Low value means Write, and RDB falling to Low value means Read.

3.2.1 Using Dedicated Address

Using Dedicated Address, address line constitutes in 3 bits, thus, not able to designate all TRH033M-S memory map having total 6 bits. Therefore, TRH033M-S utilizes low level 3 bits of PAGE(0x00) register to designate upper level 3 bits of address. MSB of PAGE(0x00) register is set to 1 when using PAGE(0x00) register low level bit for address. PAGE(0x00) register value is to set ADDR pin to all 0 and Write.



Picture 3-2 Dedicated Address Configuration

Picture 3-2 displays Dedicated Address configuration. ADDR implies data entered from TRH033M-S input pin, and Address implies to TRH033M-S last used address.

Table 3-1 PAGE register

Name	Address	Reset	Value							
PAGE	0x00	0x80	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			UsePage	0	0	0	0	PageSelect		

Number	Name	Description
7	UsePage	0: The PageSelect is not in use for register address setting. 1: The PageSelect is in use for register address setting.
2-0	PageSelect	If UsePage value is 1, upper level of register address 3 bit PageSelect value is used.

3.3 Parallel Interface Hardware Configuration

Parallel interface are divided into 4 different types by address allocation methods and control signal use methods. However, difference in control methods do not impact hardware configuration. Whether user selects Separated mode or Common mode, hardware configuration is the same and control method is determined using software. TRH033M-S control method is based on first executed write command after reset. Basically if separated mode is used to write after reset then until next reset Separate mode is used continuously.

Hardware configuration for address delivery method is as below. In case of Dedicated Address, PALE pin is not used. In Multiplexed, ADDR pin is not used. Table 3-2 displays each value when not using PALE or ADDR.

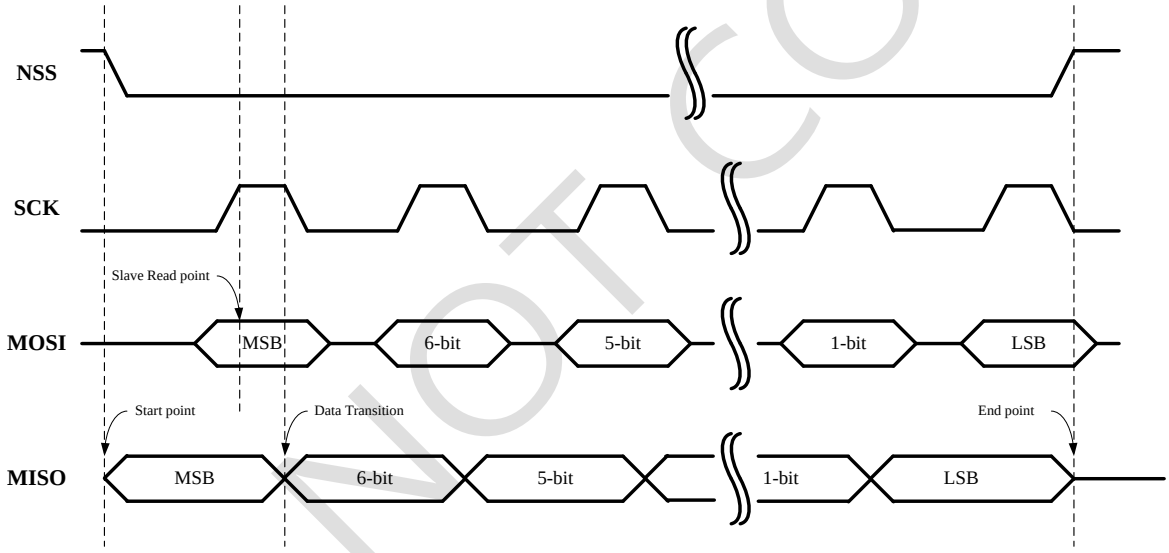
Table 3-2 Allocation of signal based on Addressing methods

PIN Name	Dedicated Address Bus	Multiplexed Address Bus
PALE	HIGH	PALE
ADDR2	ADDR2	LOW
ADDR1	ADDR1	HIGH
ADDR0	ADDR0	HIGH

3.4 SPI Serial Interface

TRH033M-S also supports SPI serial interface in addition to parallel interface. SPI (Serial Peripheral Interface) can send and receive data through 3 to 4 bus lines. TRH033M-S is ideal for small quantity bus control or control many TRH033M-S' with one microprocessor. SPI is divided by master and slave. Master gives commands from SPI protocol and slave follows the commands. TRH033M-S functions as slave during communication.

SPI clock (SCK) is created by master, and use MOSI (Master-Out Slave-In) during communication from master to slave and MISO (Master-Out Slave-In) during communication from slave to master. NSS (Negative Slave Select) is similar to Chip Select being used during one master controlling multiple slaves and wanting to select specific slave to set command.



Picture 3-3 SPI Serial interface operation

Picture 3-3 displays 1 byte (8bit) delivery process using SPI interface. To initiate SPI communication, first NSS need to change to Low value. MSB of MISO begins output from negative edge of NSS. Then, MOSI signal transfers from master to slave. Slave reads MOSI signal from positive edge of SCK. And data of MISO changes in negative edge of SCK. Up to this point is the process of 1 bit data transaction. Basically from positive edge of SCK enter 1 bit of data from master to slave, and from negative edge of SCK and negative edge of NSS slave outputs 1 bit of data to master. This process is repeated 8 times to send and receive 8 bits of data and completes 1 byte transaction. To send or receive more than 1 byte of data, maintain NSS to low and send and receive by byte. After all data is sent NSS returns to High value.

3.4.1 SPI Serial Interface Hardware Configuration

SPI interface, unlike parallel interface, is determined during reset process. Therefore, to use SPI modes, before sending reset signal assign inputs as below table 3-3.

Table 3-3 SPI SPI Interface Configuration

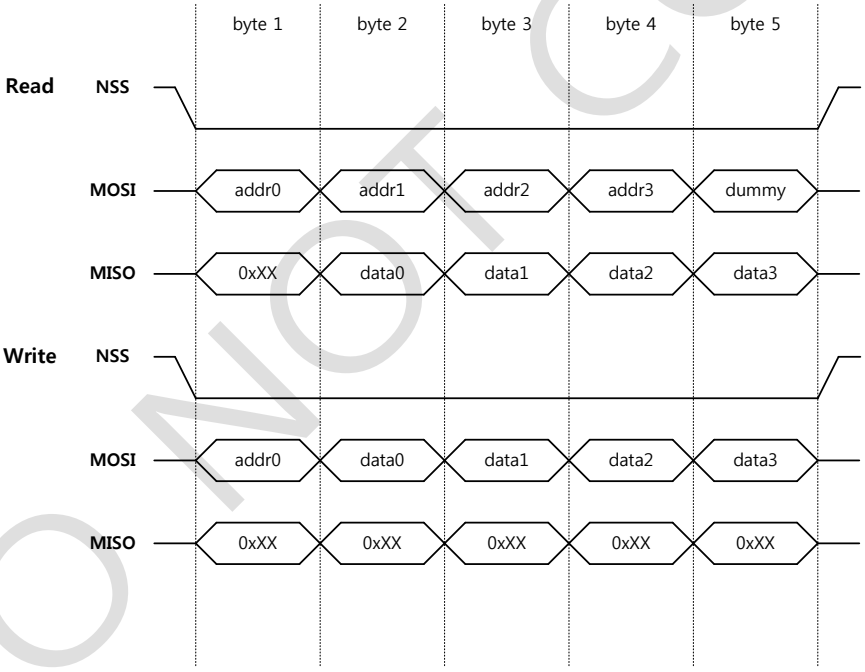
PIN Name	SPI Interface
PALE	NSS
ADDR2	SCK
ADDR1	LOW
ADDR0	MOSI
RDB	HIGH
WRB	HIGH
CSB	LOW
DATA7 … DATA1	1100001
DATA0	MISO

When using SPI interface, if more than 2 devices are connected to SPI line, setting *SpiMISOz* value of PROTOCOLSET(0x14) register bit 6 as 1 then MISO Pin is set as entered when TRH033M-S PALE value is High then more than 2 devices can be connected to communicate.

3.4.2 SPI Serial Interface Data Format

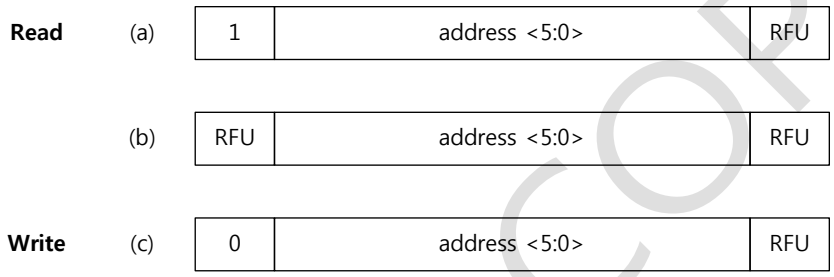
Picture 3-4 displays SPI command structure (Example: Master reading 4 registers). When executing Read command, master must send to slave the register address wanted to read. End byte is dummy thus to read 4 registers 5 bytes are entered. Consequently, to read n number of registers, user must enter n+1 number of bytes. Typically dummy uses 8 continuous 0 values. One additional point of caution is that after address input, data output occurs when next byte is entered. As seen in the picture, when addr1 is entered data0 output occur not data1.

In write command there is not output through MISO, but through MOSI, address and data types of signal should be entered. Entry steps are first byte recognizes as address, and before NSS becomes High, previously entered bytes are recognized as data. From the picture, data0 to data3 4bytes are written in address addr0. To execute write to other registers initialize NSS to High then change to Low and re-enter address then write data.



Picture 3-4 SPI Command Structure

In SPI communication determining whether it is Read or Write command depends on first byte of MSB. If first byte of MSB is 0 then it is Write command, and if 1 then it is Read command. If MSB is bit 7 and LSB is bit 0 then Read/Write is determined by MSB then address is located from bit6~bit1. Picture 3-5 is address structure for SPI communication. (a) is first address of Read command. Basically it is addr0 of Read command in Picture 3-4. As explained above MSB value is 1. (b) is address format from addr1 to addr3. MSB and LSB are all RFU. (c) is Write command address that is Write command addr0 in Picture 3-4. As explained above MSB value is 0. RFU is meaningless value and user can set it at his own discretion.



Picture 3-5 SPI Address Structure

Chapter4 Command

4.1 Introduction

TRH033M-S actions are initiated by commands. Writing command to address COMMAND(0x01) register, TRH033M-S functions based on current register setting value and FIFO data value.

4.2 Command Explanation

Table 4-1 displays commands available in TRH033M-S.

Table 4-1 COMMAND register

Name	Address	Reset	Value							
			7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
COMMAND	0x01	0x00	0	0	Command					

Number	Name	Description
5-0	Command	Register to store TRH033M-S executing commands. **IDLE (00h):** Remains in idle mode. (When writing command as 00, current executed function stops.) **TRANSMIT (1Ah):** Transmit data stored in FIFO and changes to idle mode. **RECEIVE (16h):** Store received data in FIFO and changes to idle mode. **TRANSCEIVE (1Eh):** Store new received data to FIFO after transmitting FIFO stored data then changes to idle mode. **FELICASLOT (2Eh):** Command for Felica Anti-collision. Store card response (3 times) received to FIFO after transmitting FIFO stored data. **CALFELICASLOT (24h):** Calibration + FELICASLOT command **CALTRANSCEIVE (14h):** Before executing Transceive command (1Eh), execute Calibration. **CARDDETECT (3Ah):** Command to check if tag is within RF field. For card detection, DETECTIR command is often used.

During TRH033M-S initiates, COMMAND(0x00) Register becomes *IDLE(00h)* status after oscillator stabilizated time. It comes to sleep status itself and if command *IDLE(00h)* command is used, IC comes to sleep mode.

Consequently TRH033M-S stays sleep mode when it doesn't execute at all. However, this command can activate by microprocessor unlike *INIT(3Fh).* When *IDLE(00h)* command is activated by microprocessor, it means discontinuing of any command in action. For example, when *RECEIVE(16h)* is being executed, writing *IDLE(00h)* to command register then TRH033M-S stops receiving and remains idle mode.

TRANSMIT(1Ah) command encodes FIFO stored data and after modulation, then transmits through TX1 and TX2 pins. When there is no data in FIFO, it does not transmit but remains in *IDLE(00h)* mode. *TRANSMIT(1Ah)* command sends no response command for test purpose at times.

RECEIVE(16h) command is a command to demodulate/decode response signal from antenna then stores in FIFO. This command also activates by microprocessor and used mainly for test purpose.

FELICASLOT(2Eh) command stores continuously received FELICA card response by slot to FIFO continuously. Received error result from stored data can be confirmed using FelCRC3, FelCRC2 and FelCRC1 of ERRFLAG(0x0A).

CALFELICASLOT(24h) command executes same function as *FELICASLOT(2Eh)*command but executes CALIBRATION first. Since it executes CALIBRATION first, always corrects receiving layer thus card reading is optimized.

CALTRANCEIVE(14h) command executes same function as *TRANSCEIVE(1Eh)* command but executes CALIBRATION first. Since it executes CALIBRATION first, always corrects receiving layer thus card reading is optimized.

CARDDETECT(3Ah) is the command to check if tag is detected within RF field. Card Detection function detects if tag exists before sending command. Thus, it helps decreasing power consumption by removing unnecessary transmission. To use this function, a couple of register should be set. Detail information are referred to the "TRH03XM-S CookBook".

4.3 Transmit/Receive Status Check

Microprocessor checks transmission status by reading TRH033M-S register. Not only execution of transmit/receive status but also error occurrence and other status checks are possible. Microprocessor occasionally checks information on TRH033M-S transmit/receive status and determines next course of action.

Table 4-2 STATUS1 register

Name	Address	Reset	Value							
STATUS1	0x03	0x01	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			CdOut	ModemState			IRQ	ERR	HiAlert	LoAlert

Number	Name	Description
7	CdOut	Result flag of Card Detector Enabled 0: Card not detected, 1: Card detected
6-4	ModemState	000: Idle - ready status. 001: TxSOF - transmitting the SOF(Start of flame). 010: TxData - transmitting data of FIFO buffer. 011: TxEOF - transmitting the EOF(End of flame). 100: GoToRx - starting receive. 101: PrepareRx - waiting till selected period in the RXWAIT register is expired. 110: AwaitingRx - waiting for the receiving signal. 111: Receiving - receiving the signal.
3	IRQ	Displays interrupt occurrence. Set interrupt use by utilizing IEN register.
2	ERR	Showing an error state. When ERRFLAG register value is 0 then ERR value is 0.
1	HiAlert	When FIFO stored data size is above certain level then value become 1.
0	LoAlert	When FIFO stored data size is below certain level then value become 1.

STAUS1(0x03) register is a register confirming overall transmit/receive status. Also current executed transmit/receive process can be verified by *ModemState* of STATUS1(0x03) register. One transmit Frame is configured by SOF(Start of Frame), data and EOF(End of Flame) following ISO/IEC standard. Through *ModemState* flag of STATUS1(0x03) register, can verify which step of Frame is being transmitted by transmitter. Table 4-2 explains definition by *ModemState* value.

IRQ flag of STATUS1(0x03) register obtain High value when interrupt occurs by IEN(0x06) register

setting. When interrupt request completes, it automatically changes to 0 value.

IRQ flag of STATUS1 (0x03) register performs always Active High irrelevant of *IrqPinInv* value. *ERR* flag of STATUS1(0x03) register becomes High value when any error occurs from ERRFLAG(0x0A) register. This flag as well as *IRQ* flag automatically clears when ERRFLAG(0x0A) register flags are cleared.

HiAlert and *LoAlert* flag of STATUS1(0x03) are registers to check data size in FIFO. For detailed explanations please referred "6.3.3 "

Table 4-3 STATUS2 register

Name	Address	Reset	Value							
STATUS2	0x05	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			TRunning	0	0	0	0	RxLastBits		

Number	Name	Description
7	TRunning	When timer is running value is 1. When stopped value is 0.
2-0	RxLastBits	When using ISO 14443A protocol, store valid bit quantity when Collision occurs.

STATUS2(0x05) register (same as STATUS1(0x03)) is a register to confirm activating status. STATUS2(0x05) register displays timer status. *TRunning* flag of STATUS2(0x05) register maintains 1 value even during timer counting.

*RxLastBits*flag indicates number of valid bits location of last byte received. For example, if conflict occurs in 6th bit after RECEIVE command, *RxLastBits* become 5 and valid bits become 5 bits. Every bits of last received byte are received normally, *RxLastBits* becomes 0. Please refer to "5.3 Anti-Collision".

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4.4 Control

CONTROL(0x09) register is a register to execute various functions. *PowerDown* of CONTROL (0x09) register leads TRH033M-S to Stand-by mode using software. During power down mode, TRH033M-S cannot execute transmit/receiving but power consumption is minimized. For detailed explanations, please refer to "9.3.2".

TStopNow and *TStartNow* flag are used to execute timer. When writing 1 to *TStartNow* flag, timer begins counting, and when writing 1 to *TStopNow* flag, timer counting stops. *FlushFIFO* function is to delete data remaining in FIFO buffer. When tag is not responding, noise can be a cause. Sometimes noise can be recognized as data and stored in FIFO. When transmit/receiving without deleting FIFO data, incorrect data caused by noise can be transmitted. Therefore, before storing transmitted data to FIFO, use *FlushFIFO* to delete all FIFO data and store data to be transmitted.

In *PowerDown,* when set as value 1, the value stays the same. However, *FlushFIFO, TStopNow* and *TStartNow* commands clear to 0 automatically. *IrqPinInv* bit is used to determine output phase of IRQ Pin. If the value is 0, it's Negative Polarity and this value is Default.

Table 4-4 CONTROL register

Name	Address	Reset	Value							
CONTROL	0x09	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			IrqPinInv	0	UseCRC	PowerDown	0	TStopNow	TStartNow	FlushFIFO

Number	Name	Description
7	IrqPinInv	Set Interrupt Pin(IRQ) Polarity 0: Negative Polarity 1: Positive Polarity
5	UseCRC	CRC calculation used by Default value(setting 0). 1: CRC PRESET Register used by CRC calculation Initial value.
4	PowerDown	Setting value to 1, internal power consumption is minimized and remains waiting mode. Transmitting, Receiving and Card detection all Power Down.
2	TStopNow	Setting this value to 1 will initiate timer count. This value automatically changes to 0.
1	TStartNow	Setting this value to 1 will stop timer. This value automatically changes to 0.
0	FlushFIFO	Delete all FIFO stored data. This value automatically changes to 0.

4.5 Error Check

ERRFLAG(0x0A) register is a register to check error during transmit/receiving.
It's used to check error response during *FelCRC3, FelCRC2* and *FelCRC1* Felica card anti-collision. When multiple cards are presented slot is determined for card response. CRC Error occurs when collision occurs thus Anti Collision Error occurrence can be determined by CRC Error.

If FIFO buffer data is full, then *FIFOOvfl* flag changes to value 1. When *FIFOOvfl* occurs, using *FlushFIFO* eliminates FIFO buffer data and *FIFOOvfl* error clears automatically. *CRCErr* displays CRC error during transmission, and *ParityErr* displays parity error for ISO/IEC 14443 type A.

These two value update automatically when Transceive command restart. *CollErr* flag sets when Collision error occurs. *CollErr* also as *ParityErr* and *CRCErr* automatically updates when command start. For detailed information on Collision, please refer to "5.3.1 ", and detailed information on *ParityErr* and *CRCErr*, please refer to"7.2 ".

표 4-5 ERRFLAG 레지스터

Name	Address	Reset	Value							
ERRFLAG	0x0A	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			FelCRC3	FelCRC2	FelCRC1	FIFOOvfl	CRCErr	0	ParityErr	CollErr

Number	Name	Description
7	FelCRC3	When executing Felica Protocol Anticollision, CRC Error occurs from 3rd response Slot Only applies when FELICASLOT command is used.
6	FelCRC2	When executing Felica Protocol Anticollision, CRC Error occurs from 2nd response Slot
5	FelCRC1	When executing Felica Protocol Anticollision, CRC Error occurs from 1st response Slot
4	FIFOOvfl	When FIFO data is overflow then value is 1.
3	CRCErr	When CRC Check error occurs then value is 1.
1	ParityErr	When Parity Check error occurs then value is 1.
0	CollErr	When Collision occurs then value is 1.

Chapter5 Protocol

5.1 Introduction

This chapter explains protocols (ISO/IEC 14443 A/B, ISO15693, Tag-It, Felica) and use methods supported by TRH033M-S. Changing protocols are done by changing registers related to protocols.

5.2 Data Format Select

To choose a protocol, user must select Transmit data format. Format implies Encoding method and Framing method and do not include Analog Modulation. TRH033M-S supports total 8 types of protocol and for ISO15693, 2 Encoding methods are available. Therefore, user can select up to 9 formats.

Table 5-1 PROTOCOLSET register

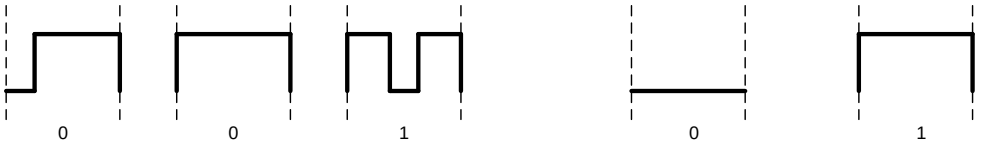
Name	Address	Reset	Value							
PROTOCOLSET	0x14	0x01	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			15693RxL	SpiMISOz	Fel424k	15693Anti	ProtocolSet			

Number	Name	Description
7	15693RxL	Determines 15693 receiving as Fast or Slow. 1: Slow, 0: Fast
6	SpiMISOz	If multiple devices are connected to SPI when using SPI interface, set as 1 and MISO output becomes off by NSS value.
5	Fel424k	Supports 424K Bps Mode of Felica Protocol. 0 – 212K bps Communication(supports all type of cards) 1 – 424K bps Communication (supports only specified cards)
4	15693Anti	When anti-collision of 15693 is operated, Collision detection from ID field of 2th bite should be carried out, without detection of first receiving flag collision 0 – Detect collision from first byte, COLLPOS. 1 – Detect collision from second byte, COLLPOS.
3-0	ProtocolSet	Set reader chip Protocol 0000: Set Protocol as ISO 14443B Type. 0001: Set Protocol as ISO 14443A Type. 1111: Set Protocol as ISO 15693 fast mode (1 out of 4 coding). 1110: Set Protocol as ISO 15693 standard mode (1 out of 256 coding). 1100: Set Protocol as Felica Type. 1000: Set Protocol as Jewel (Innovision) Type. 0100: Set Protocol as Tag-It (Texas Instrument). 0110: Set Protocol as ICODE fast mode. 0111: Set Protocol as ICODE standard mode. 1010: Set Protocol as ISO/IEC 14443A Type & Active RX mode

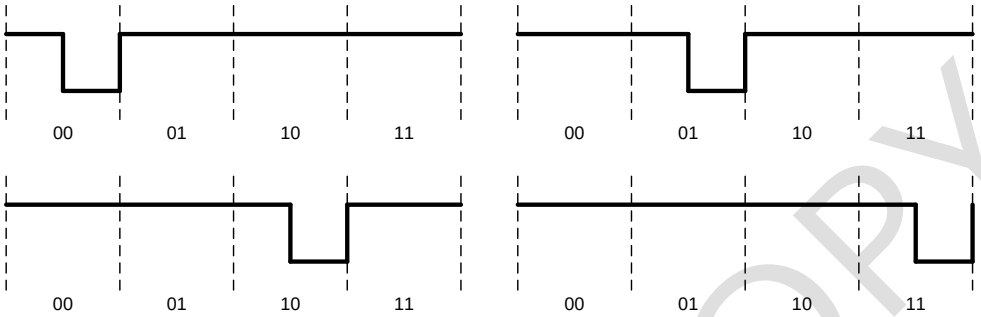
Using PROTOCOLSET(0x14) register protocol set *ProtocolSet* value, set protocol to read cards intended to use. Transmitting and receiving can be set using one protocol.

Table 5-2 Transmit data format by *ProtocolSet* value

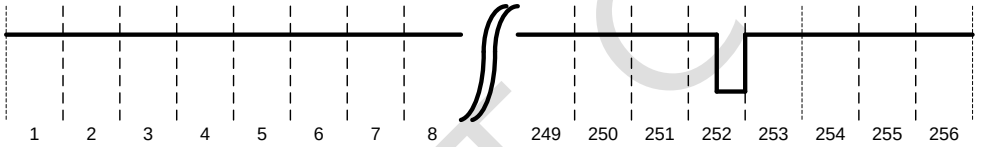
ProtocolSet	Standard	Format
0000	ISO/IEC 14443B	NRZ
0001	ISO/IEC 14443A	Modified Miller
1010	Active communication Proprietary standard (RF interface: ISO/IEC 14443A)	Modified Miller
1100	Felica Type	Manchester Code
1111	ISO/IEC 15693 (1out of 4 coding)	Pulse Position Modulation
1110	ISO/IEC 15693 (1 out of 256 coding)	Pulse Position Modulation
0110	I-CODE1 fast mode	Pulse Position Modulation
0111	I-CODE1 standard mode	Pulse Position Modulation
1000	Jewel Type	Modified Miller
0100	Tag-It	Pulse Width Modulation



(a) 14443A (b) 14443B



(c) 15693 (1 out of 4 coding)



(d) 15693 (1 out of 256 coding)

(d) Tag-It

Obverse amplitude Reverse amplitude

(e) Felica

Picture 5-1 Encoding method by protocol

Picture 5-1 displays Encoding method by protocol.

ISO/IEC 14443A type (Picture 5-1(a)) encode by Modified Miller form and two data formats to display 0.

ISO/IEC 14443B type (Picture 5-1(b)) is the most standard encoding method, NRZ coding. ISO/IEC 15693 two forms of PPM (Pulse Position Modulation) method to indicate data.

Picture 5-1(c) and Picture 5-1(d) display two Encoding method for ISO/IEC 15693. PPM format is a method of data value to tabularize as pulse location. Reader can select either one of these two formats, and tag responds by both data format.

Tag-It protocol use PWM (Pulse Width Modulation) method. PWM method distinguishes data by pulse length. Picture 5-1(e) Shows encoding method of Felica. Felica has obverse amplitude and reverse amplitude methods.

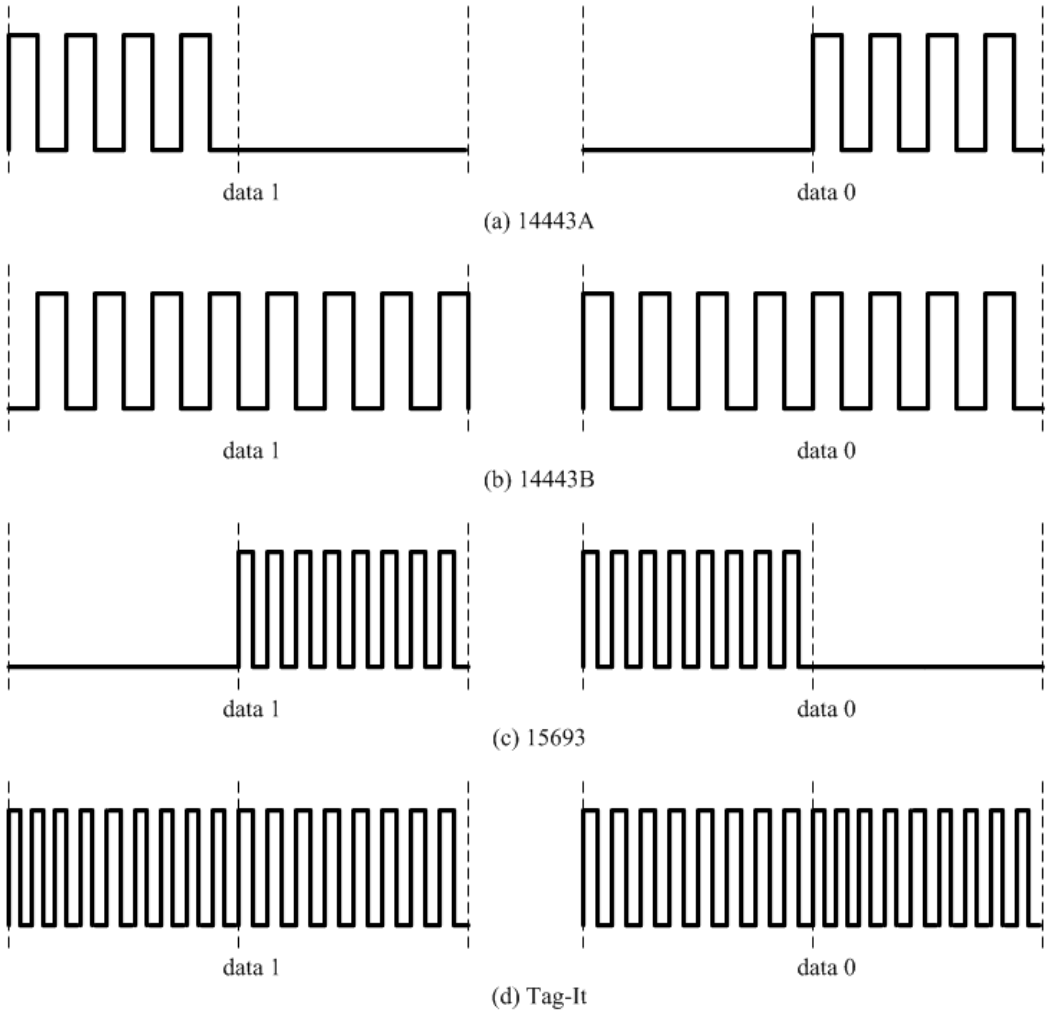
By PROTOCOLSET(0x14) Register value received data format is automatically selected. All protocols (except Felica) use sub carrier and they (except ISO14443B) use Manchester coding method.

ISO/IEC 14443A type and ISO/IEC 14443B type use 847 KHz subcarrier, and ISO/IEC 14443B type use BPSK modulation. BPSK modulation is a method changing phase 180° when data is changed. ISO/IEC 15693 use same format with ISO/IEC 14443A type, and subcarrier speed is half of ISO/IEC 14443A, 423 KHz.

For Tag-it, change subcarrier speed to tabularize data. For data 1, subcarrier changes from 484 KHz to 423KHz, and for data 0, changes from 423 KHz to 484 KHz conversely.

Felica uses Manchester coding method but it does not use sub-carrier like other protocols. Felica has obverse amplitude and reverse amplitude methods.

15693_FS flag is set to 1 when using ISO/IEC 15693 protocol in Fast mode. When using Fast mode, tag response data rate increases. To use Fast mode not only register value but also command flag must be changed.



Picture 5-2 Receiver data format by protocol

5.2.1 Receive Delay Time

RXWAIT(0x21) is a register to set the delay time between Transmitting and receiving signal. RXWAIT(0x21) enables block noise during delay time. However, if delay time is set too long than may not able to receive response from tag thus set the proper value through testing. Delay time is a value *RxWait* multiplied by 128/fc.

Table 5-3 RXWAIT register

Name	Address	Reset	Value							
			7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
RXWAIT	0x21	0x06	0	0	RxWait					

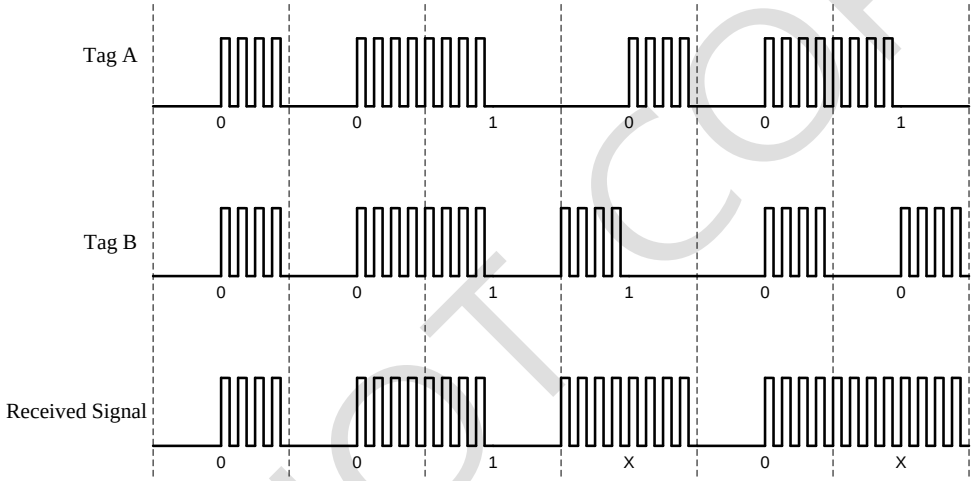
Number	Name	Description
5-0	RxWait	Setting the interval time after transmission before receiving.

5.2.2 Bit Level Receiving

Collision occurrence from tag during data receiving or if less than 1 byte data is received, to display the number of normal received bits from last received bytes, *RxLastBits* of STATUS2(0x05) register is used. *RxLastBits* are in 3 bits, and value are 0 when all bytes are Received normally.

5.3 Anti-Collision

If multiple tags are in RF field, all tags respond at same time, and tag signals are mixed in RF field making it difficult to distinguish data. Therefore, reader must read tags in RF field sequentially. In order to avoid tag collision, anti-collision algorithm is used. For ISO/IEC 14443B and ISO/IEC 15693 tag collision detection is required for anti-collision to function. However, ISO/IEC 14443A requires hardware detection of collision location and collision occurrence to activate anti-collision function. TRH033M-S has ability to detect collision and its location when collision occurs.



Picture 5-3 Collision Detection

5.3.1 Collision Detection

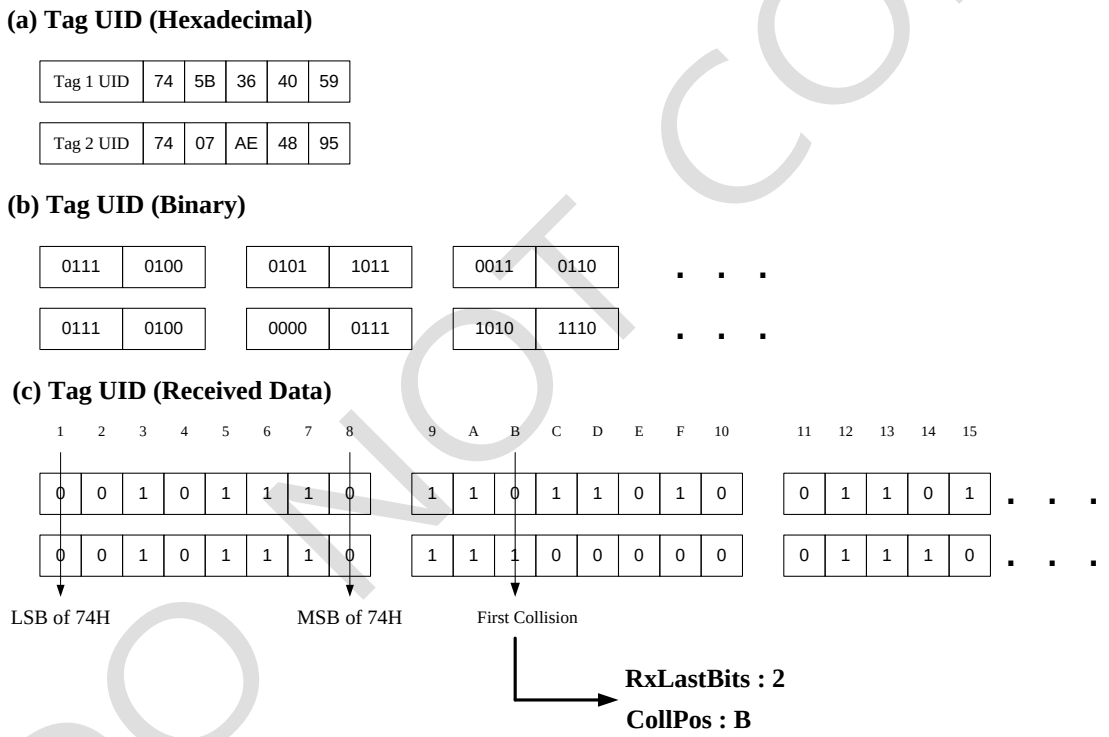
Picture 5-3 displays how TRH033M-S detects collision. Tag A and tag B have different value from 4th bit. When tag A and tag B have different value (as seen on picture 5-3), receiver cannot determine whether Received data is 0 or 1. When TRH033M-S receives a signal undetermined whether 0 or 1 (Seen as picture 5-3), location is stored at *CollPos* flag of COLLPOS(0x0B) register and set to 1 on *CollErr* flag of ERRFLAG(0x0A) register thus microprocessor can accomplish anti-collision functions. Parity bit is excluded from *CollPos* calculation.

Table 5-4 COLLPOS register

Name	Address	Reset	Value							
COLLPOS	0x0B	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			CollPos							

Number	Name	Description
7-0	CollPos	Indicate a position where first collision occurred.

When collision is detected *ZrAfColl* of ETCCTRL(0x1E) is set and all data after first collision are stored in FIFO as 0. This type of data processing is very convenient to develop software to handle anti-collision meeting ISO standard.



Picture 5-4 Register value during collision occurrence

Above picture 5-4 displays an example of two tags collision. Picture 5-4(a) is UID of two tags. First byte has same value of 74 but from second byte each value of 5B and 07 are given. Picture 5-4 (b) is tabularized UID in binary numbers. Picture 5-4(c) displays actual receiving steps. For ISO/IEC 14443A, LSB is received first and steps as picture 5-4(c) occurs. When TRH033M-S terminates receiving, collision occurs in 11th Received bit, therefore, *CollPos* flag value becomes B and *RxLastBits* value becomes 2.

If *ZrAfColl* is set as 1, 2nd byte is stored to FIFO as 03h and lower level 3 bytes are stored as 00h. If *ZrAfColl* is set to 0, data value after Collision becomes unpredictable value different from original UID.

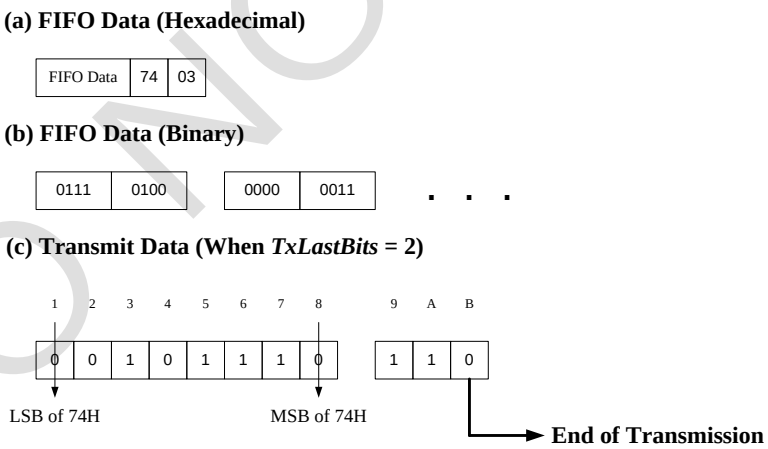
5.4 Bit Level data Transmit/Receive

Table 5-5 BITFRAME register

Name	Address	Reset	Value							
BITFRAME	0x0F	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	RxAlign			0	TxLastBits		

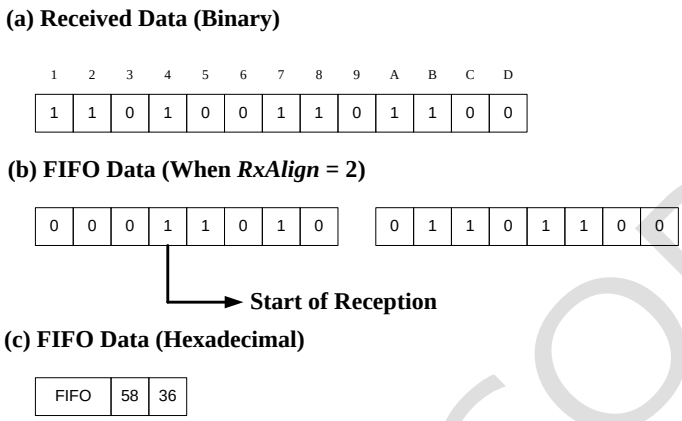
Number	Name	Description
6-4	RxAlign	Set where(bit) to store receiving data.
2-0	TxLastBits	Use when transmitting less than a byte. TxLastBits is a bit value for data to be transmitted.

TRH033M-S can Transmit/Receive data by bit level. For bit level Transmit, *TxLastBits* flag of BITFRAME(0x0F) register is used and for bit level receiving *RxAlign* flag is used.



Picture 5-5 Bit Level Transmit

Above picture 5-5 displays bit level Transmit. If FIFO stored data is same as picture 5-5(a), data is tabularized in binary numbers as seen in picture 5-5(b). If *TxLastBits* is set to 2 and Transmit command carries out, then first byte 74 is all transmitted and second data 03 is transmitted up to 3 bits.



Picture 5-6 Bit Level Receive

Picture 5-6 displays bit level Receiver steps. When Receiver data (On picture 5-6(a)) *RxAlign* value is set to 2, data is stored in FIFO as picture 5-6 (b) beginning 4th bit. Picture 5-6(c) displays hexadecimal data stored in FIFO.

5.5 Protocol

This section describes each protocol and related register functions.

5.5.1 ISO/IEC 14443A Protocol

ZrAfColl flag is used for ISO14443A type. When *ZrAfColl* flag is set to 1, all data received after collision error is stored to FIFO as 0. This feature allows ISO14443A Anti-Collision process very simple.

Table 5-6 ETCCTRL register

Name	Address	Reset	Value							
ETCCTRL	0x1E	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	0	ZrAftColl	0	0	0	Dcdsrc	RxInv

Number	Name	Description
5	ZrAftColl	Setting to 1 allows all received card response after collision as 0.
1	Dcdsrc	Use to define input signal of receiver decoder logic. 0: Use response signal from card as input. 1: Use signal through TESTIN pin as input.
0	RxInv	0: normal operation 1: Invert receiving signal as decoder block. According to protocol, inversion is much more efficient.

Dcdsrc is a flag to determine which signal to decode. When *Dcdscr* is 0, signal from receiver is decoded and when it is 1, signal from TESTIN pin is decoded. Signal received from TESTIN pin is decoding function testing purpose and typically is set to 0 when used for transmit/receive purpose.

RxInv is a control signal to invert phase of response received from card. Not for typical operation but mostly used for testing methods.

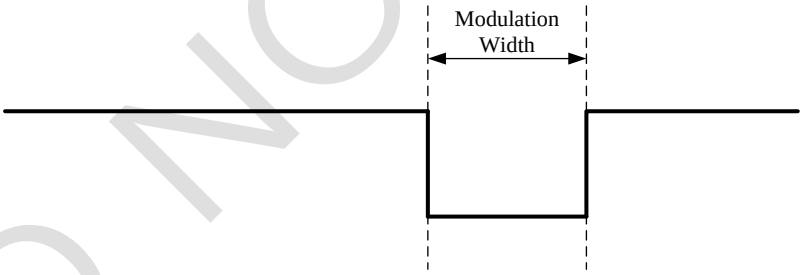
Modulation Width Changes

ISO/IEC 14443A type protocol communication from reader to tag utilize 100% ASK Modulation and Modified Miller coding method. Modified Miller tabularize data value by pulse location, and TRH033M-S allows functionality to adjust pulse width. *ModWidth* flag of MODWIDTH(0x15)register is used for 14443A type pulse width adjustment in transmit signal.

Table 5-7 MODWIDTH register

Name	Address	Reset	Value							
			7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
MODWIDTH	0x15	0x10	0	0	ModWidth					

Number	Name	Description
5-0	ModWidth	Set 100% modulation width for ISO14443A T_{mod} = 2(ModWidth_Dec+1) X (1/f_c) EX) 1/fc = 1/13.56MHz = 73.7nsec ModWidth_Hex = 10 → ModWidth_Dec = 16 **MODWIDTH(0x15) = 0x10, Tmod = 2(16+1) X 73.7n = 2.5usec



Picture 5-7 Modulation Width

Table 5-8 OFFWIDTH register

Name	Address	Reset	Value							
			7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
OFFWIDTH	0x16	0x7A	TagItOFFWidthValue							

Number	Name	Description
7-0	TagItOFFWidthValue	It is used in regulating the length of pause duration when transmitting command in 15693 or Tag-it Protocol operation. Default value setting.

5.5.2 ISO/IEC 14443B Protocol

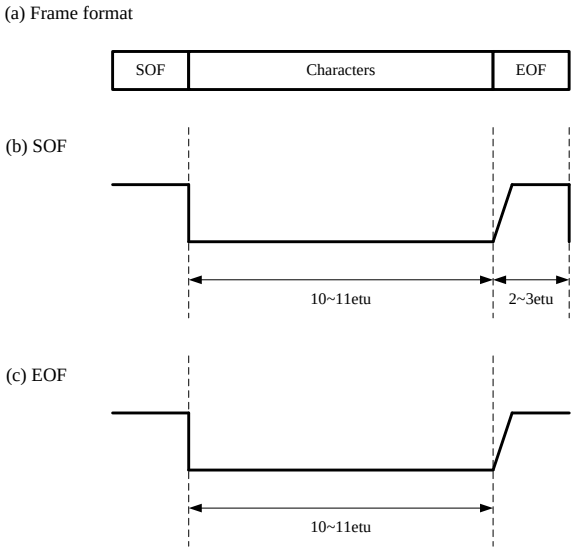
ISO/IEC 14443B Type Frame Setting

TRH033M-S contains functionality for frame adjustment using ISO/IEC 14443B type protocol.
In case of ISO/IEC 14443B type, SOF, EOF and EGT length in frame are set. Through BFRAMING (0x17) register user can adjust values within specification.

Table 5-9 BFRAMING register

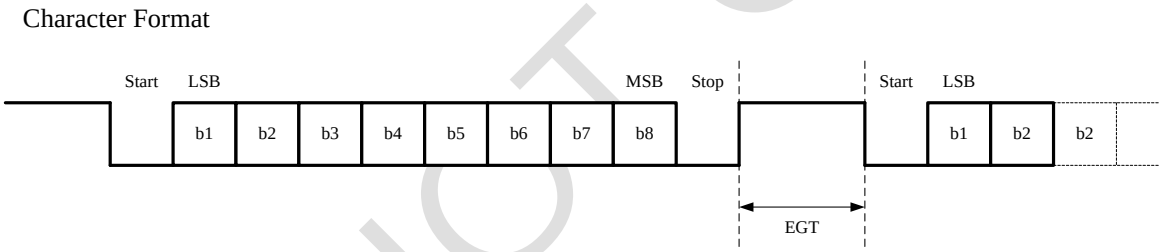
Name	Address	Reset	Value							
BFRAMING	0x17	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			Noguard	0	EOFWidth	CharSpacing			SOFWidth	

Number	Name	Description
7	Noguard	Setting to 1 is decoding with 14443B type card response without extra-guard time. Setting to 0 is decoding with extra-guard time. Depending on 14443 B Type noguard can be set differently thus in actual use case guard value can be set if card type is determined. However variety of B Type cards are being used then set guard as 1 to read card and set as 0 to read each once to read all types of cards.
5	EOFWidth	0: Set the EOF to length of 10 ETU. 1: Set the EOF to length of 11 ETU.
4-2	CharSpacing	Set EGT width. Set in 128 / fc multiples.
1-0	SOFWidth	00: Set the SOF to length of 10 ETU Low 2 ETU High. 01: Set the SOF to length of 10 ETU Low 3 ETU High. 10: Set the SOF to length of 11 ETU Low 2 ETU High. 11: Set the SOF to length of 11 ETU Low 3 ETU High.



Picture 5-8 Length of SOF and EOF

Picture 5-8 displays SOF and EOF used in ISO/IEC 14443B type. Picture 5-8(a) is frame architecture of ISO/IEC 14443B type. Frame begins with SOF and ends with EOF, and characters are located in between. Picture 5-8(b) displays form of SOF. SOF is a signal with low section length is 10~11etu and high section length is 2~3etu. This value can be adjusted through *SOFWidth* flag. Picture 5-8(c) displays EOF signal. EOF length is 10~11etu and can be adjusted using *EOFWidth* flag.



Picture 5-9 Length of EGT

Picture 5-9 explains EGT(extra guard time). Same as picture 5-8, character comprise of start bit and stop bit with total of 8 binary data. Delay time between two characters is called EGT. From specification EGT value is 0~57us when transmitting and 0~19us when receiving. User can adjust EGT length by 128/fc using *CharSpacing* flag of BFRAMING(0x17) register.

The standard data rate of ISO/IEC 14443 is 106kbps. But as shown as table 5-10, data rate will be able to be adjusted upward in case of high speed data rate supported card.

Table 5-10 RATE 14443 register

Name	Address	Reset	Value							
RATE14443	0x1B	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	0	0	LastpInv	Speed14443Tx		Speed14443Rx	

Number	Name	Description
4	LastpInv	Last parity bit inverting
3-2	Speed14443Tx	Transmitter speed select 00: 106kbps (default) 01: 212kbps 10: 424kbps 11:848kbps
1-0	Speed14443Rx	Receiver speed select 00: 106kbps (default) 01: 212kbps 10: 424kbps 11:848kbps

5.5.3 JEWEL protocol

Jewel is a tag protocol developed by Innovision that is quite similar to ISO/IEC 14443A. TRH033M-S use JEWELCTRL(0x1D) register to support Jewel protocol. Table 5-11 is explanation of JEWELCTRL(0x1D) register.

Table 5-11 JEWELCTRL register

Name	Address	Reset	Value							
JEWELCTRL	0x1D	0x55	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			OneByteIns	0	RRDDSet				DRD	

Number	Name	Description
7	OneByteIns	Set to 1 when using command with 1 byte.
5-2	RRDDSet	Set Reader-Reader Data Delay time as stated in standard document. Use default value.
1-0	DRD	Set Device Response Delay time as stated in standard document. Use default value.

5.5.4 TAG-IT protocol

TAG-IT suggested by Texas Instrument is the protocol quite similar to ISO/IEC 15693. TRH033M-S use TAGITCTRL(0x1F) register to support TAG-IT protocol. Table 5-12 is explanation of TAGITCTRL(0x1F) register.

Table 5-12 TAGITCTRL register

Name	Address	Reset	Value							
TAGITCTRL	0x1F	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	TerrFlag	TadFlag	LockStatus		0	Tmask	TAddrSet

Number	Name	Description
6	TerrFlag	Error in tag response Field Flag is stored in case of setting Tag-It protocol.
5	TadFlag	Address Flag in tag response Field is stored in case of setting Tag-It protocol.
4-3	LockStatus	Lock Status of memory block Field in Get Block Response is stored at the time of Tag-It protocol operation.
1	Tmask	It is used in setting Tag-It protocol and Mask Bit in SID Request command. When Mask Length value is stored in TxLastBits, then only selected Mask value is transmitted to Tag-It tag at the time of data transmission in FIFO.
0	TAddrSet	Set Taddr Field value in Tag-It protocol operation.

5.5.5 FELICA protocol

FELICA is a tag protocol suggested by SONY.

Table 5-13 FELPREAMBLE register

Name	Address	Reset	Value							
FELPREAMBLE	0x34	0x2F	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	0	FelicaPreambleCount					

Number	Name	Description
5-0	FelicaPreambleCount	The register that sets Preamble size in case of Felica Protocol operation. When default value (2F) is used, some cards used to increase Preamble value.

Chapter6 FIFO Buffer

6.1 Introduction

TRH033M-S has 128-Byte FIFO buffer. This FIFO buffer stores data temporarily while data transfer between microprocessor and TRH033M-S.

When microprocessor orders transmit command after writing data to FIFO buffer, data stored in FIFO is transmitted. And receive command is as well FIFO related functions, as same as other TRH033M functions, are executed through register.

6.2 FIFO Buffer Data Input/Output

FIFO buffer input/output is accomplished using FIFODATA(0x02) register. Microprocessor write to FIFODATA(0x02) register the data to be transmitted and read data received through FIFODATA(0x02) register. FIFODATA(0x02) register outputs first data stored in FIFO. Again, FIFODATA(0x02) register read data sequentially based on first in first out basis.

Table 6-1 FIFODATA register

Name	Address	Reset	Value							
			7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
FIFODATA	0x02	0xXX	FIFOData							

Number	Name	Description
7-0	FIFOData	FIFO buffer input/output register

X: don't care

FIFOLength flag of FIFOLENGTH(0x04) register is a register expressing FIFO buffer stored data in byte level. *FIFOLength* flag comprises of 7 bits to express up to 128 bytes.

Table 6-2 FIFOLENGTH register

Name	Address	Reset	Value							
FIFOLENGTH	0x04	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	FIFOLength						

Number	Name	Description
6-0	FIFOLength	Show the number of bytes stored in the FIFO buffer.

6.3 FIFO Buffer Related Function

6.3.1 FIFO Buffer Data Deletion

FIFO buffer data can be deleted by *FlushFIFO* flag of CONTROL(0x09) register. Finally FIFOLENGTH(0x04) becomes 0 and FIFO can store up to 128 bytes. *FlushFIFO* command allows inaccurate data deletion due to noise before transmit/receive function.

6.3.2 FIFO Buffer Error

When data is full in FIFO buffer, error occurs and sets *FIFOOvfl* of ERRFLAG(0x0A) register to 1. *FIFOOvfl* error can be cleared using *FlushFIFO* command.

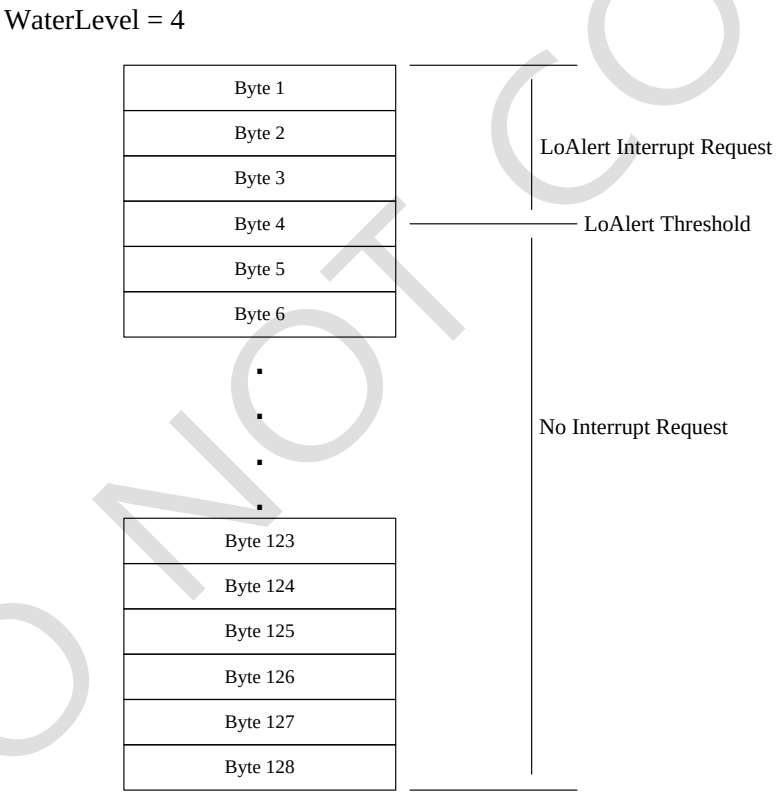
6.3.3 FIFO Buffer caused Interrupt

There can be interrupts due to TRH033M-S FIFO buffer stored data quantity, and these interrupts occurs by *WaterLevel* flag of FIFOLEVEL(0x29) register value.

Table 6-3 FIFOLEVEL register

Name	Address	Reset	Value							
FIFOLEVEL	0x29	0x08	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	0	WaterLevel					

Number	Name	Description
5-0	WaterLevel	Set HiAlert and LoAlert alert level. HiAlert occurs when FIFO available space is below WaterLevel. LoAlert occurs when FIFO stored data quantity is below WaterLevel.



Picture 6-1 WaterLevel value interrupts

Picture 6-1 displays FIFO buffer stored data quantity and interrupt occurrence due to *WaterLevel* value. Total of 128 bytes can be stored in FIFO. *LoAlert* interrupt occurs when FIFO data is less than *WaterLevel* specified value and *HiAlert* interrupt occurs when less space is available in FIFO then *WaterLevel* specified value. Other occasions, interrupt do not occur.

Chapter7 Signal Integrity

7.1 Introduction

Wireless communication has number of insecure elements. Electromagnetic waves from other peripherals, natural environment changes and other elements impact communication error. Therefore, all protocols contain methods to detect error, and TRH033M-S provides error correction methods by hardware.

7.2 Signal Integrity Setting Method

Table 7-1 Signal integrity check method by Protocol and its register setting method

Protocol Type	Redundancy Check Method	ParityOdd Flag	ParityEn Flag
ISO 14443A	16-bit CRC (ISO 14443A), Odd Parity	1	1
ISO 14443B	16-bit CRC (ISO/IEC3309)	0	0
ISO 15693	16-bit CRC (ISO/IEC3309)	0	0
Felica	16-bit CRC (ISO/IEC3309)	0	0
Tag-It	16-bit CRC (ISO/IEC3309)	0	0

Table 7-1 tabularizes signal integrity checking method by protocol and its register setting methods. *ParityEn* flag of register REDUNDANCY(0x22) is a flag to determine parity check use.

ParityOdd flag determines to use Odd parity or Even Parity.

As seen on above table, all protocols except ISO/IEC 14443A type do not use parity error check method and also CRC type use different format for ISO/IEC 14443A type.

표 7-2 REDUNDANCY 레지스터

Name	Address	Reset	Value							
REDUNDANCY	0x22	0x03	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	CRCWr	0	0	RxCRCEn	TxCRCEn	ParityOdd	ParityEn

Number	Name	Description
6	CRCWr	Store received CRC value on FIFO.
3	RxCRCEn	Processing CRC calculation for received data.
2	TxCRCEn	Adding CRC calculation for transmission data.
1	ParityOdd	Setting Parity calculation. ISO 14443 A-type only. 0: Even Parity 1: Odd Parity
0	ParityEn	Setting parity checking. ISO 14443 A-type only.

CRCWr flag of REDUNDANCY(0x22) register writes received CRC value to FIFO buffer. When *CRCWr* is set to 1, microprocessor reads CRC value from FIFO and calculates CRC value in software level to confirm signal integrity.

RxCRCEn and *TxCRCEn* are flags to determine to use CRC during Transmit/Receive. When *TxCRCEn* is set to 1, CRC is sent with transmit data, and when *RxCRCEn* is set to 1 then data is received and calculates CRC for signal integrity.

According to command type, users should confirm CRC use through standard specification, and may need to set *RxCRCEn* and *TxCRCEn*.

Table 7-3 CRCPRESETLSB register

Name	Address	Reset	Value							
CRCPRESETLSB	0x23	0x63	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			CRCPresetLSB							

Number	Name	Description
7-0	CRCPresetLSB	Store CRC preset value LSB 8bit.

Table 7-4 CRCPRESETMSB register

Name	Address	Reset	Value							
CRCPRESETMSB	0x24	0x63	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			CRCPresetMSB							

Number	Name	Description
7-0	CRCPresetMSB	Store CRC preset value MSB 8bit.

CRCPRESETLSB(0x23) and CRCPRESETMSB(0x24) register are registers determining initial value of CRC calculation. CRC preset value are 8 bits each through 2 registers since 16-bit CRC is used. This register can change by microprocessor. Therefore, user can set CRC operation initial value.

Table 7-5 CRCRESULTLSB register

Name	Address	Reset	Value							
CRCRESULTLSB	0x0D	0xXX	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			CRCResultLSB							

Number	Name	Description
7-0	CRCResultLSB	Store CRC calculation result LSB 8bit.

X: don't care

Table 7-6 CRCRESULTMSB register

Name	Address	Reset	Value							
CRCRESULTMSB	0x0E	0xXX	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			CRCResultMSB							

Number	Name	Description
7-0	CRCResultMSB	Store CRC calculation result MSB 8bit.

X: don't care

CRCRESULTLSB(0x0D) and CRCRESULTMSB(0x0E) register are registers to store CRC calculation result. *CRCErr* flag of ERRFLAG(0x0A) register can be confirmed by microprocessor. Also microprocessor uses *CRCResultLSB* and *CRCResultMSB* to confirm CRC error occurrence.

Chapter8 Interrupt

8.1 Introduction

TRH033M-S supports various types of interrupt. Using interrupt benefits for microprocessor to control TRH033M. First, processing speed enhancement can be expected and second, efficiency in microprocessor calculation. If microprocessor controls more than 2 devices, benefits of interrupt enhance.

TRH033M-S supports total of 6 interrupts and user can select choose to use any interrupt.

8.2 Interrupt Use Method

TRH033M-S alerts microprocessor through IRQ pin when interrupt occurs in IEN(0x06) register setting. Therefore, user must select interrupts to be used set in IEN(0x06) register.

When microprocessor set the interrupt in IEN(0x06) and verify interrupt occurrence through IRQ pin, the microprocessor reads the IRQ(0x07) register to find out which interrupt has occurred. IRQ(0x07)register is automatically set to 1 when interrupt occurs but maintains the value until microprocessor change the value to 0. When multiple interrupt occur, if not microprocessor initialize interrupt to 0, despite additional interrupt occurrence IRQ pin has no impact thus microprocessor is not aware of interrupt occurrence.

Therefore, interrupt request is recommended to re-initialize after occurrence. IEN(0x06) and IRQ(0x07) registers are changeable by bit level. Basically user can change specific bit value and keep others as is. This function is useful when initializing single interrupt.

Table 8-1 IEN register

Name	Address	Reset	Value							
IEN	0x06	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			SetIEn	DtcIEn	TimerIEn	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn

Number	Name	Description
7	SetIEn	0: Clear Bit, From 0~6, set flag marked 1 as 0. 1: Set Bit. 0~6 set flag marked 1 as 1
6	DtcIEn	0: DtcIEn signal not sent to IRQ pin. 1: DtcIEn signal sent to IRQ pin.
5	TimerIEn	0: Not transfer TimerIRq signal to IRQ pin 1: Transfer TimerIRq signal to IRQ pin.
4	TxIEn	0: Not transfer TxIRq signal to IRQ pin. 1: Transfer TxIRq signal to IRQ pin.
3	RxIEn	0: Not transfer RxIRq signal to IRQ pin. 1: Transfer RxIRq signal to IRQ pin.
2	IdleIEn	0: Not transfer IdleIRq signal to IRQ pin. 1: Transfer IdleIRq signal to IRQ pin.
1	HiAlertIEn	0: Not transfer HiAlertIRq signal to IRQ pin. 1: Transfer HiAlertIRq signal to IRQ pin.
0	LoAlertIEn	0: Not transfer LoAlertIRq signal to IRQ pin. 1: Transfer LoAlertIRq signal to IRQ pin.

Table 8-2 IRQ register

Name	Address	Reset	Value							
IRQ	0x07	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			SetIRq	DtcIRq	TimerIRq	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq

Number	Name	Description
7	SetIRq	0: Clear Bit. From 0~6, set register marked 1 as 0. 1: Set Bit. 0~6 set register marked 1 as 1.
6	DtcIRq	0: Card detection result shows no card within RF field. 1: Card detection result shows card is detected within RF field.
5	TimerIRq	0: TimerValue register is not '0'. 1: TimerValueE register is '0'.
4	TxIRq	0: FIFO data not transmitted yet. 1: All FIFO data transmitted.
3	RxIRq	0: Receiving not complete yet. 1: Receiving complete.
2	IdleIRq	0: Not in Idle mode. 1: Command execution complete and remains in Idle mode.
1	HiAlertIRq	0: FIFO available space is more than WaterLevel. 1: FIFO available space is less than WaterLevel.
0	LoAlertIRq	0: FIFO data is more than WaterLevel. 1: FIFO data is less than WaterLevel.

(a) Bit Setting

	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
Register Value (before Write)	0	0	0	0	1	0	0	1
Write Data (0x9C)	1	0	0	1	1	1	0	0
Register Value (After Write)	0	0	0	1	1	1	0	1

(b) Bit Clear

	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
Register Value (before Write)	0	0	0	0	1	0	0	1
Write Data (0x1C)	0	0	0	1	1	1	0	0
Register Value (After Write)	0	0	0	0	0	0	0	1

Picture 8-1 IEN and IRQ register setting method

Above picture 8-1 displays IEN(0x06) register and IRQ(0x07) register setting method. Picture 8-1(a) displays register setting of bit value 1, and picture 8-1(b) displays register bit setting of 0.

From picture 8-1 (a) and (b), first byte data is previous data before written, 2nd byte is IEN(0x06) or IRQ(0x07) written data. Lastly 3rd byte changed value after it is written.

As seen on picture 8-1, when setting IEN(0x6) or IRQ(0x07)register as either 1 or 0 is determined by MSB then only bit 1 is changed and other bits maintains previous value.

IRQCONFIG(0x2D) register from TRH031M changed its location to CONTROL(0x09) Register Bit7. CONTROL[7] register is to set interrupt polarity. When *IrqPinInv* is set as 1, IRQ pin maintains value 1 during IDLE mode and when interrupt occur changes to 0. When *IrqPinInv* is set to 0, IRQ pin conversely maintains value 0 during IDLE mode and changes to value 1 when interrupt occurs.

Chapter9 Power Management

9.1 Introduction

TRH033M-S provide power down mode to minimize power consumption. User can minimize power consumption during reader chip idle mode using power down mode.

9.2 Power down Mode Effect

When power down mode is executed, TRH033M stops all devices consuming power and maintain idle until wake-up. Below table displays pin status during power down mode. For optimum performance of power down mode entry pin must assign different value other than high-Z.

Table 9-1 Pin assignment in power down mode

Symbol	I/O	Description
XIN	I	Oscillator disabled
IRQ	O	Output High
TX1	O	Output Low
TX2	O	Output Low
CSB, WRB, RDB	I	Input
DATA7 – DATA0	I	Input
PALE,TESTIN	I	Input
ADDR2, ADDR1, ADDR0	I	Input
TESTOUT, ATESTO	O	Output
RX	I	Input
VMID	I	Input
XOUT	O	Oscillator disabled
RST	I	Input (High)

9.3 Powerdown Mode Directions

9.3.1 Hardware PowerDown Mode

Hardware power down mode is a method to minimize power consumption using TRH033M-S RST pin. TRH033M-S activates power down mode when RST pin is 1. During power down mode, TRH033M-S internal main clock does not oscillate and needs some time to re-activate after RST is given low value. It's because stopped oscillation to resume clock and to stabilize requires a certain time. This required time is less than 1000us.

9.3.2 Software PowerDown Mode

Software power down mode activates when CONTROL(0x09) register sets as *PowerDown* flag to 1, and during software power down mode, all internal current consumption is minimized. This process is actually the same as hardware power down mode. In software power down mode, host interface remains in action mode to release from power down mode. Same as hardware power down mode, in software power down mode clock does not oscillate.

Also for RF/Analog Part power saving by each block, use TXCONTROL(0x11) *TxPwdn*, RXCONTROL1(0x19) *RxPwdn* and CARDDTCREG(0x33) *CdPwdn* to control receiving, transmitting and card detector.

CONTROL(0x09) Register *PowerDown* suspends power consumption in transmitting, receiving and card detector.

9.3.3 Card Detection Mode

Writing Detection command(0x5A : REQA command, 0x5C : REQA with Calibration, 0x57 : Detect command) to DETECTIR(0x35) register changes to card detection mode. Before writing Detection command to DETECTIR(0x35) register, setting CARDDTCREG(0x33) register Bit4, *IoscPwdn* flag value to 0 will initiate embedded internal oscillator.

Then, write command to DETECTIR(0x35) and through Internal Oscillator in TRH033M-S it wakes periodically to detect card and if card is not detected, it returns to sleep mode (All power Off except Internal Oscillator). While repeating this operation, if card is detected interrupt occurs, and alerts MCU through IRQ Pin. Then, Main Controller clears DETECTIR(0x35) and executes card reader function.

By reading card and if card is not registered then rewrite command to DETECTIR(0x35) for TRH033M-S to enter into Detect Mode and Main Controller enters to Standby mode for minimized power consumption.

By card detect interrupt, prior to MCU awake MCU can detect card automatically through TRH033M-S internal Oscillator by time count periodically even during the MCU standby mode.

At this time, after setting *IrqClrEn,* bit6 of DETECCTRL(0x2D), IRQ pin goes to low and returns to the detection mode. If this *IrqClrEn* value is 0, then IRQ Pin maintains Low value. Detailed technical information is available in Chapter 12.

Chapter10 Timer

10.1 Introduction

Microprocessor executes various timer operations. Using timer related registers, timer speed, timer control by event and timer interrupt occurrence are possible.

10.2 Timer Setting

Timer speed is determined by *TPreScaler* flag value of TIMERCLK(0x2A) register. Timer speed implies changes in speed of timer actual value. *TPreScaler* is divided into total of 5 bits. Timer speed is determined by 13.56MHz cycle. In below, $T_{TimerClock}$ implies timer speed.

$$T_{TimerClock} = 2^{T\,PreScaler} \times 73.7ns = \frac{2^{T\,PreScaler}}{13.56\text{MHz}}$$

TPreScaler value can be set from 0 to 21, therefore, possible $T_{Timerclock}$ value is from 74ns to 150ms.

Table 10-1 TIMERCLK register

Name	Address	Reset	Value							
TIMERCLK	0x2A	0x07	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	0	TRestart	TPreScaler				

Number	Name	Description
5	TRestart	If this value is 1, timer count is completed to 1 then reload TReloadValue to automatically restart timer.
4-0	TPreScalar	Set timer count speed.

From TIMERCLK(0x2A) register, *TRestart* is a register to re-start timer automatically. If *TRestart* is already set, do not reduce the timer value to 0, and when timer value is 1, *TimerReloadValue* value is reloaded and begins re-counting.

TRH033M-S timer begins counting from designated value. User can set timer start value using *TimerReloadValue* flag of TRELOADVALUE(0x2C) register.

Table 10-2 TRELOADVALUE register

Name	Address	Reset	Value							
TRELOADVALUE	0x2C	0x0A	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			TimerReloadValue							

Number	Name	Description
7-0	TimerReloadValue	The timer loads this value, when it works.

From timer start event to timer to have specific timer value, can be obtained using below. *TimerReloadValue* implies timer start value, and *TimerValue* is current timer value.

$$T_{Timer} = T_{TimerClock} \times (T\,\mathrm{Re}\,loadValue - TimerValue)$$

Subsequently, T_{Timer} value is estimated from 74ns to 40s.

Table 10-3 TIMERVALUE register

Name	Address	Reset	Value							
TIMERVALUE	0x0C	0xXX	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			TimerValue							

Number	Name	Description
7-0	TimerValue	Show the current value of the timer.

X: don't care

TimerValue flag of TIMERVALUE(0x0C) is a register to display current timer value. *TimerValue* flag comprises of 8 bits. *TimerValue* is made of total 8 bits thus timer can count from 0 to 2^{64}.

10.3 Timer Function

Basically timer can start or stop using *TStartNow* and *TStopNow* flag of CONTROL(0x09) register. Setting *TStartNow* to 1, timer load *TimerReloadValue* value to *TimerValue* flag and begin counting as reducing *TimerValue* value by 1. When timer is counting, user sets *TStartNow* to 1. Then, timer stops and displays consumed time through *TimerValue* value.

Other than timer function through CONTROL(0x09) register to utilize timer for transmit/receive select TCONTROL (0x2B) register. TCONTROL(0x2B) register controls timer count, and it is used when transmit/receive begin or end. For example, if user wants to know the amount of time after transmit complete, *TStartTxEnd of* TCONTROL(0x2B) register set to 1.

Table 10-4 TCONTROL register

Name	Address	Reset	Value							
TCONTROL	0x2B	0x06	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	0	0	0	TStopRxEnd	TStopRxBe	TStartTxEnd	TStartTxBe

Number	Name	Description
3	TStopRxEnd	When finished data receiving, timer end.
2	TStopRxBe	When starting data receiving, timer end.
1	TStartTxEnd	When finished data sending, timer start.
0	TStartTxBe	When starting data sending, timer start.

TStopRxEnd is a flag to stop timer after transmit completion, and *TStopRxBe* is a flag to stop timer when receiver begins. *TStartTxBe* is a flag to start timer when transmission begins.

TRunning flag of STATUS2(0x05) register displays current timer status. When start event begins, timer begins to count and *TRunning* flag becomes 1. Also when end event begins, timer stops counting and *TRunning* flag returns to 0.

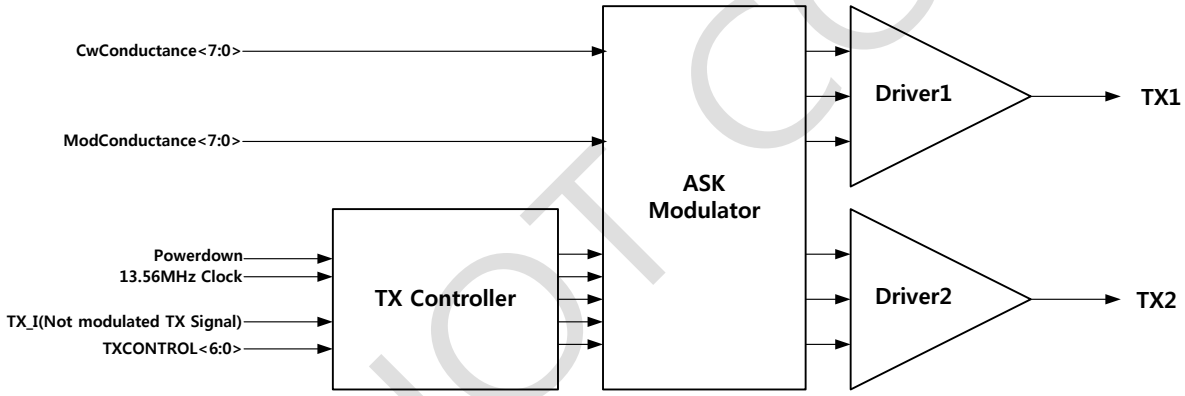
Timer is set to create interrupt. *TimerIRq* flag of IRQ(0x07) register is an interrupt request when timer value becomes 0.

Chapter11 Analog

11.1 Transmitter

Analog transmitter comprise of control block, ASK Modulator and driver. Transmitter transmits modulated 13.56MHz carrier frequency simultaneously controls TX1 and TX2 pin output signals.

11.2 Transmitter Structure



Picture 11-1 Transmitter Structure

Picture 11-1 displays transmitter configuration. TRH033M-S use two transmitter drivers for antenna signal efficiency.

11.3 Transmitter Function

Transmitter setting can be divided into signal type selection and output power. Next chapter explains transmitter setting method.

11.3.1 TX1 and TX2 Function Setting

Transmitter transmit TX_I (Transferred digital signal for modulation) modulated 13.56MHz carrier signal through TX1 and TX2. Also output signal from TX1 and TX2 for filtering and matching activate antenna through few external elements. TX1 and TX2 output signal can be set in various format through TXCONTROL(0x11) register.

Table 11-1 TXCONTROL register

Name	Address	Reset	Value							
TXCONTROL	0x11	0x58	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			TxPwdn	ModulatorSource		F100ASK	TX2Inv	TX2Cw	TX2RFEn	TX1RFEn

Number	Name	Description
7	TxPwdn	Tx Power down signal
6-5	ModulatorSource	Select the modulator source 00: Constant Low (continuously 0 signal) 01: Constant High (continuously 1 signal) 10: Internal coder source 11: TESTIN pin source
4	F100ASK	0: ASK modulation depth is determined by ModConductance value. 1: Fix ASK modulation depth to 100%.
3	TX2Inv	0: TX2 pin and TX1 pin output carrier signals are in-phase. 1: TX2 pin output carrier signal is 180˚ phase to TX1.
2	TX2Cw	0: TX2 pin and TX1 pin output signals are modulated. 1: TX2 pin output signal is not modulated.
1	TX2RFEn	0: TX2 pin not used. (Output Constant Low value) 1: TX2 pin used. (Output RF signal)
0	TX1RFEn	0: TX1 pin not used. (Output Constant Low value) 1: TX1 pin used. (Output RF signal)

Table 11-2 TX1 related settings

TX1RFEn	F100ASK	TX_I	Signal on TX1
0	**X**	**X**	LOW
1	**0**	**0**	13.56MHz carrier frequency modulated
		1	13.56MHz carrier frequency
1	**1**	**0**	LOW
		1	13.56MHz energy carrier

Table 11-2 displays *TX1RFEn* and *F100ASK* flag of TXCONTROL(0x11) register and TX1 output signal by TX_I (Transferred digital signal for modulation). *TX1RFEn* flag of TXCONTROL(0x11) register is a flag for TX1 operation. Until *TX1RFEn* is set to 1, there is no output signal from TX1. When *TX1RFEn* set to 1, transmitter modulates TX_I (Transferred digital signal for modulation) based on *F100ASK* value. When *F100ASK* is set to 1, 100% ASK modulation occurs and when *F100ASK* is set to 0, user can modify modulation index based on *ModConductance* value.

Table 11-3 TX2 related settings

TX2RFEn	F100ASK	TX2Cw	TX2Inv	TX_I	Signal on TX2
0	**X**	**X**	**X**	**X**	LOW
1	**0**	**0**	**0**	**0**	13.56MHz carrier frequency modulated
				1	13.56MHz carrier frequency
			1	**0**	13.56MHz carrier frequency modulated, 180˚phase shift relative to TX1
				1	13.56MHz carrier frequency, 180˚phase shift relative to TX1
		1	**0**	**X**	13.56MHz carrier frequency
			1	**X**	13.56MHz carrier frequency, 180˚phase shift relative to TX1
	1	**0**	**0**	**0**	LOW
				1	13.56MHz carrier frequency
			1	**0**	HIGH
				1	13.56MHz carrier frequency, 180˚phase shift relative to TX1
		1	**0**	**X**	13.56MHz carrier frequency
			1	**X**	13.56MHz carrier frequency, 180˚phase shift relative to TX1

Table 11-3 displays flag value of TXCONTROL(0x11) register and TX2 output signal by TX_I (Transferred digital signal for modulation). TX2 as well as TX1 output signal only when *TX2RFEn* is set to 1 and select modulation method by *F100ASK* value.

TX2Cw regardless of TX_I (Transferred digital signal for modulation) signal to TX2 is a flag to output as same as when TX_I value is 1. Lastly, *TX2Inv* is a flag to output TX1 and TX2 phase in 180° reverse.

11.3.2 TX1 and TX2 Output Power Setting

TX1 and TX2 output drivability change by conductance value. As conductance value rise, TX1 and TX2 output rise as well. TX1 and TX2 driver conductance use *CwConductance* of CWCONDUCTANCE(0x12) register and can be adjusted. (R_p : p-channel resistance)

Table 11-4 CWCONDUCTANCE register

Name	Address	Reset	Value							
CWCONDUCTANCE	0x12	0xFF	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	0	ExtraD	CwConductance				

Number	Name	Description
5	ExtraD	Extra Driver
4-0	CwConductance	Set Conductance value of TX1 and TX2.

Table 11-5 TX1 and TX2 P-channel resistance

CwConductance	R_p [Ohm]
0	∞
1	17
2	8.5
4	4.25
8	2.12
16	1.06
32	3.19

Table 11-5 is a table to display TX1 and TX2 P-channel resistance. P-channel resistance is inverse to driver conductance. If *CwConductance* value is set to 3, P-channel resistance value becomes 5.7 with parallel calculated considering when *CwConductance* 1 value is 17 and when *CwConductance* 2 value is 8.5.

11.3.3 TX1 and TX2 Modulation Index Adjustment

If *F100ASK* is not set to 1, TX1 and TX2 modulation index is impacted by *ModConductance* of MODCONDUCTANCE(0x13) register value. The role of *ModConductance* is to adjust driver conductance when TX1 and TX2 process modulation and impacts ASK modulation index changes. (R_p : p-channel resistance)

Table 11-6 MODCONDUCTANCE register

Name	Address	Reset	Value							
			7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
MODCONDUCTANCE	0x13	0x00	0	0	ModConductance					

Number	Name	Description
5-0	ModConductance	Set modulation conductance value of TX1 and TX2.

Table 11-7 TX1 and TX2 modulation P-channel resistance

ModConductance	R_p [Ohm]
0	∞
1	102
2	51
4	25.5
8	12.75
16	6.37
32	3.19

Table 11-7 is a table displaying TX1 and TX2 modulation P-channel resistance. Same as *CwConductance*, when two or more bits are set *ModConducatance* also result in adding each Rp value in parallel. Changes in Rp change modulation index but it is impacted by Rp value and matching circuit simultaneously. Changes in modulation index due to *ModConducatance* value change, please refer to "TRH03XM CookBook"

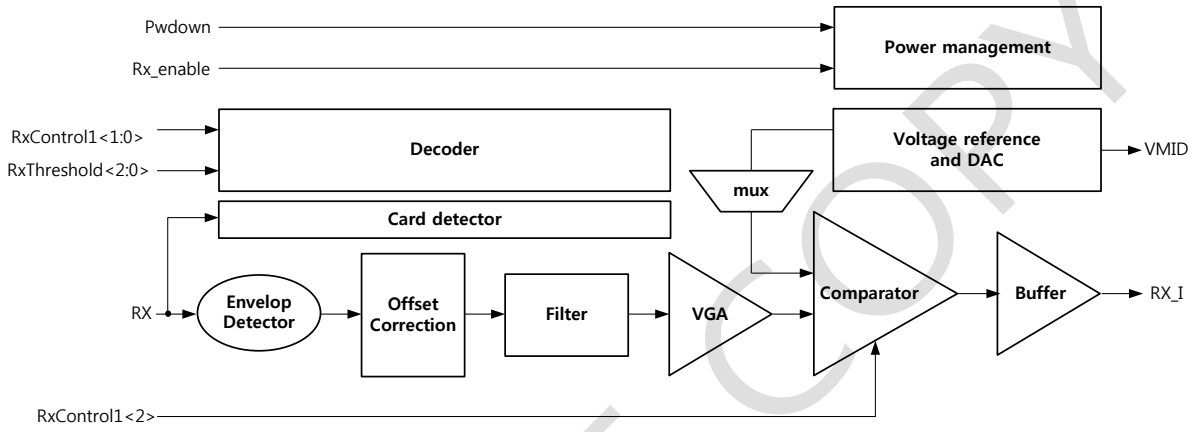
11.3.4 Recognition Distance and Power Consumption

Recognition distance and power consumption have proportional relationship. As transmitter power consumption increase recognition distance also increases. Therefore, there is a trade-off between Recognition distance and power consumption. User should consider this fact when designing.

11.4 Receiver

Receiver execute converting 13.56MHz tag signal through RX pin and sensing envelop to convert to digital signal. This process is called demodulation.

11.5 Receiver Structure



Picture 11-2 Receiver Structure

Receiver configuration is displayed in Picture 11-2. Receiver performs demodulation process through Envelop detector, VGA and Comparator. VMID informs to comparator signal distinction standard level.

11.6 Receiver Function

Receiving process can be divided into various levels. Next sections will describe each role and possible settings.

11.6.1 Envelope Detector

Envelop detection is a level to delete carrier from received signal and output envelop changes. TRH033M-S suggest PMOS diode structure for more stable data receiving.

11.6.2 Offset Collection

In this level, Offset collection for more clear and ideal DC biasing. To find this DC bias point, standard methods such as Pass Filtering and AC coupling were used.

11.6.3 Variable Gain Amplifier: VGA

Demodulated signals are amplified for improved performance. VGA Gain can be controlled using *VGAGain* flag of RXCONTROL1(0x19) register. Table 11-9 displays VGA Gain based on *VGAGain* flag value. (Filter default Gain : 27.6dB)

Table 11-8 RXCONTROL1 register

Name	Address	Reset	Value							
RXCONTROL1	0x19	0x03	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			RxPwdn	VmidPwdn	RxForce	ComRefOff	0	VGAGain		

Number	Name	Description
7	RxPwdn	Receiver Power down
6	VmidPwdn	Vmid Power down, Connects Vmid to AVDD
5	RxForce	Receiver data Enable signal
4	ComRefOff	Comparator reference voltage Off Receiver Calibration Off
2-0	VGAGain	Adjust RX amplifier gain. This value can be changed by protocol type and working environment.

Table 11-9 Gain value by VGA Gain setting

VGAGain	Gain [dB] (Simulation Results)
0	27.6
1	33.62
2	37.14
3	39.64
MSB: high → +6dB EX) VGAGain[2:0] : 111 → 39.64 + 6 = 45.64dB	

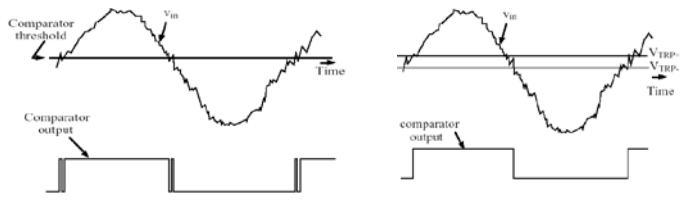
11.6.4 Comparator

Comparator is a last step to convert output signal through envelop detector and VGA to digital signal. If comparator (As seen on picture 11-3 (a)) transforms very fast at certain threshold point, inaccurate signals will output in noise environment. In this type of situation, comparator transformation characteristics should be modified. Thus, TRH033M-S allows hysteresis range (Picture 11-3(b)) in comparator. Hysteresis range can be modified by *HysRangeCon* of RXTHRESHOLD(0x1C) register.

Table 11-10 RXTHRESHOLD register

Name	Address	Reset	Value							
			7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
RXTHRESHOLD	0x1C	0x65	HysRangeCon		ComRefVolCon					

Number	Name	Description
7-6	HysRangeCon	Control comparator Hysteresis Range.
5-0	ComRefVolCon	Control comparator reference voltage.



Picture 11-3 (a) Ordinary comparator noise impact (b) Hysteresis added comparator noise impact

Table 11-11 Hysteresis range of comparator based on HysRangeCon value

Hysteresis Range Control	Hysteresis ranges/$V_{TRP\pm}$ [mV] (Simulation Results)
0	**53**
1	**72**
2	**90**
3	**108**

Table 11-11 displays hysteresis range based on *HysRangeCon* flag value. As seen on above table, hysteresis range of comparator can be modified from 53mV to 108mV. Also comparator can set Input Reference Voltage. Input Reference Voltage is standard voltage that comparator can determine whether 0 or 1. To adjust comparator Input Reference Voltage value, *ComRefOff* flag should be set as 0. Then input Reference Voltage value changes by *ComRefVolCon value of* RXTHRESHOLD(0x1C) register. If *ComRefOff* value is set to 1, Input Reference Voltage is 1.65V irrelevant of *ComRefVolCon* value. Table 11-12 displays Input Reference Voltage value by *ComRefVolCon* value.

Table 11-12 Comparator Input reference voltage by *ComRefVolCon* value

Comparator Reference Voltage Control	Reference voltage [V] (Simulation Results)
0	**1.37+1LSB**
39	**1.65**
63	**1.85**
* 1LSB = 7.5mV, 1bit increase then 7.5mV Adjustable from 1.3775V~1.85V	

11.7 Card Detector

Transmitter sends 13.56MHz signal to antenna for a set period of time for card detection. At this time signal attenuation occurs when card is detected. Card detector rectifies 13.56MHz signal so it detects cards by comparing attenuated and rectified signals. By using card detector, user can reduce unnecessary power consumption when card is not being used.

11.7.1 Card Detector Standard Voltage

Card Detector standard voltage is a voltage to compare rectified signal that is a value of TRH033M-S internal 6bit-DAC block output. Based on board and external environment, standard voltage can be adjusted as below Table 11-14.

Table 11-13 DETECTLEVEL Register

Name	Address	Reset	Value							
DETECTLEVEL	0x32	0x3F	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			AtestOutSel		CdRefVolCon					

Number	Name	Description
7-6	AtestOutSel	ATESTO Output signal control.
5-0	CdRefVolCon	Set voltage for Card Detection. (Detail information refer to "TRH03XM CookBook" and "Card detector guide")

Table 11-14 ATESTO output signal by *AtestoCon* value

AtestOutSel	Output signal
0	Ground
1	Comparator reference voltage output (ComRefVolCon controlled output)
2	Card detector rectifier output
3	Card detector reference voltage output (CdRefVolCon controlled output)

Table 11-15 Detector reference voltage by CdRefVolCon value

CdRefVolCon	Reference voltage [V] (Simulation Results)
0	1.02V + 1LSB
63	1.7V
*1LSB = 10.625mV, 1bit increase then 10.625mV Adjustable from 1.03V~1.7V	

11.7.2 Card Detector Control

For Card Detector control, setting ideal *CdRefVolCon* flag value setting to meet system requirement is most important. Before finding this ideal value, setting transmitter output for card detection is necessary. In Card detection mode, it doesn't need to operate the entire system. Thus, internal oscillator is used for low power consumption in TRH033M-S.

Table 11-16 explains about CARDDTCREG(0x33) register. CARDDTCREG(0x33) register is card detector control register.

Table 11-16 DETECTREG Register

Name	Address	Reset	Value							
CARDDTCREG	0x33	0x1C	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			BgrR	RcvInv	CdInv	CdPwdn	IoscPwdn	1	0	CdoutR

Number	Name	Description
7	BgrR	Bgr Reset, Connects Bgr to AVDD
6	RcvInv	Receiver data inverting signal. Default 0 (Calibration function only)
5	CdInv	Card detector output inverting signal. Default 0
4	CdPwdn	Card detector Power down 1 – Card detector Power Down 0 – Card detector Enable
2	IoscPwdn	Internal Oscillator Power down (Oscillation frequency : 50kHz) 1 – Internal Oscillator Power Down 0 – Internal Oscillator On
0	CdoutR	Card detector output value Register When card detected value is set as 0. (For detailed information refer to "TRH03XM CookBook" and "Card detector guide")

Detector power output can be confirmed from hardware using TESTOUT pin. TESTOUTSEL(0X26) Setting TESTOUTSEL(0X26) register to 05h, detector power output can be confirmed. Set detector power output to High *CdRefVolCon* value of DETECTLEVEL(0x32), and power output becomes low when card is detected. In order to prevent the malfunction in detector environment, an offset Calibration is done. (Refer to "12.1 Offset Calibration")

If offset Calibration is carried out (writing 27h value to CALIR(0x2E)), card detector analog value is written to CARDDTCREG2(0x3E). At the same time, CALOFFSET(0x25) value is calculated and writed to *CdRefVolCon* of DETECTLEVEL(0x32). When CALOFFSET(0x25) 00h is set, it often malfunctions in card detection. Thus, setting minus margin enable removes the malfunction which looks like there is a card.

Table 11-17 DETECTREG2 register

Name	Address	Reset	Value							
CARDDTECREG2	0x3E	0x3F	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	0	CdScanR					

Number	Name	Description
5-0	CdScanR	Card detector Rectifier Scan result Register

Chapter12 Calibration and Card Detection function

Two key characteristics of TRH033M-S are internal calibration for maximum optimized operation and card detection function independently without MCU control.

12.1 Offset Calibration - Receiving and Card Detector

TRH033M-S offers calibration function for optimized performance by reader configuration and environment, card type and location.

Calibration is useful since various antenna size, type and reader system environment impact card reading and detection performance negatively. It is mainly due to TRH033M-S internal RF/Analog circuit reference point is impacted by this environment, and calibration allows optimized performance despite changes in reader system environment. Thus calibration allows TRH033M-S to perform at its maximum wherever possible.

Calibration is divided into card reader receiving calibration and card detector calibration. Calibration is accomplished by entering command to CALIR(0x2E), and for receiving calibration, set to execute automatically prior to reading functions.

Table 12-1 CALOFFSET register

Name	Address	Reset	Value							
CALOFFSET	0x25	0x10	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			CardOffset				ReceiverOffset			

Number	Name	Description
7-4	CardOffset	Card Detector Offset margin setting 7: Offset Sign / 0 – Plus, 1 - Minus 6-5: Margin Value / 0 ~ 7value
3-0	ReceiverOffset	Receiver Calibration Offset margin setting 3: Offset Sign / 0 – Plus, 1 - Minus 2-0: Margin Value / 0 ~ 7value

As seen on Table 12-1, offset as plus/minus value can be manually set after calibration. After calibration of receiving layer, default value is usually set without regulating offset margin. Card detector offset margin needs to be set.

12.1.1 Receiving Calibration

Writing value 36h to CALIR(0x2E), TRH033M-S receiving executes calibration. After calibration, CALIR(0x2E) value is automatically This receiving calibration process should be used by using card Read command as *CALTRANSCEIVE*(14h) of COMMAND(0x01) command to automatically optimize its performance.

Table 12-2 CALIR register

Name	Address	Reset	Value							
CALIR	0x2E	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			CalibrationInstruction							

Number	Name	Description
7-0	CalibrationInstruction	It is used in calibration command and executes automatically card reading command. It sets optimal reading range, manually Calibration is executed by commanding manually this Register. 0x00 : Idle 0x37: Receiving Calibration operation 0x27: Detection Calibration operation

12.1.2 Card Detector Calibration

Writing value 27h to CALIR(0x2E), TRH033M-S card detector calibration is executed. After calibration, CALIR(0x2E) value is automatically cleared.

Table 12-3 DETECTCTRL register

Name	Address	Reset	Value							
DETECTCTRL	0x2D	0x03	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			0	IrqClrEn	0	0	SelCalClk		DTCTX2En	DTCTX1En

Number	Name	Description
6	IrqClrEn	As a result of detection, executing, Interrupt through IRQ Pin occurs. If Detection Mode is not terminated within certain time, then Interrupt is generated periodically through IRQ Pin. Setting this function is helpful to prevent malfunction of set.
3-2	SelCalClk	Set Calibration function time and use 0 value.
1	DTCTX2En	1: At the time of Calibration execution TX2, RF Carrier is On 0: At the time of Calibration execution TX2, RF Carrier is Off In case TX2 is used in antenna output, then set as 1
0	DTCTX1En	1: At the time of Calibration execution, TX1, RF Carrier is On 0: At the time of Calibration execution, TX1, RF Carrier is Off In case X1 is used in antenna output,, set as 1

12.2 Executing Card Detection Function

Card Detection function suspends electricity flow in all blocks in TRH033M-S including main oscillator. Without MCU control, card detection is automatically executed by time calculation of approximately 50KHz interval internal oscillator. For card detection execution, 50KHz Internal Oscillator is not used but turning on Main Oscillator of 13.56MHz. Main oscillator after executing card detection function returns to off mode when card is not detected.

Only internal Oscillator activation makes it power saving mode. Since card detection function executes itself automatically without MCU control, As MCU is in Power Down mode, it enables to save the power consumption. When card is detected, MCU is awaken by interrupt.

Like above card detection function executes itself periodically without MCU control and informs MCU through IRQ pin when card is detected, MCU is not required to execute separate functions.

Using card detection function power saving is maximized, and card reader without power-on button becomes possible. Basically MCU remains in Power-down status, and TRH033M executes card detection functions. When card is detected MCU is awaken by interrupt then MCU executes card reading capability thus establishing convenient very low power consuming system. Applications using batteries including door lock, locker lock, toys, etc are ideal for using card detection functions.

There are two types of card detection functions; REQA Detection for ISO 14443A card only and Auto Detection to use all RF cards. REQA Detection function executes 14443A standard REQA command by set time to confirm card response. Since 14443A standard REQA execution time is reasonably short thus card detection is accomplished without much power consumption. However, this method uses REQA command thus only can be used with 14443A card. Other ISO standard cards (14443B or 15693) command operating time takes much longer than REQA thus power consumption is high thus this is more applicable for 14443A only. Other detection method is to auto detect by receiving RX current from reader antenna and using its value to detect card. This method can be used regardless of card type. This method also maintains TRH033M-S main oscillator (13.56MHz) in off status and internal oscillator (50KHz) process time counting then periodically turns on main oscillator to send non-modulated RF wave to antenna at the same time receiving response signal from antenna through RX pin to detect card. Compared to REQA method RF on time is short thus more ideal for minimized power consumption. However, in case of this method may reduce a little bit detecting distance. User can select either method for card detection functions.

12.2.1 REQA Detection

To enable REAQ detection command user must set 14443A Type REQA command registers, and set TX1 and TX2 RF drivers in off status. Also clear *IoscPwdn* of CARDDTCREG(0x33) register to 0. Then internal oscillator will be on to calculate REQA Detection command executing time.

From REQA Detection mode setting REQA detect command executing time are determined setting and executes command by DTRELOADH(0x36) and DTRELOADL(0x37).

Table 12-4 CALIR register

Name	Address	Reset	Value							
			7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
CARDDTCREG	0x33	0x1C	BgrR	RcvInv	CdInv	CdPwdn	IoscPwdn	1	0	CdOut_R

Number	Name	Description
7	BgrR	BGR Reference voltage Reset (TEST Register)
6	RcvInv	Receiver inverting signal
5	CdInv	Card detector output signal inverting
4	CdPwdn	Card detector Power down
3	IoscPwdn	Internal Oscillator Power down (50kHz Oscillator)
0	CdOut_R	Card detector output value Register

Table 12-5 DTRELOADH register

Name	Address	Reset	Value							
DTRELOADH	0x36	0x7A	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			DetectionTimerReloadHigh							

Number	Name	Description
7-0	DetectionTimerReloadHigh	For auto-Polling function, internal Oscillator of 50KHz operates Polling function periodically. The period decreased 16 bits Register value set as DTRELOADH and DTRELOADL by internal Oscillator of 50KHz. Until it decreases to 0 value, it operates polling function once. Thus, Auto-Polling period is determined by this Register value like internal Oscillator of 50KHz.

Table 12-6 DTRELOADL register

Name	Address	Reset	Value							
			7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
DTRELOADL	0x37	0x12	DetectionTimerReloadLow							

Number	Name	Description
7-0	DetectionTimerReloadLow	For auto-Polling function, internal Oscillator of 50KHz operates Polling function periodically. The period decreased 16 bits Register value set as DTRELOADH and DTRELOADL by internal Oscillator of 50KHz. Until it decreases to 0 value, it operates polling function once. Thus, Auto-Polling period is determined by this Register value like internal Oscillator of 50KHz.

Detection period is the value 16bit multiplied by 20us. Maximum Detection period is 65536 x 20us = 1.32sec.

표 12-7 MCLKONCNT 레지스터

Name	Address	Reset	Value							
			7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
MCLKONCNT	0x39	0x70	MainOscOnTimeCount							

Number	Name	Description
7-0	MainOscOnTimeCount	Main Oscillator on duration can be calculated by MCLKONCNT value multiplied by 80us.

Table 12-8 RFONCNT register

Name	Address	Reset	Value							
RFONCNT	0x3C	0x30	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			DetectorRFOnTimer							

Number	Name	Description
7-0	DetectorRFOnTimer	For auto-Polling function, Auto-Polling period is set by DTRELOADH, DTRELOADL value and one RF Card exists from one period. RF On duration can be calculated by RFONCNT value multiplied by 80us.

MCLKONCNT(0x39), RFONCNT(0x3C) value determines 'on' duration of Main Oscillator of 13.56MHz and RF.This value makes Main Oscillator 'on' state for MCLKONCNT(0x39) multiplied by 80us. RF On duration is recommended to be set for RF to become On, 800us after Oscillator becomes On.

By setting detection timer clock as above, DTRELOADH(0x36) and DTRELOADL(0x37) 16bit value initiates detection and simultaneously reload to internal 16bit detection timer. Consequently, this detection timer value is reduced by 1. By this 16bit detection timer value, detection activation time is set.

When MCLKONCNT(0x39) x Detection Timer Clock value is determined and MCLKONCNT(0x39) is 30h, then, 30h(hexadecimal number) x 80us = 3840us = 3.84ms, basically main Oscillator is On in 3.84ms. RFONCNT(0x3C) is the Register that determines RF-On time. RF On value setting can be calculated by same method like MCLKONCNT(0x39). It has to be used less value than MCLKONCNT(0x39). If RFONCNT(0x3C) value is 20h, RF is On for 20h x 80us = 2560us = 2.56ms.
As above determine card detection cycle and writing to 5Ch value in DETECTIR(0x35) Register TRH033M-S reader chip enters card REQA Detection Mode.

Afterward MCU control is not necessary, and TRH033M performs card detection independently. If REQA is detected, through IRQ Pin alerts MCU that a card is detected. Therefore, MCU can maintain standby mode to conserve power during TRH033M-S card detection operation thus maximizing power saving very conveniently.

Table 12-9 DETECTIR register

Name	Address	Reset	Value							
DETECTIR	0x35	0x00	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			DetectInstruction							

Number	Name	Description
7-0	DetectInstruction	Command Register executing Auto-Polling function. There are two type of commands The one is command executing Auto-Polling 5Ah of 14443 A Type The other type is applying all of cards 57h. When 5Ah or 57h commands execute, main Oscillator of 13.56MHz becomes Off state It is awaken by internal Oscillator with periodic and polling function is executed. To finish this command, this Register is cleared as 00h.

Table 12-10 DTCTIMERV register

Name	Address	Reset	Value							
DTCTIMERV	0x3B	0xXX	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			DetectorTimerValue							

Number	Name	Description
7-0	DetectorTimerValue	Read Only. In Auto-Polling, becomes Count Down 16-bit Counter upper 8-bit for period calculation. Not necessary to use.

X: don't care

Table 12-11 DTCASTATR register

Name	Address	Reset	Value							
DTCASTATR	0x2F	0x35	7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
			DetectorStartTimerReload							

Number	Name	Description
7-0	DetectorStartTimerReload	It used in Auto Polling mode. When TIMERV Register value is as same as DTCASTARTR Register value, then REQA Detection command is executed. In Auto Polling mode, TIMERV Register value decreases from setting value of TRELOAD Register, if this value is as same as DTCASTARTR, REQA command executes.

12.2.2 Auto Detection

Auto Detection is a method that receives reader antenna RX current and using that value to detect card. This method can detect any type of card regardless of ISO protocols. This method also keeps TRH033M Main Oscillator (13.56MHz) in Off status, and Internal Oscillator(50KHz) performs Time Counting then turn on Main Oscillator at set period of time to send non-modulated 13.56MHz RF wave to Antenna simultaneously receiving RX Pin antenna response signal to detect card. Compared to REQA method RF On time is short thus more beneficial for saving power. However, in case of ISO 14443A Type card, card detection distance and reading distance are about equal but this method may decrease detection distance.

After setting DTRELOADH(0x36), DTRELOADL(0x37), MCLKONCNT(0x39) and RFONCNT(0x3C) value, write 57h value to DETECTIR(0x35) for Auto Detection operation. Detection cycle, alerting MCU through Interrupt after detection and Main Oscillator remains Off except during detection operation are same as REQA detection. However, detecting time is shorter than REQA Detection thus MCLKONCNT(0x39) value can be set less than REQA Detection.

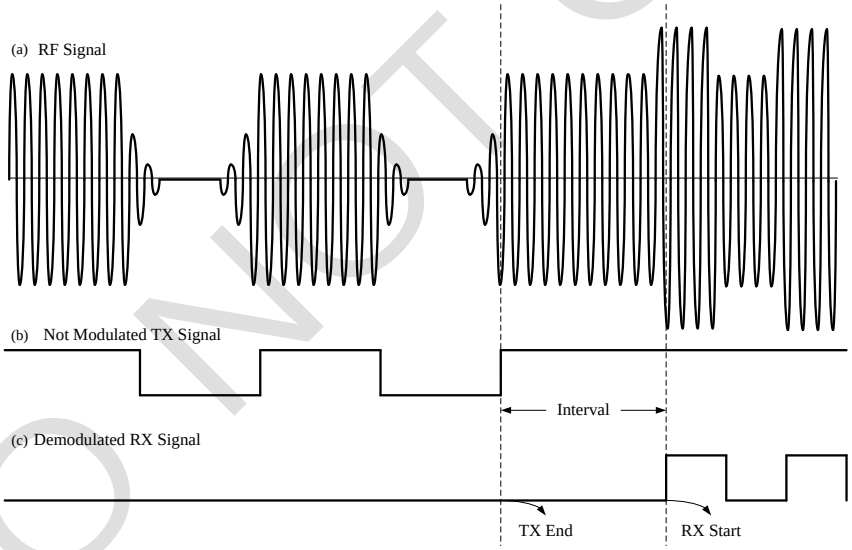
Chapter13 Test

13.1 Introduction

TRH033M-S supports debugging process after design completion using various test features. Using TESTOUT pin for signal output from TRH033M-S, user can test functionality.

13.2 How to use test pin

Picture 13-1 is transmit and receiving process



Picture 13-1 Observable signals by using test pin

Table 13-1 TESTOUTSEL register

Name	Address	Reset	Value							
			7-bit	6-bit	5-bit	4-bit	3-bit	2-bit	1-bit	0-bit
TESTOUTSEL	0x26	0x00	0	0	0	0	TestSel			

Number	Name	Description
3-0	TestSel	Select send out signal to TESTOUT pin. 0000: Constant low 0001: Constant high 0010: Demodulated RX Signal 0100: Not modulated TX Signal 0101: Card detector output Signal 1000: Internal Oscillator output Signal

Picture 13-1(a) is signal on antenna and picture 13-1(b) is transmitted digital signal from digital block to analog block for modulation. Picture 13-1(c) is digital signal originally received from tag and demodulated from analog block and sent to digital block. User can confirm activation using TESTOUT pin to observe picture 13-1(b) and picture 13-1(c) signal. TESTOUT pin output can be set using *TestSel* flag of TESTOUTSEL(0x26) and if the value is 04h, then picture 13-1(b) and value is 02h then picture 13-1(c) signal output occurs.

Chapter14 Electrical Characteristics

14.1 Operating condition range

Symbol	Parameter	MIN	TYP	MAX	UNIT
T_{op}	Operating temperature range	-25	+25	+85	℃
DVDD	Digital power supply	2.9	3.3	3.6	V
AVDD	Analog power supply	2.9	3.3	3.6	V
TVDD	Transmitter power supply	2.9	3.3	3.6	V

14.2 Current consumption

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
I_{DVDD}	Digital Supply current	Idle Command	5.0	7.5	9.5	mA
		Power Down mode	0.1	0.2	0.4	uA
I_{AVDD}	Analog Supply current	Receiver On	2.5	3.15	4.5	mA
		Power Down mode	0.01	0.05	0.5	uA
I_{TVDD}	Transmitter Supply current	Continuous Wave Antenna unconnected (TX1 and TX2 On, CwConductance = 3F)	110	130	150	mA
		Continuous Wave Antenna unconnected (TX1 On and TX2 Off, CwConductance = 01)	24	28	33	mA
		TX1 and TX2 unconnected, TX1,2 disable / clock on	7.0	9	11.0	uA
		TX1 and TX2 unconnected, TX1,2 disable / clock off	0.05	0.1	0.3	uA
I_{ek}	Total Leakage current	Power Down mode	0.1	0.35	1.0	uA
I_{op}	Total Operating current	Operating mode (* Minimum powerTX1 On TX2 Off, CwConductance = 01)	130 (34)	140 (38)	150 (44)	mA

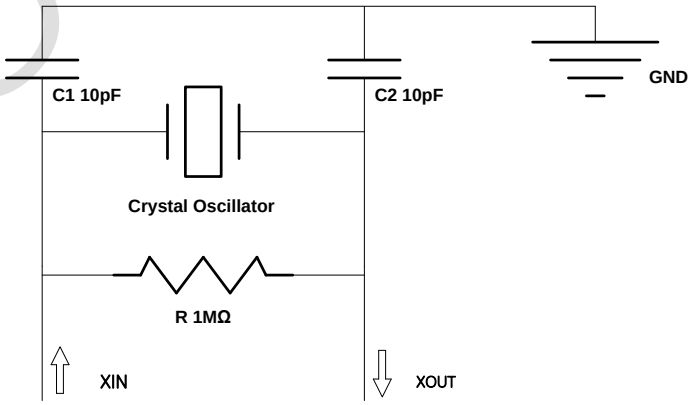
14.3 Internal Oscillator characteristics

SYMBOL	PARAMETER	Power / Temp.	2.7V	3.0V	3.3V	3.6V
F_{Iosc}	Iosc Frequency	-40°C	34 kHz	37 kHz	40 kHz	42 kHz
		-25°C	36 kHz	40 kHz	42 kHz	45 kHz
		25°C	43 kHz	47 kHz	50 kHz	52 kHz
		85°C	51 kHz	55 kHz	58 kHz	61 kHz
		125°C	55 kHz	59 kHz	62 kHz	65 kHz

SYMBOL	PARAMETER	Power / Temp.	2.7V	3.0V	3.3V	3.6V
I_{Iosc}	Iosc Current	25°C	1uA	1.33uA	1.7uA	2uA

14.4 External Oscillator characteristics

Symbol	Parameter	MIN	TYP	MAX	UNIT
F_{xtal}	Frequency range	-	13.56	-	MHz
R_{xtal}	Crystal Oscillator Resistor value	-	1M	-	Ohm
C_{xtal}	Crystal Oscillator Capacitor value	-	10p	-	F
S_{xtal}	Crystal Oscillator settling(start-up) time : XOUT Pin, *see note1	-	-	0.5	ms



Picture 14-1 External Crystal Oscillator circuit

14.5 Receiver characteristics

Symbol	Parameter		MIN	TYP	MAX	UNIT
RX_{in}	Receiver input dynamic range		-	-	3.3	V_{pk-pk}
RX_{sen}	Receiver Demodulation sensitivity		3	-	-	mV
RX_{cf}	Receiver IF filter cut-off frequency		100k	-	1M	Hz
VMID	Vmid output voltage		-	1.65	-	V
VM_{st}	Vmid settling(start-up) Time *see note1	No load	-	-	0.2u	sec
		Output load 47nF	-	-	0.4m	
		Output load 100nF	-	-	1.0m	

Notes

1. Settling time depends on the surround environments.
   (PCB board capacitance, Capacitor device variation, Soldering, ETC)

14.6 Auto-Calibration characteristics

Symbol	Parameter	MIN	TYP	MAX	UNIT
T_{rxcal}	Receiver Calibration time DTCCTRL(0x2D) *SelCalClk=00,*	-	-	100u	sec

14.7 Standard I/O Pin DC characteristics

SYMBOL	PARAMETER	MIN	MAX	Conditions	
				VDD	비고
VIL	Low level input voltage	-0.5V	0.3 X VDD	2.7V to 3.6V	Guaranteed Input Low Voltage
VIH	High level input voltage	0.7 X VDD	VDD + 0.5V	2.7V to 3.6V	Guaranteed Input High Voltage
VOL	Low level output voltage		VSS + 0.1V	2.7V	
VOH	High level output voltage	VDD – 0.1V		2.7V	

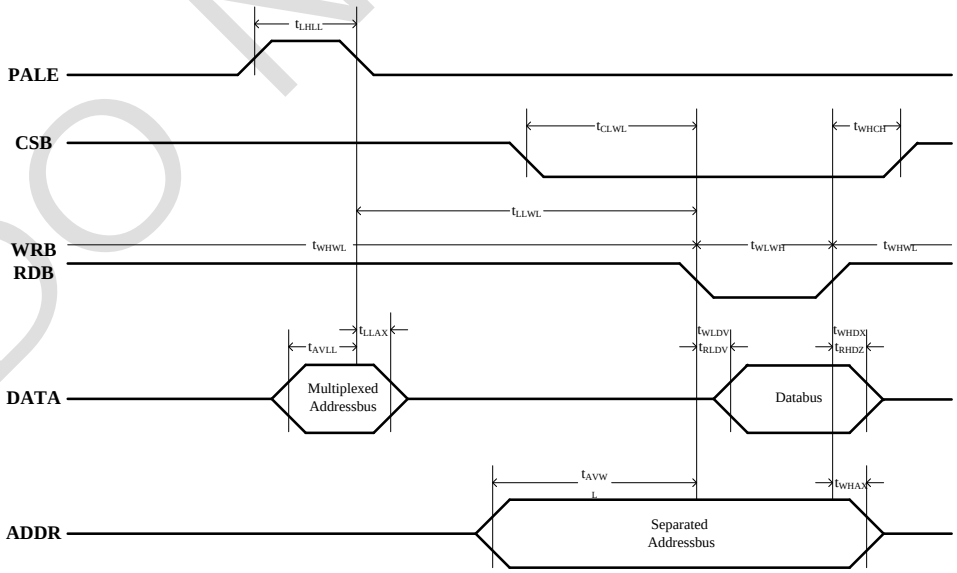
14.8 Schmitt Trigger Input Threshold

VT+			VT-			Hysteresis			Unit
MIN	MAX	TYP	MIN	MAX	TYP	MIN	MAX	TYP	
1.39	2.06	1.82	0.9	1.46	1.24	0.49	0.6	0.58	V

14.9 Timing specification

14.9.1 Timing for Read/Write Strobe

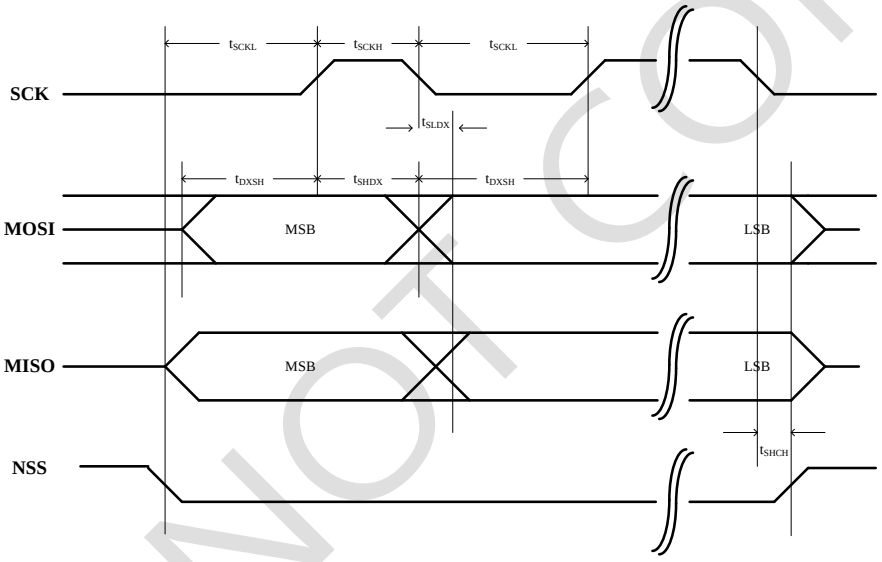
SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{LHLL}	PALE pulse width	10		ns
t_{AVLL}	Multiplexed Address Bus Setup Time	4		ns
t_{LLAX}	Multiplexed Address Bus Hold Time	6		ns
t_{LLWL}	PALE low to WRB, RDB low	5		ns
t_{CLWL}	CSB low to WRB, RDB low	0		ns
t_{WHCH}	WRB, NWR high to CSB high	0		ns
t_{RLDZ}	RDB low to DATA valid		35	ns
t_{RHDZ}	RDB high to DATA high impedance		20	ns
t_{WLDV}	WRB low to DATA valid		35	ns
t_{WHDX}	DATA Bus Hold Time		6	ns
t_{WLWH}	WRB, RDB pulse width	41		ns
t_{AVWL}	Separated Address Bus Setup Time	5		ns
t_{WHAX}	Separated Address Bus Hold Time	6		ns
t_{WHWL}	Period between sequenced R/W accesses	150		ns



Picture 14-2 Timing for Separated Read/Write Strobe

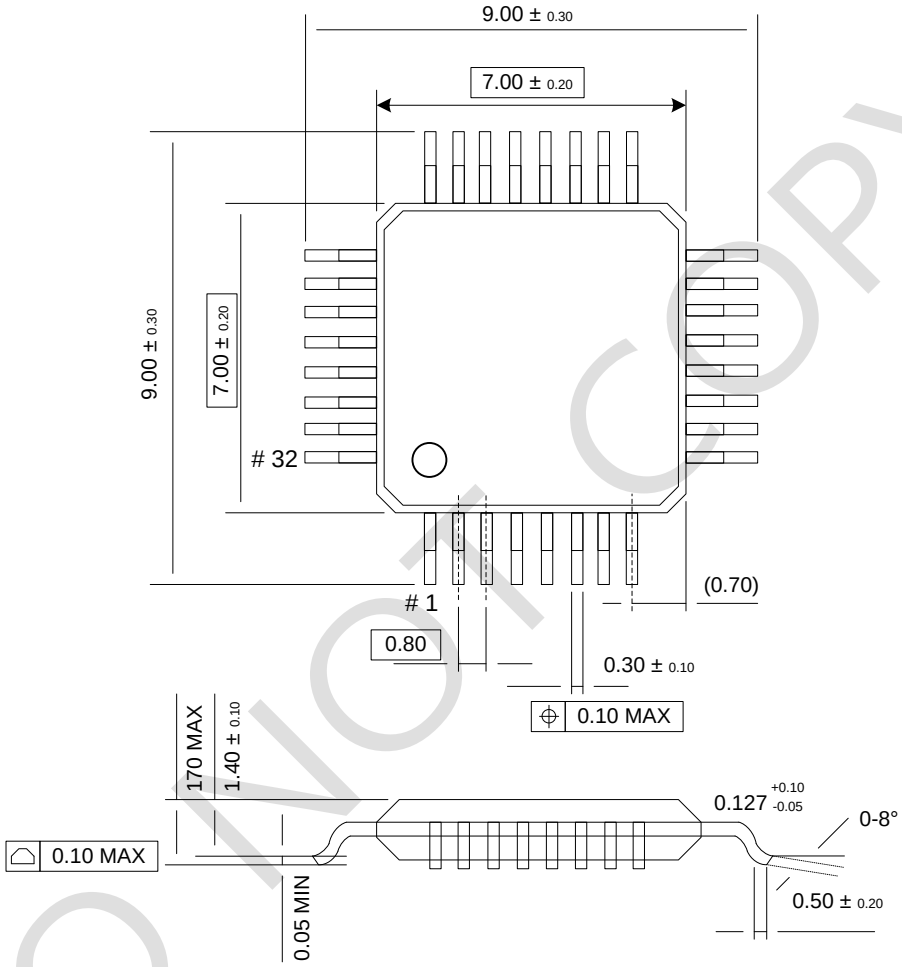
14.9.2 Timing for SPI compatible interface

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{SCKL}	SCK low pulse width	100		ns
t_{SCKH}	SCK high pulse width	100		ns
t_{SHDX}	SCK high to data changes	20		ns
t_{DXSH}	data changes to SCK high	20		ns
t_{SLDX}	SCK low to data changes		15	ns
t_{SLNH}	SCK low to NSS high	20		ns



PICTURE 14-3 Timing for SPI compatible interface

14.10 Package Information



PICTURE 14-4 32-PIN LQFP PACKAGE DIMEMSION

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Tel : (82) – (31) – 715 – 7117
Fax : (82) – (31) – 719 – 7551
Homepage : http://www.3alogics.com
Email : info@3alogics.com

7th Floor, Hyundai-office Bldg., 9-4,
Sunae-dong. Bundang-gu, Seongnam-si,
Gyeonggi-do,463-783,Korea