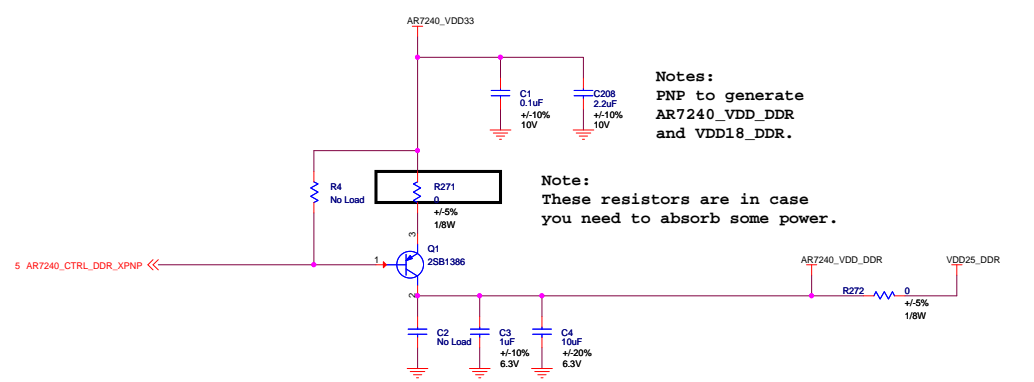
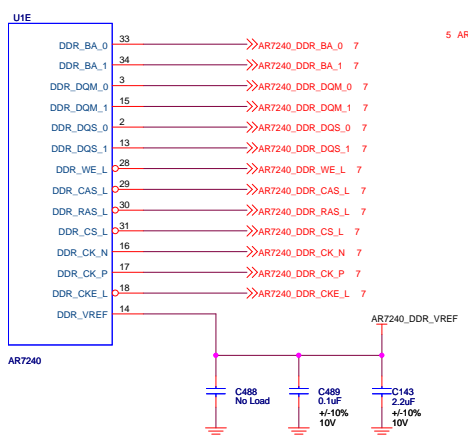
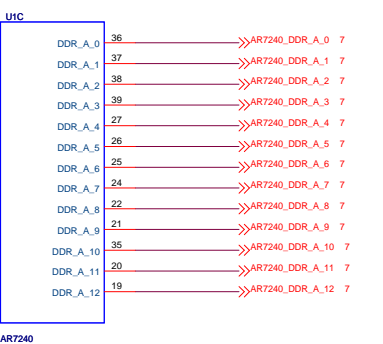
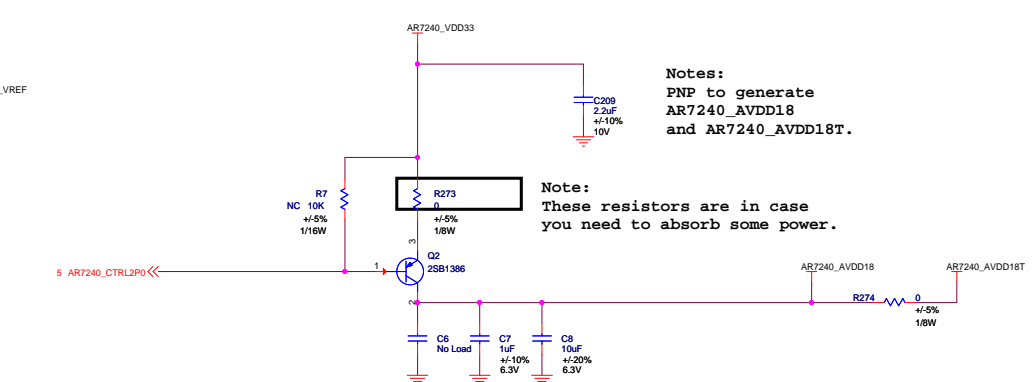
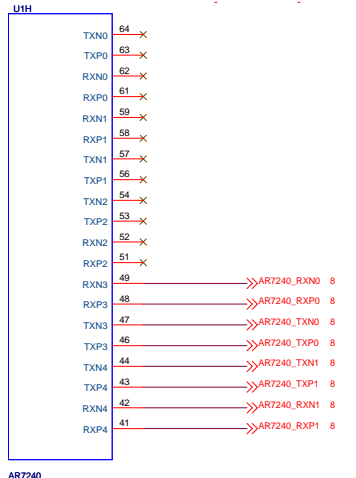


Notes:
 AR7240_CPUREGIN is the input to an internal regulator which generates AR7240_VDD12CD.



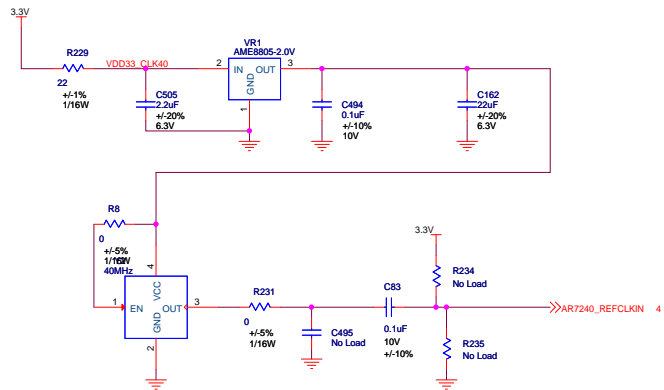
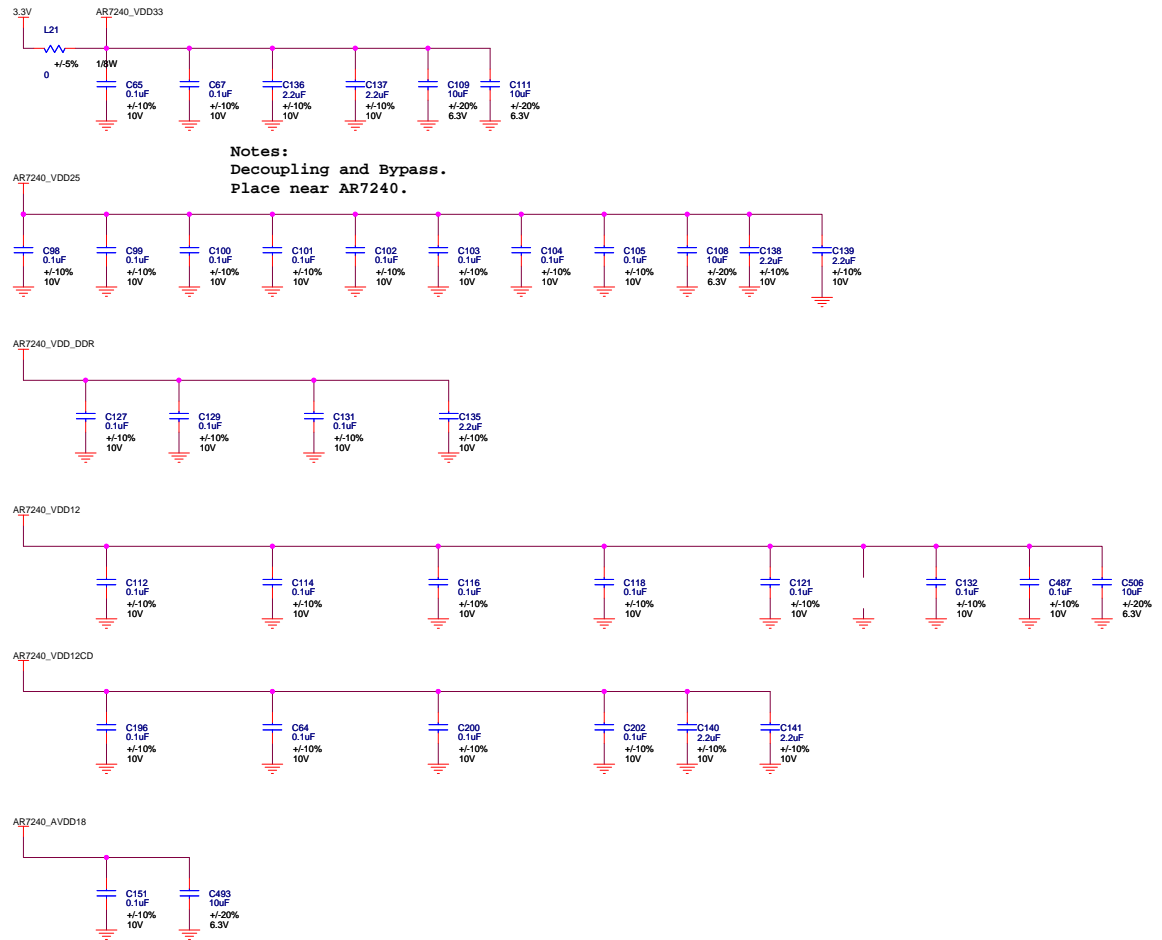
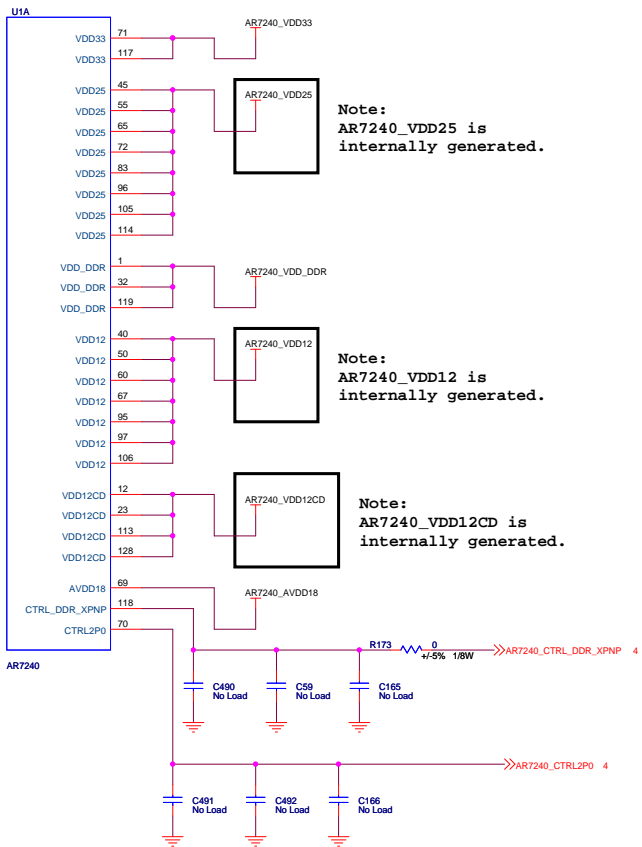
Notes:
 PNP to generate AR7240_VDD_DDR and VDD18_DDR.

Note:
 These resistors are in case you need to absorb some power.



Notes:
 PNP to generate AR7240_AVDD18 and AR7240_AVDD18T.

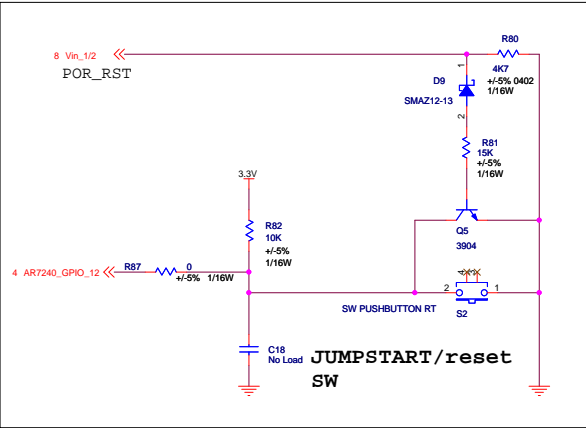
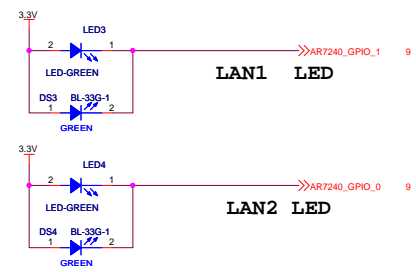
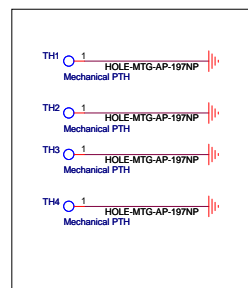
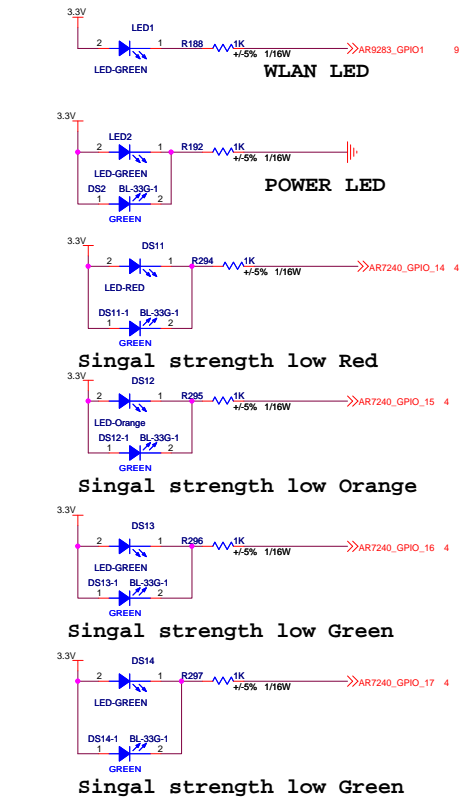
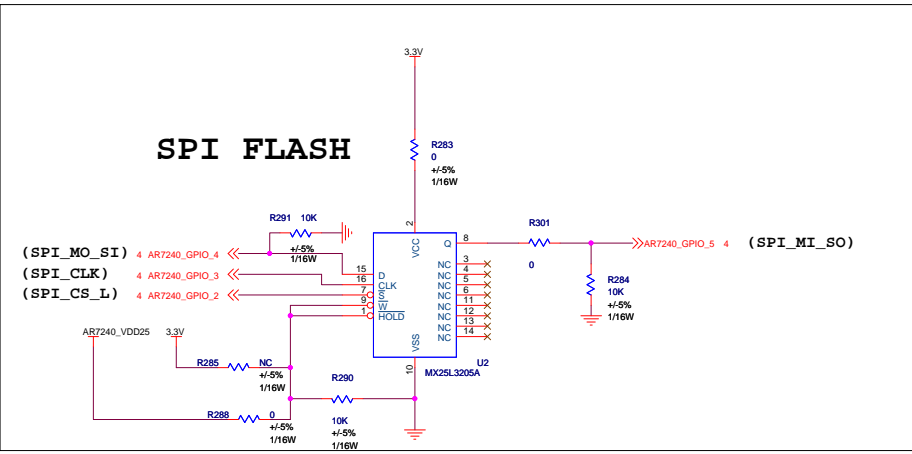
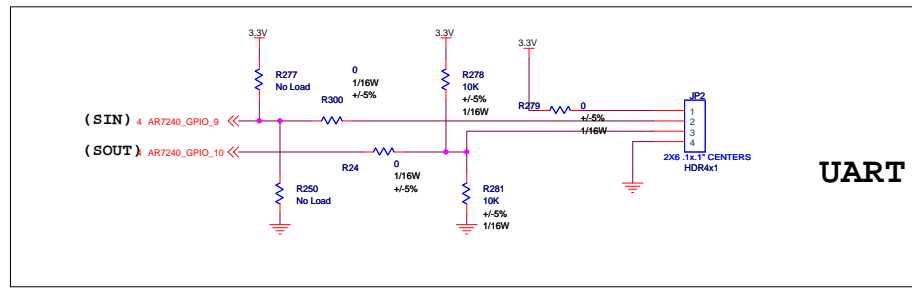
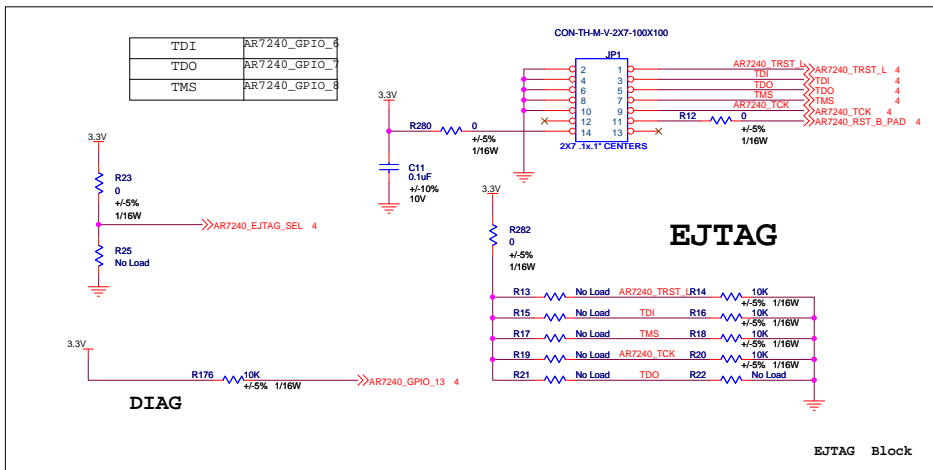
Note:
 These resistors are in case you need to absorb some power.



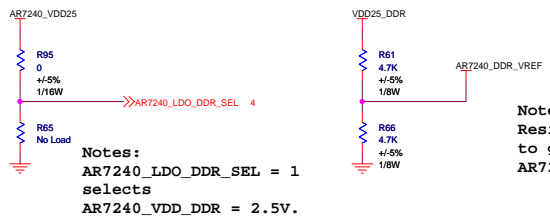
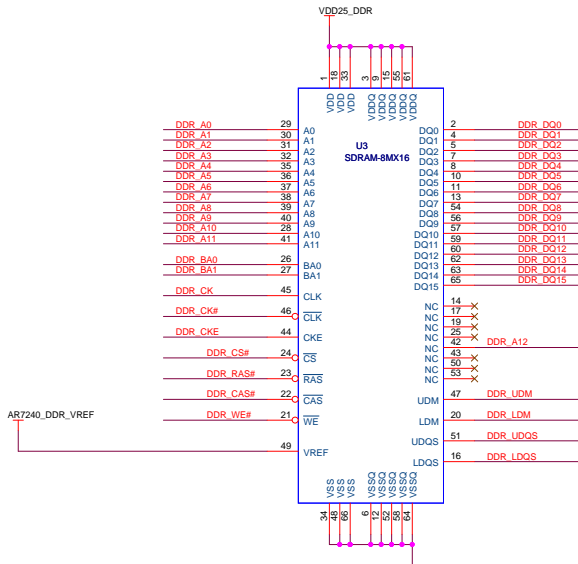
Notes:
To USE 40MHZ OSC for AR9283:
R11, C85, R141 are loaded
C143=0ohm
C142, Y2 are not loaded
(Both OPT1 and OPT2 are configured this way.)

To USE 40MHZ XTAL for AR9283:
R11, C85, R141 are not loaded
C142=C143=22pF
Y2 is loaded

40MHz OSC

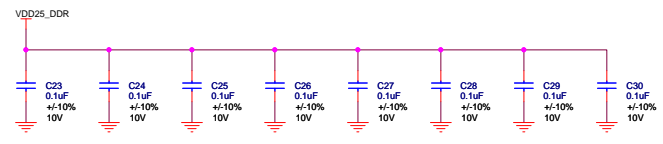
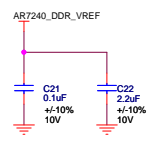


DDR

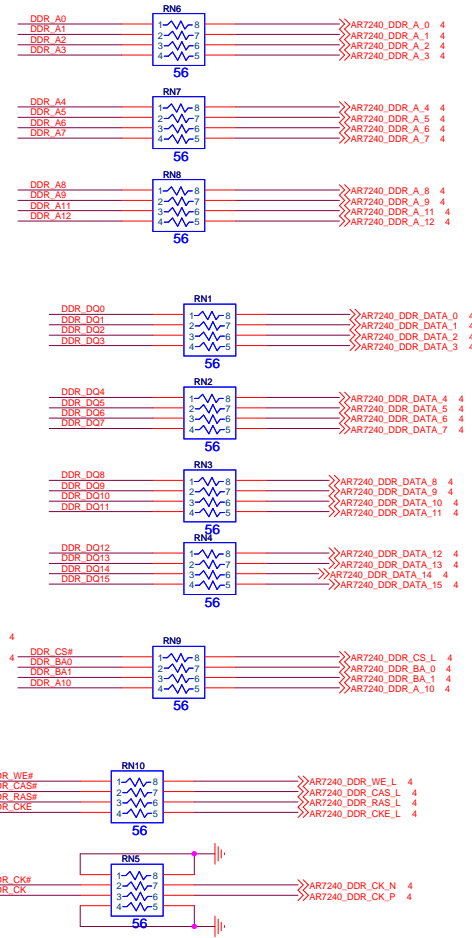


Notes:
AR7240_LDO_DDR_SEL = 1
selects
AR7240_VDD_DDR = 2.5V.

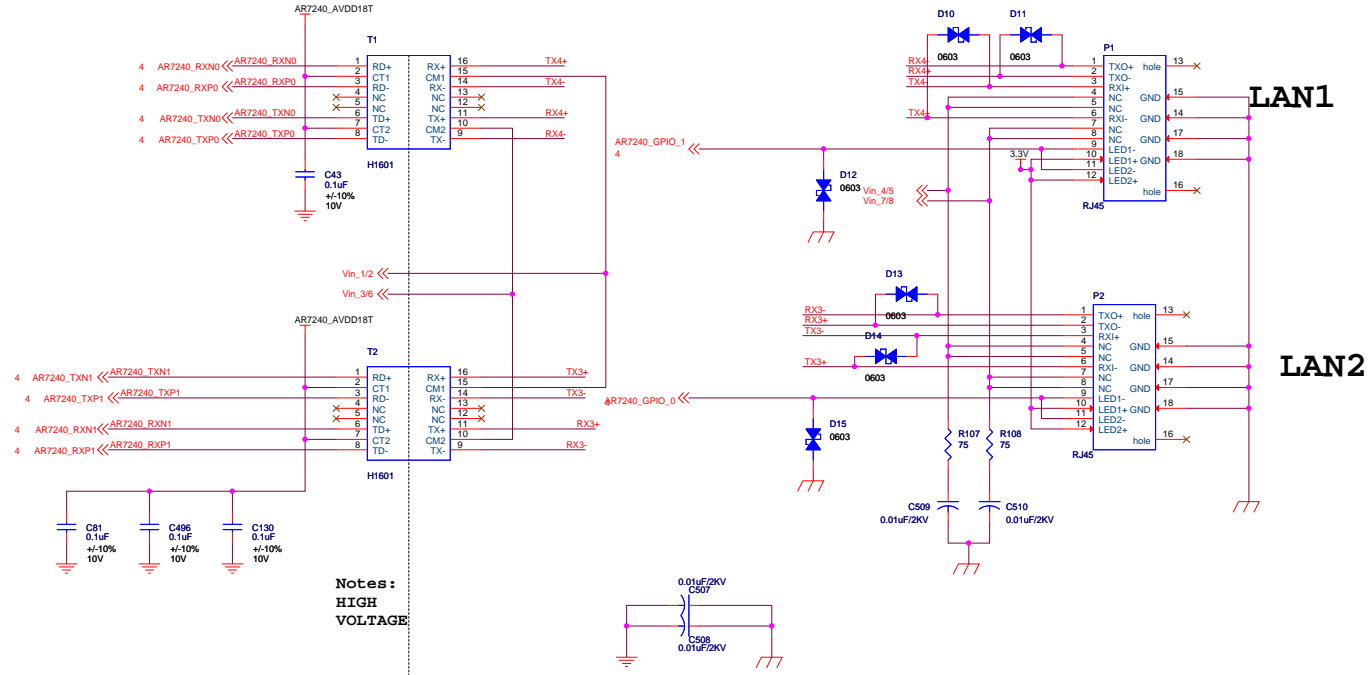
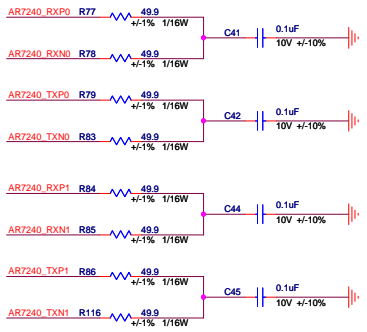
Notes:
Decoupling and Bypass.
Place near DDR.



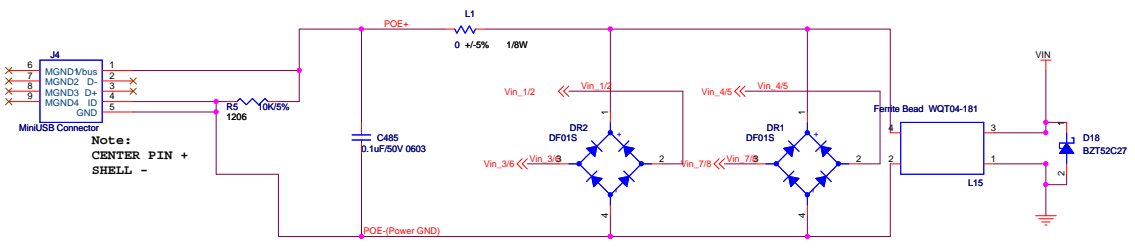
Notes:
Place Rs near DDR.



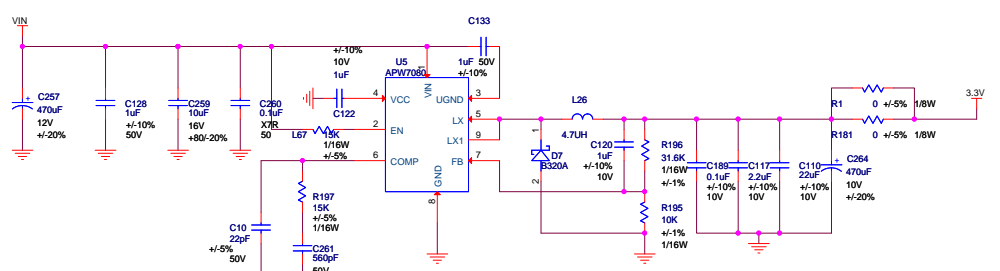
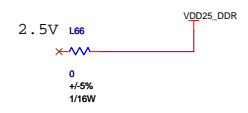
Notes:
Resistor divider
to generate
AR7240_VREF.



Notes:
HIGH
VOLTAGE

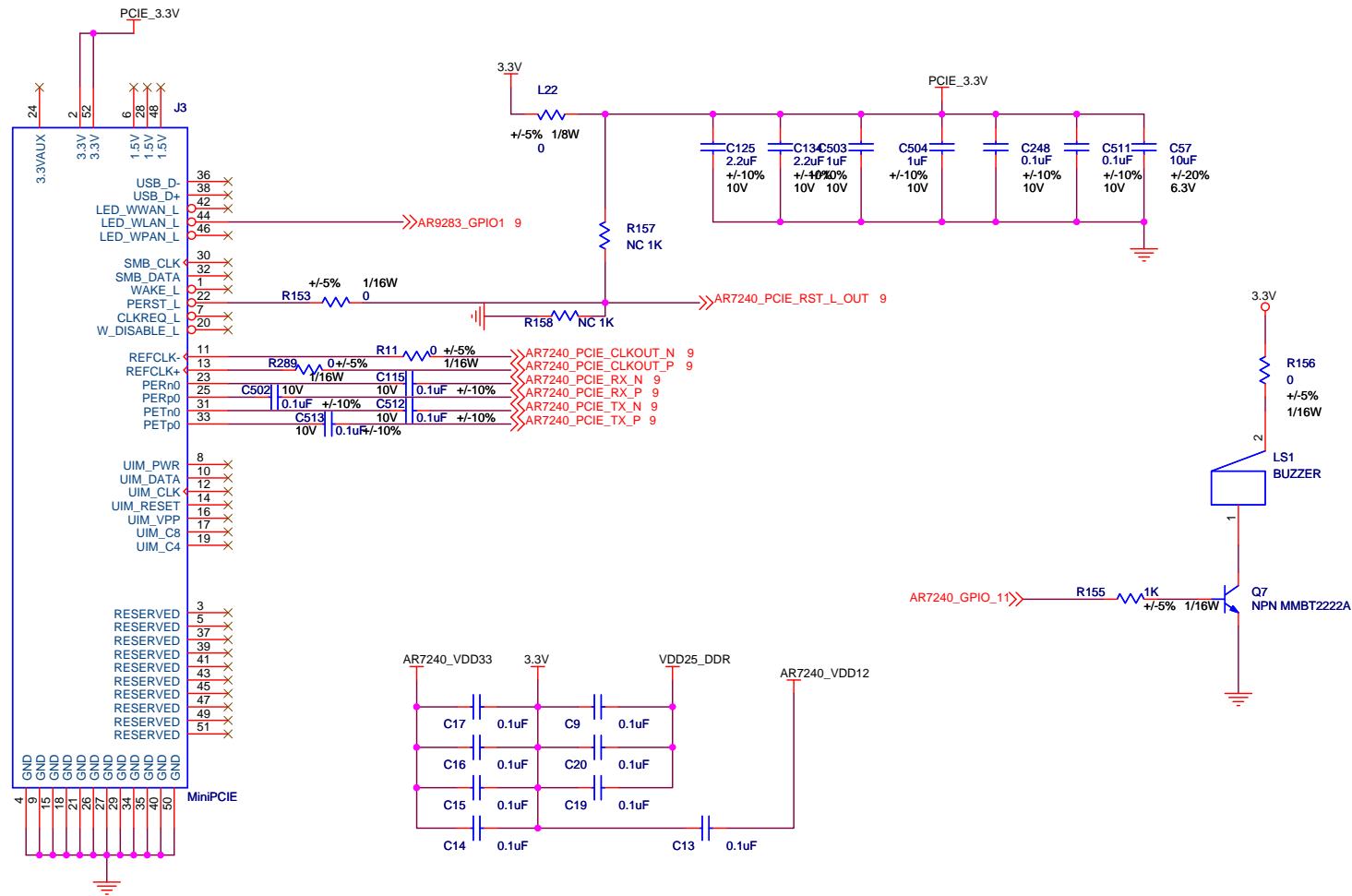


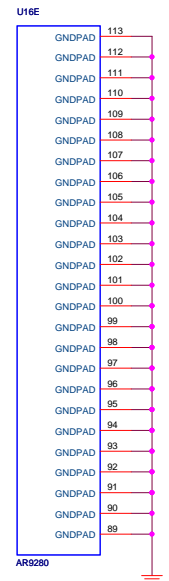
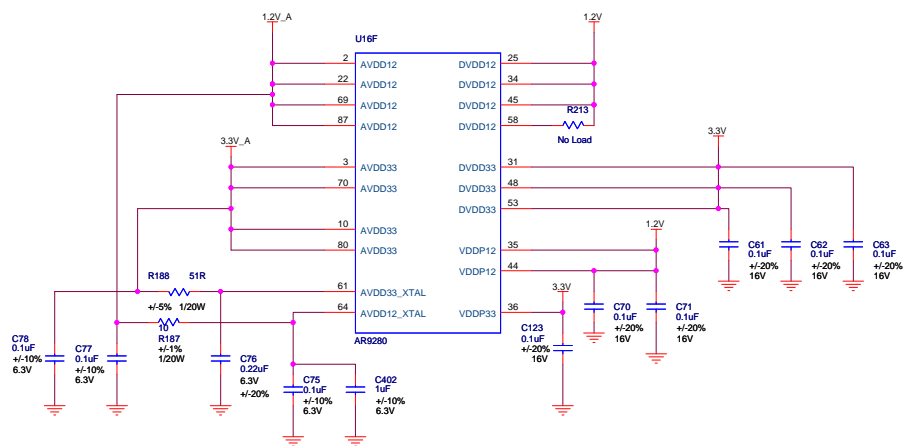
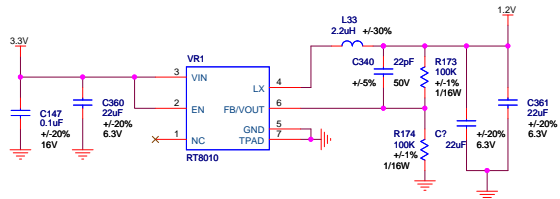
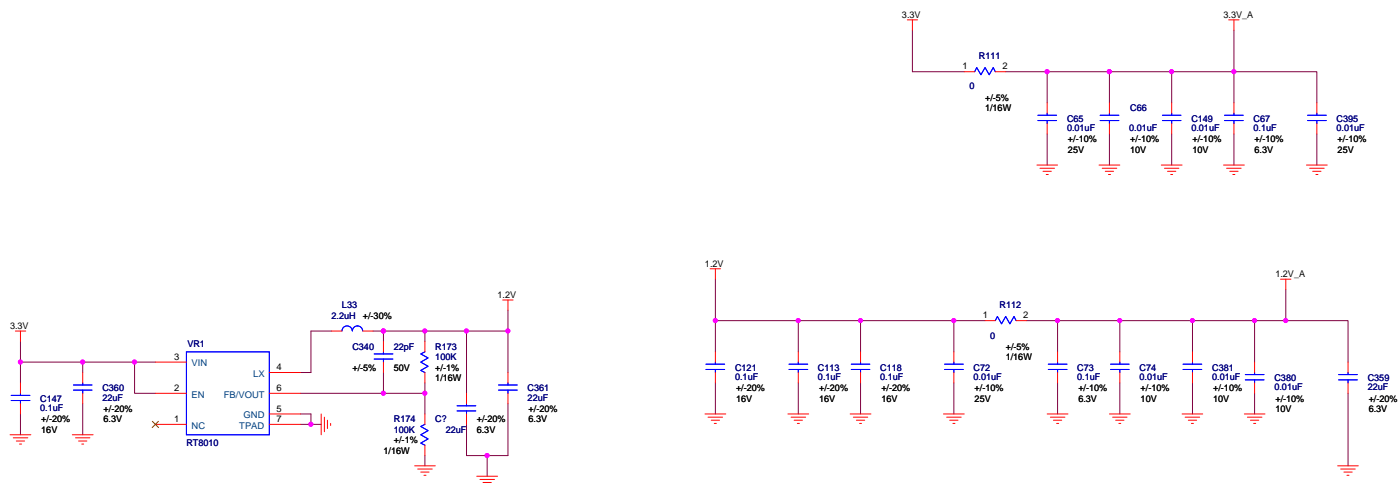
Note:
CENTER PIN +
SHELL -



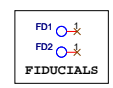
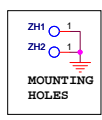
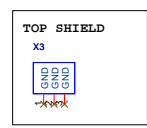
NOTE:
 $V_{out} = 0.8 \times (1 + R1/R2) = 0.8 \times (1 + 31.6/10)$
 $= 3.328V$

3.3V Output

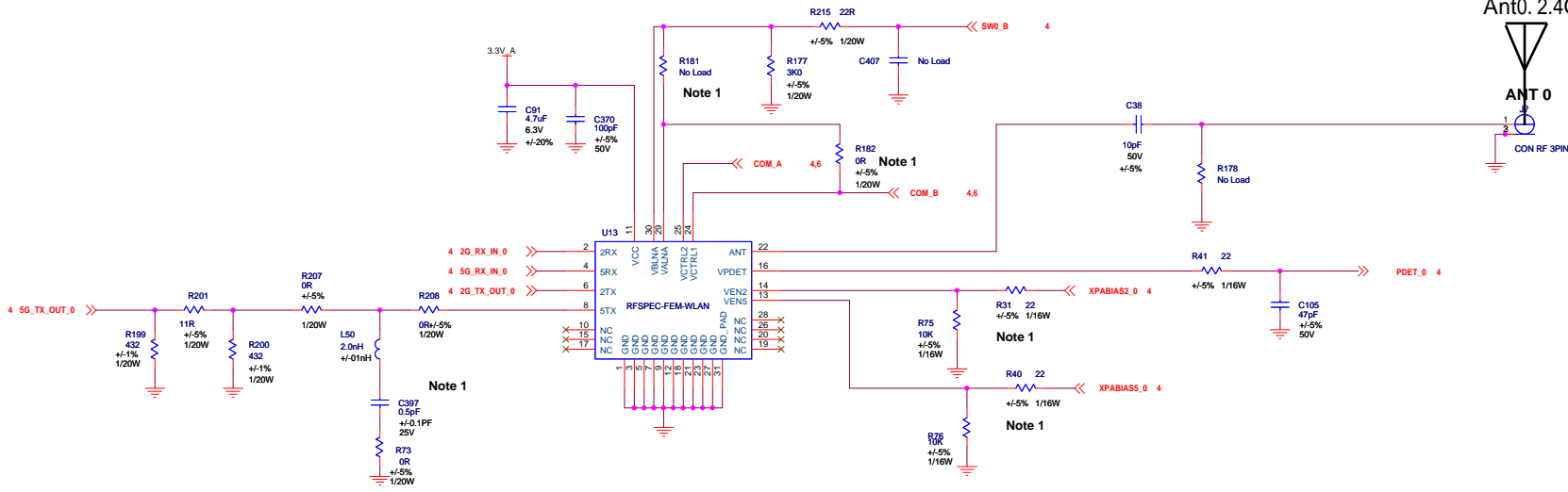




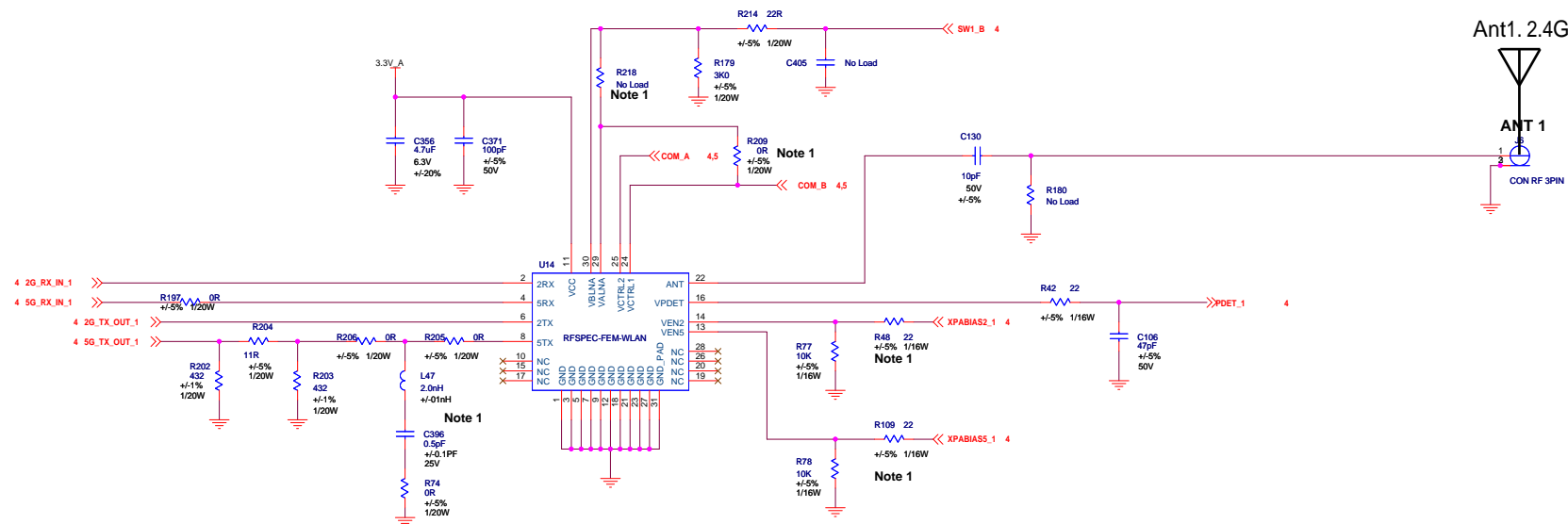
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Ant0. 2.4G/5.2G/5.8G



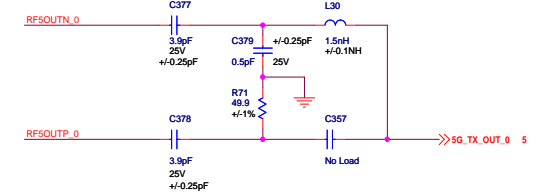
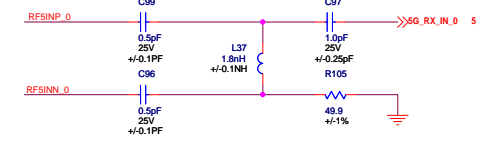
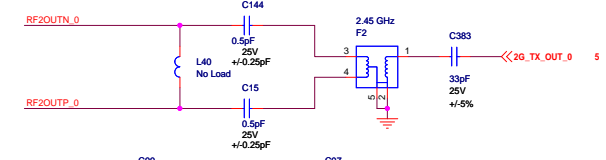
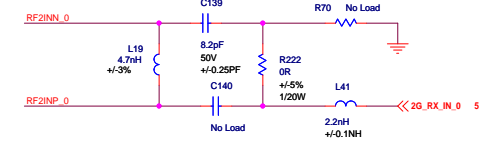
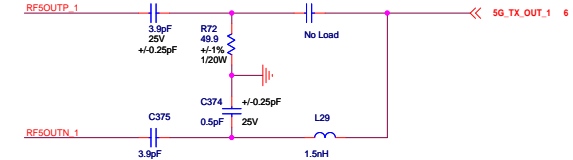
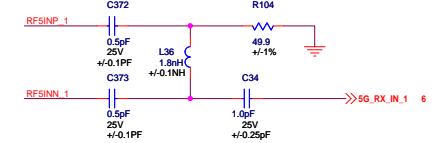
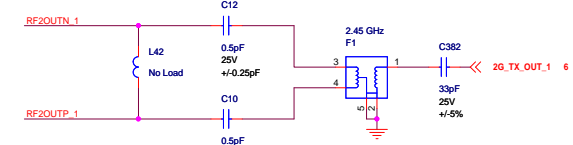
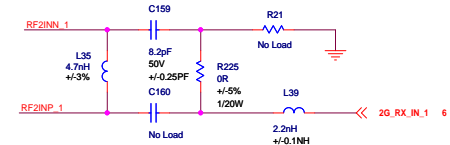
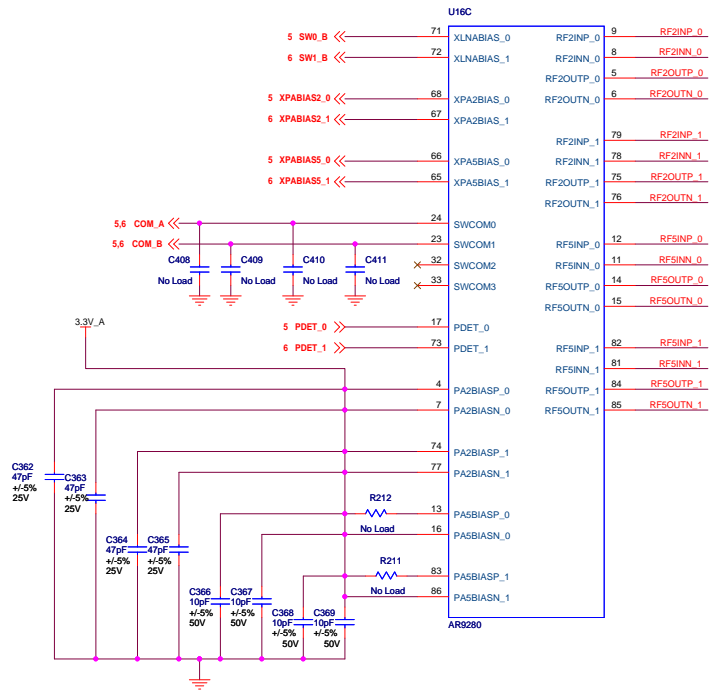
Ant1. 2.4G/5.2G/5.8G

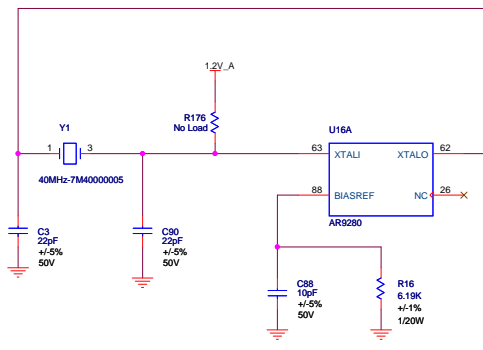
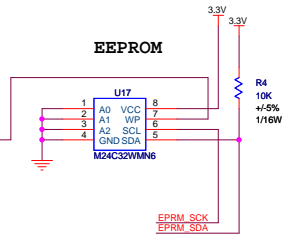
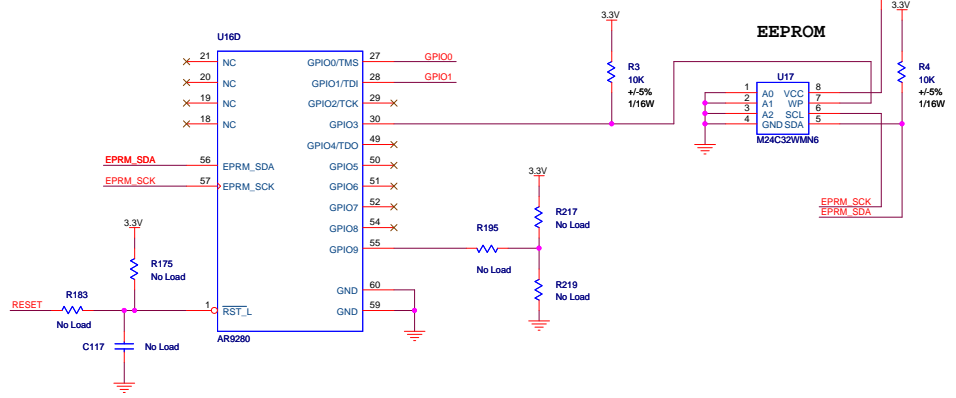
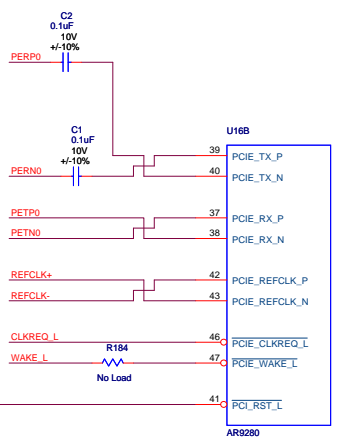
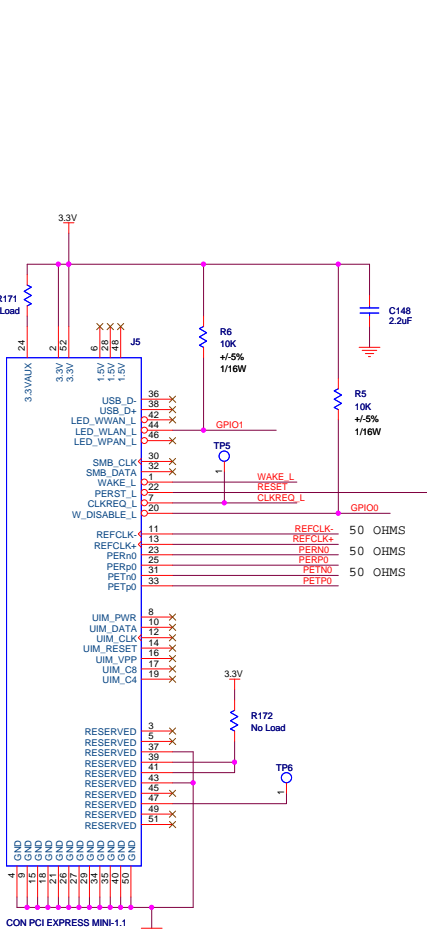


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