WLS1271L

WLAN Functional Blocks

The DR-WLS1271L-102 WLAN architecture includes a digital radio processor and a point-to-multipoint baseband core function. The architecture is based on a single-processor ARM core. The device includes on-chip peripherals to enable easy communication between a host system and the WLAN core function.

WLAN SDIO Transport Layer

SDIO is the WLAN host interface in the DR-WLS1271L-102. This interface is a standard SDIO interface (SDIO Version 2.0), supporting a maximum clock rate of 26 MHz. The DR-WLS1271L-102 SDIO also supports the following features:

- 4-bit data bus
- Functions number 0 and 2
- Multi-Block data transfer
- The SDIO interface is used for WLAN. The WLAN block uses function 2. Function 0 is used for the common I/O area.

WLAN MAC

The DR-WLS1271L-102 MAC implements the IEEE standard 802.11 MAC sub-layer using both dedicated hardware and embedded firmware. The MAC hardware implements real-time functions, including access protocol management, encryption and decryption.

WLAN Baseband Processor

The DR-WLS1271L-102 baseband processor sits between the on-chip MAC and the radio. The DR-WLS1271L-102 baseband processor implements the IEEE 802.11b/g/n PHY sub-layers and has been optimized to perform well in conditions of high multipath and noise.

WLAN RF Radio

The DR-WLS1271L-102 radio is a highly integrated Digital Radio Processor (DRP) designed for 802.11b/g/n applications. The DR-WLS1271L-102 RF interface is a single-band RF front end for 2.4 GHz 802.11b/g/n applications.

BT Functional Blocks

The DR-WLS1271L-102 BT architecture comprises a digital radio processor and a point-to-multipoint baseband core function. The architecture is based on a single-processor ARM core. The device includes on-chip peripherals to enable easy communication between a host system and the Bluetooth core function.