Stereo FM Transmitter circuit operation

This stereo FM transmitter is capable of broadcasting good quality. It's ideal for broadcasting music from a CD player or from any other source so that it can be picked up in another location.

For example, if you don't have a CD player in you car, you can use the transmitter to broadcast signals from a portable CD player to your car's radio. Alternatively, you might want to use the transmitter to broadcast signals from your lounge-room CD player to an FM receiver located in another part of the house or by the pool.

Because it's based on a single IC, this unit is a snack to build and fits easily into a small plastic utility box. It broadcasts on the FM band (88-108MHz) so that its signal can be received on any standard FM tuner or portable radio.

DIP switch is used to select one of 7 preset frequencies. These are available in ranges covering 106.7-107.9MHz in 0.2MHz steps.

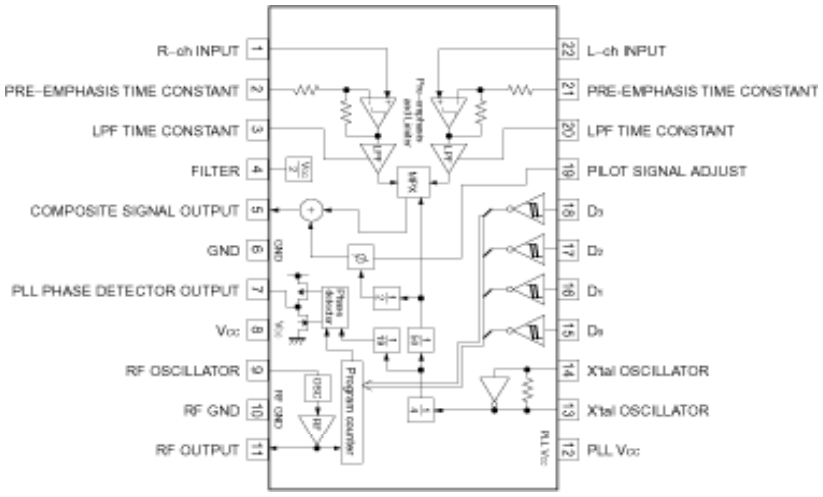

Fig.1: block diagram of the Rohm BH1417F stereo FM transmitter IC.

BH1417F transmitter IC

Fig.1 shows the internal features of the BH1417F. It includes all the processing circuitry required for stereo FM transmission and also the crystal control section which provides precise frequency locking.

As shown, the BH1417F includes two separate audio processing sections, for the left and right channels. The left-channel audio signal is applied to pin 22 of the chip, while the right channel signal is applied to pin 1. These audio signals are then applied to a pre-emphasis circuit which boosts those frequencies above a 50ms time constant (ie, those frequencies above 3.183kHz) prior to transmission.

Basically, pre-emphasis is used to improve the signal-to-noise ratio of the received FM signal. It works by using a complementary de-emphasis circuit in the receiver to attenuate the boosted treble

frequencies after demodulation, so that the frequency response is restored to normal. At the same time, this also significantly reduces the hiss that would otherwise be evident in the signal.

The amount of pre-emphasis is set by the value of the capacitors connected to pins 2 & 21 (note: the value of the time constant = 22.7kΩ x the capacitance value). In our case, we use 2.2nF capacitors to set the pre-emphasis to 50μs which is the Australian FM standard.

Signal limiting is also provided within the pre-emphasis section. This involves attenuating signals above a certain threshold, to prevent overloading the following stages. That in turn prevents over-modulation and reduces distortion.

The pre-emphasised signals for the left and right channels are then processed through two low-pass filter (LPF) stages, which roll off the response above 15kHz. This rolloff is necessary to restrict the bandwidth of the FM signal and is the same frequency limit used by commercial broadcast FM transmitters.

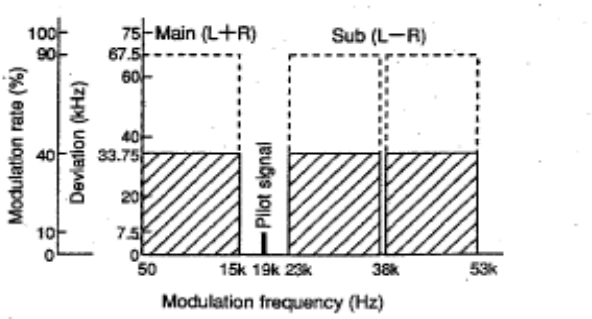

Fig.2: the frequency spectrum of the composite stereo FM signal. Note the spike of the pilot tone at 19kHz.

The outputs from the left and right LPFs are in turn applied to a multiplex (MPX) block. This is used to effectively produce sum (left plus right) and difference (left - right) signals which are then modulated onto a 38kHz carrier. The carrier is then suppressed (or removed) to provide a double-sideband suppressed carrier signal. It is then mixed in a summing (+) block with a 19kHz pilot tone to give a composite signal output (with full stereo encoding) at pin 5.

The phase and level of the 19kHz pilot tone are set using a capacitor at pin 19.

Fig.2 shows the spectrum of the composite stereo signal. The (L+R) signal occupies the frequency range from 0-15kHz. By contrast, the double sideband suppressed carrier signal (L-R) has a lower sideband which extends from 23-38kHz and an upper sideband from 38-53kHz. As noted, the 38kHz carrier is not present.

The 19kHz pilot tone is present, however, and this is used in the FM receiver to reconstruct the 38kHz subcarrier so that the stereo signal can be decoded.

The 38kHz multiplex signal and 19kHz pilot tone are derived by dividing down the 7.6MHz crystal oscillator located at pins 13 & 14. The frequency is first divided by four to obtain 1.9MHz and then divided by 50 to obtain 38kHz. This is then divided by two to derive the 19kHz pilot tone.

In addition, the 1.9MHz signal is divided by 19 to give a 100kHz signal. This signal is then applied to the phase detector which also monitors the program counter output. This program counter is actually a programmable divider which outputs a divided down value of the RF signal.

The division ratio of this counter is set by the voltage levels at inputs D0-D3 (pins 15-18). For example, when D0-D3 are all low, the programmable counter divides by 877. Thus, if the RF oscillator is running at 106.7MHz, the divided output from the counter will be 100kHz and this matches the frequency divided down from the 7.6MHz crystal oscillator (ie, 7.6MHz divided by 4 divided by 19).

In practice, the phase detector output at pin 7 produces an error signal to control the voltage applied to a varicap diode. This varicap diode (VC1) is shown on the main circuit diagram (Fig.3) and forms part of the RF oscillator at pin 9. Its frequency of oscillation is determined by the value of the inductance and the total parallel capacitance.

Since the varicap diode forms part of this capacitance, we can alter the RF oscillator frequency by varying its value. In operation, the varicap diode's capacitance varies in proportion to the DC voltage applied to it by the output of the PLL phase detector.

In practice, the phase detector adjusts the varicap voltage so that the divided RF oscillator frequency is 100kHz at the program counter output. If the RF frequency drifts high, the frequency output from the programmable divider rises and the phase detector will "see" an error between this and the 100kHz provided by the crystal division.

As a result, the phase detector reduces the DC voltage applied to the varicap diode, thereby increasing its capacitance. And this in turn decreases the oscillator frequency to bring it back into "lock".

Conversely, if the RF frequency drifts low, the programmable divider output will be lower than 100kHz. This means that the phase detector now increases the applied DC voltage to the varicap to decrease its capacitance and raise the RF frequency. As a result, this PLL feedback arrangement ensures that the programmable divider output remains fixed at 100kHz and thus ensures stability of the RF oscillator.

By changing the programmable divider we can change the RF frequency. So, for example, if we set the divider to 1079, the RF oscillator must operate at 107.9MHz for the programmable divider output to remain at 100kHz.

Frequency modulation

Of course, in order to transmit audio information, we need to frequency modulate the RF oscillator. We do that by modulating the voltage applied to the varicap diode using the composite signal output at pin 5.

Note, however, that the average frequency of the RF oscillator (ie, the carrier frequency) remains fixed, as set by the programmable divider (or program counter). As a result, the transmitted FM signal varies either side of the carrier frequency according to the composite signal level - ie, it is frequency modulated.

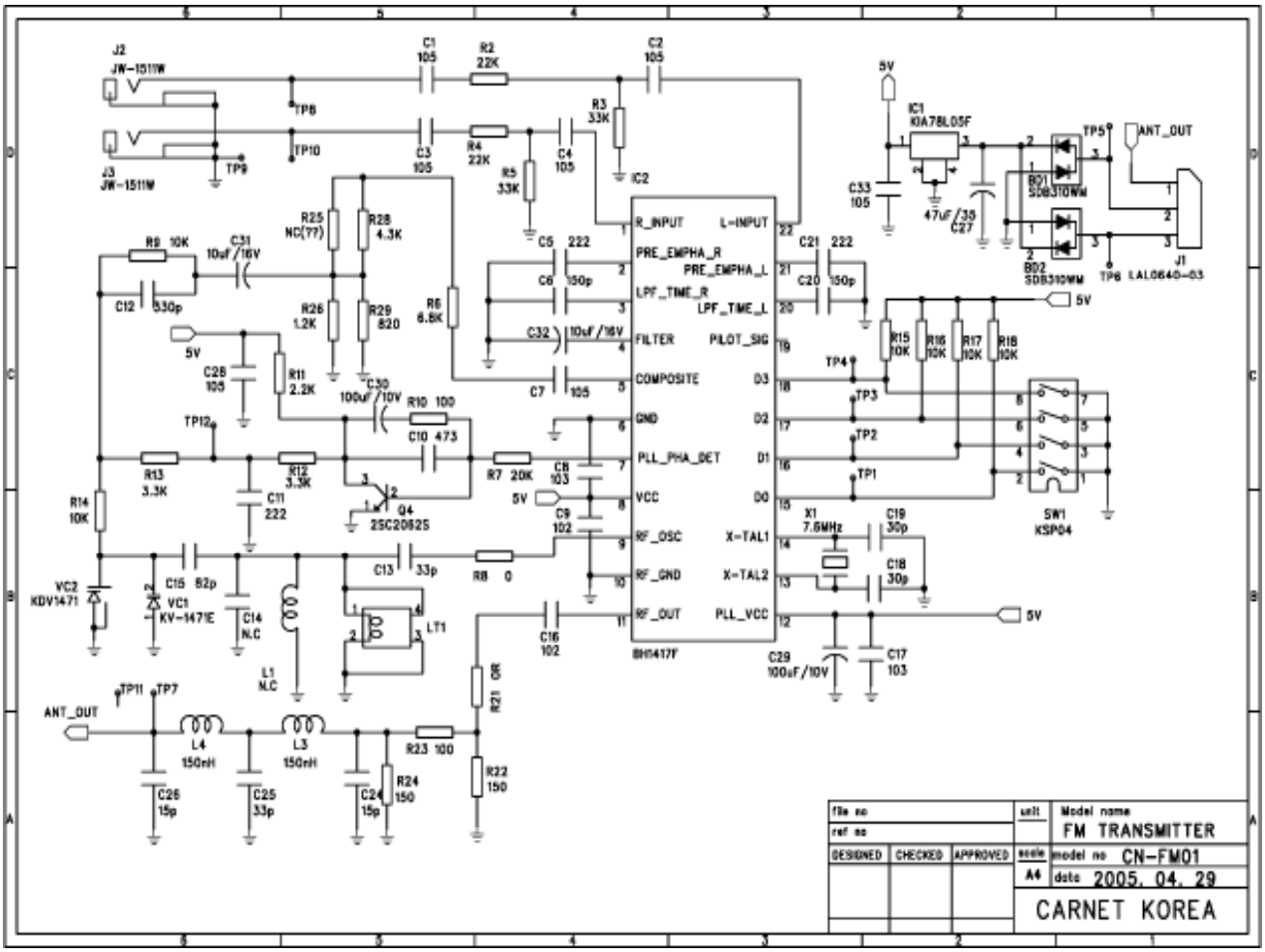

Fig.3: the complete circuit of the Stereo FM Transmitter.

Circuit details

Refer now to Fig.3 for the full circuit of the Stereo FM Micromitter. As expected, IC1 forms the main part of the circuitry with a handful of other components added to complete the FM stereo transmitter.

The left and right audio input signals are fed in via 1µF bipolar capacitors and then applied to attenuator circuits consisting of 22kΩ resistors and 33kΩ resistors. From there, the signals are coupled into pins 1 & 22 of IC1 via 1µF electrolytic capacitors.

Note that the 1µF bipolar capacitors are included to prevent DC current flow due to any DC offsets at the signal source outputs. Similarly, the 1µF capacitors on pins 1 & 22 are necessary to prevent DC current in the trimpots, since these two input pins are biased at half-supply. This half-supply rail is decoupled using a 10µF capacitor at pin 4 of IC1.

The 2.2nF pre-emphasis capacitors are at pins 2 & 21, while the 150pF capacitors at pins 3 & 20 set the low-pass filter rolloff point. The pilot level can be set with a capacitor at pin 19 - however, this is not usually necessary as the level is generally quite suitable without adding the capacitor.

In fact, adding a capacitor here only reduces the stereo separation because the pilot tone phase is altered compared to the 38kHz multiplex rate.

The 7.6MHz oscillator is formed by connecting a 7.6MHz crystal between pins 13 & 14. In practice, this crystal is connected in parallel with an internal inverter stage. The crystal sets the frequency of oscillation, while the 30pF capacitors provide the correct loading.

The programmable divider (or program counter) is set using switches at pins 15, 16, 17 & 18 (D0-D3). These inputs are normally held high via 10kΩ resistors and pulled low when the switches are closed. Table 1 shows how the switches are set to select one of 14 different transmission frequencies.

The RF oscillator output is at pin 9. This is a Colpitts oscillator and is tuned using inductor LT1, the 82pF fixed capacitors and varicap diode VC1.

The 82pF fixed capacitor performs two functions. First, it blocks the DC voltage applied to VC1 to prevent current from flowing into LT1. And second, because it is in series with VC1, it reduces the effect of changes in the varicap capacitance, as "seen" by pin 9.

This, in turn, reduces the overall frequency range of the RF oscillator due to changes in the varicap control voltage and allows better phase lock loop control.

Similarly, the 10pF capacitor prevents DC current flow into LT1 from pin 9. Its low value also means that the tuned circuit is only loosely coupled and this allows a higher Q factor for the tuned circuit and easier starting of the oscillator.

Modulating the oscillator

The composite output signal appears at pin 5 and is fed via a 1µF capacitor to R25,28/ R26,R29 resistor. This resistor sets the modulation depth. From there, the attenuated signal is fed via another 10µF capacitor and two 10kΩ resistors to varicap diode VC1.

As mentioned previously, the phase lock loop control (PLL) output at pin 7 is used to control the carrier frequency. This output drives high-gain Darlington transistor Q4 and this, in turn, applies a control voltage to VC1 via two 3.3kΩ series resistors and the 10kΩ isolating resistor.

The 2.2nF capacitor at the junction of the two 3.3kΩ resistors provides high-frequency filtering.

Additional filtering is provided by the 100µF capacitor and 100Ω resistor connected in series between Q4's base and collector. The 100Ω resistor allows the transistor to respond to transient changes, while the 100µF capacitor provides low-frequency filtering. Further high-frequency filtering is provided by the 47nF capacitor connected directly between Q4's base and collector.

The 2.2kΩ resistor connected to the 5V rail provides the collector load. This resistor pulls Q4's collector high when the transistor is off.

FM output

The modulated RF output appears at pin 11 and is fed to a passive LC bandpass filter. Its job is to remove any harmonics produced by the modulation and in the RF oscillator output. Basically, the filter passes frequencies in the 88-108MHz band but rolls off signal frequencies above and below this.

The filter has a nominal impedance of 75Ω and this matches both IC1's pin 11 output and the following attenuator circuit.

Two 150Ω series resistors the attenuator and this reduces the signal level into the antenna. This attenuator is necessary to ensure that the transmitter operates at the legal allowable limit of about 10µW.

Power supply

Power for the circuit is derived from car battery power 9-16V.
Regulator IC(78L05) provides a steady +5V rail to power the circuit.