Prepared (also subject responsible if other)		No.		
EAB/PDR/GRB Larry Lindström		TA8AKRC11819-1		
Approved	Checked	Date	Rev	Reference
KI/EAB/PDR/GRB (L Lindström)		2005-05-26	A	

Exhibit 12 – Cover Sheet

Contents

1 2.1033(c) Circuit Description

1.1 (2) FCC Identifier: TA8AKRC11819-1

This RU (Radio Unit) consists of one synthesized transmitter operating in the frequency band of 1930 to 1990 MHz.
There are twelve Channels available. The transmitter is capable of operation in a WCDMA system. For each channel there are 64 code slots available, each containing digital speech or data for QPSK or 16QAM.

1.2 (4) Type of Emission: 4M17F9W

1.3 (5) Frequency range: 1930 to 1990 MHz

1.4 (6) Range of Operating Power:

This transmitter is designed to supply a nominal power level of 46 dBm at the output connector.

1.5 (7) Maximum Power Rating:

The maximum power rating with one RU under environmental and supply voltage variations is equal to 46 dBm plus a power level tolerance of + 1.0 dB. Therefore the maximum output power is 47 dBm equal to 50 Watt at the output connector of the RU.

1.6 (8) Final Amplifier Voltage and Current in normal operation

	Average Output Power 46 dBm Values for U1308
Voltage	30 Volt DC
Current	2.1 Amps DC

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1.7 (10) Frequency Stabilizing Circuit Description

The RU has a stabilizing clock circuit of 30 MHz. This clock is phase-locked to an incoming 30.72 MHz clock reference from the CBU board via the RUIF board. The radio (transmitter and receiver) in the RU has a 10 MHz reference, which is locked to the 30 MHz clock above.
The TX (transmitter) part has a Local Oscillator (PLL) which is mixed with the base band I and Q signals in the I&Q-modulator to the actual transmit frequency and then fed to the Power Amplifier. The Local Oscillator is locked to the 10 MHz reference.

The 30.72 MHz clock reference is generated in a voltage controlled oscillator placed in the CBU Board. This clock is phase-locked to an 8 kHz oscillator also placed in the CBU. This oscillator is in turn locked to the extracted frame-sync of 8 kHz from the PCM Transmission Link. As an option can the CBU be directly frequency synchronized with a GPS source.

1.8 (10) Spurious and Harmonic Suppression

Spurious and harmonic suppression is achieved by using two separate bandpass filters of ceramic type in the exciter (in RU). A filter module at the output (in RU) works like a bandpass filter around the carrier

1.9 (10) Limiting Power

The RU (Radio Unit) measures the output power at its output connector via a RF-detector and the detected value is used by the power loop control block to steer the variable gain amplifiers in the exciter amplifier. The dynamic power control included in the WCDMA system is controlled by the exciter amplifier in the RU.

1.10 (10) Digital Modulation QPSK and 16QAM

5 Downlink spreading and modulation

5.1 Spreading

Figure 8 illustrates the spreading operation for all physical channels except SCH. The spreading operation includes a modulation mapper stage successively followed by a channelisation stage, an IQ combining stage and a scrambling stage. All the downlink physical channels are then combined as specified in sub subclause 5.1.5.

The non-spread downlink physical channels, except SCH, AICH, AP-ICH CD/CA-ICH, E-HICH and E-RGCH consist of a sequence of 3-valued digits taking the values 0, 1 and "DTX". Note that "DTX" is only applicable to those downlink physical channels that support DTX transmission.

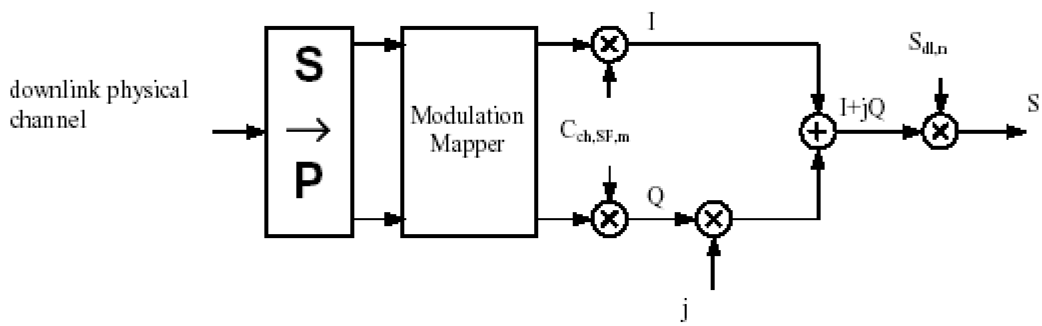

Figure 8: Spreading for all downlink physical channels except SCH

NOTE: Although subclause 5.1 has been reorganized in this release, the spreading operation as specified for the DL channels in the previous release remains unchanged.

5.1.1 Modulation mapper

Table 3A defines which of the IQ mapping specified in subclauses 5.1.1.1 and 5.1.1.2 may be used for the physical channel being processed.

Table 3A: IQ mapping

Physical channel	IQ mapping
HS-PDSCH	QPSK or 16QAM
All other channels (except the SCH)	QPSK

5.1.1.1 QPSK

For all channels, except AICH, AP-AICH, CD/CA-ICH, E-HICH and E-RGCH, the input digits shall be mapped to real-valued symbols as follows: the binary value "0" is mapped to the real value +1, the binary value "1" is mapped to the real value –1 and "DTX" is mapped to the real value 0. For the indicator channels using signatures (AICH, AP-AICH, CD/CA-ICH), the real-valued input symbols depend on the exact combination of the indicators to be transmitted as specified in [2] subclauses 5.3.3.7, 5.3.3.8 and 5.3.3.9.For the E-HICH and the E-RGCH the input is a real valued symbol sequence as specified in [2] Each pair of two consecutive real-valued symbols is first converted from serial to parallel and mapped to an I and Q branch. The definition of the modulation mapper is such that even and odd numbered symbols are mapped to the I and Q branch respectively. For all QPSK channels except the indicator channels using signatures, symbol number zero is defined as the first symbol in each frame or sub-frame. For the indicator channels using signatures, symbol number zero is defined as the first symbol in each access slot.

5.1.1.2 16QAM

In case of 16QAM, a set of four consecutive binary symbols n_k, n_{k+1}, n_{k+2}, n_{k+3} (with k mod 4 = 0) is serial-to-parallel converted to two consecutive binary symbols ($i_1 = n_k$, $i_2 = n_{k+2}$) on the I branch and two consecutive binary symbols ($q_1 = n_{k+1}$, $q_2 = n_{k+3}$) on the Q branch and then mapped to 16QAM by the modulation mapper as defined in table 3B.

The I and Q branches are then both spread to the chip rate by the same real-valued channelisation code $C_{ch,16,m}$. The channelisation code sequence shall be aligned in time with the symbol boundary. The sequences of real-valued chips on the I and Q branch are then treated as a single complex-valued sequence of chips. This sequence of chips from all multicodes is summed and then scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$. The scrambling code is applied aligned with the scrambling code applied to the P-CCPCH.

Table 3B: 16 QAM modulation mapping

$i_1q_1i_2q_2$	I branch	Q branch
0000	0.4472	0.4472
0001	0.4472	1.3416
0010	1.3416	0.4472
0011	1.3416	1.3416
0100	0.4472	-0.4472
0101	0.4472	-1.3416
0110	1.3416	-0.4472
0111	1.3416	-1.3416
1000	-0.4472	0.4472
1001	-0.4472	1.3416
1010	-1.3416	0.4472
1011	-1.3416	1.3416
1100	-0.4472	-0.4472
1101	-0.4472	-1.3416
1110	-1.3416	-0.4472
1111	-1.3416	-1.3416

5.1.2 Channelisation

For all physical channels (except SCH) the I and Q branches shall be spread to the chip rate by the same real-valued channelisation code $C_{ch,SF,m}$, i.e. the output for each input symbol on the I and the Q branches shall be a sequence of SF chips corresponding to the channelisation code chip sequence multiplied by the real-valued symbol. The channelisation code sequence shall be aligned in time with the symbol boundary.

5.1.3 IQ combining

The real valued chip sequence on the Q branch shall be complex multiplied with j and summed with the corresponding real valued chip sequence on the I branch, thus resulting in a single complex valued chip sequence.

5.1.4 Scrambling

The sequence of complex valued chips shall be scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$. In case of P-CCPCH, the scrambling code shall be applied aligned with the P-CCPCH frame boundary, i.e. the first complex chip of the spread P-CCPCH frame is multiplied with chip number zero of the scrambling code. In case of other downlink channels, the scrambling code shall be applied aligned with the scrambling code applied to the P-CCPCH. In this case, the scrambling code is thus not necessarily applied aligned with the frame boundary of the physical channel to be scrambled.

5.1.5 Channel combining

Figure 9 illustrates how different downlink channels are combined. Each complex-valued spread channel, corresponding to point S in Figure 8, may be separately weighted by a weight factor G_i. The complex-valued P-SCH and S-SCH, as described in [2], subclause 5.3.3.5, may be separately weighted by weight factors G_p and G_s. All downlink physical channels shall then be combined using complex addition.

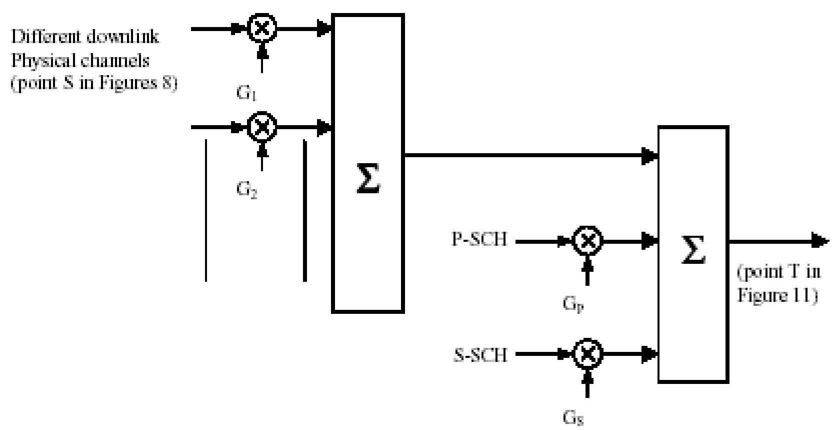

Figure 9: Combining of downlink physical channels

5.2 Code generation and allocation

5.2.1 Channelisation codes

The channelisation codes of figure 8 are the same codes as used in the uplink, namely Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between downlink channels of different rates and spreading factors. The OVSF codes are defined in figure 4 in subclause 4.3.1.

The channelisation code for the Primary CPICH is fixed to $C_{ch,256,0}$ and the channelisation code for the Primary CCPCH is fixed to $C_{ch,256,1}$.The channelisation codes for all other physical channels are assigned by UTRAN.

With the spreading factor 512 a specific restriction is applied. When the code word $C_{ch,512,n}$, with n=0,2,4….510, is used in soft handover, then the code word $C_{ch,512,n+1}$ is not allocated in the cells where timing adjustment is to be used. Respectively if $C_{ch,512,n}$, with n=1,3,5….511 is used, then the code word is not allocated in the cells where timing adjustment is to be used. This restriction shall not apply in cases where timing adjustments in soft handover are not used with spreading factor 512.

When compressed mode is implemented by reducing the spreading factor by 2, the OVSF code used for compressed frames is:

- $C_{ch,SF/2,\_n/2\_}$ if ordinary scrambling code is used.
- $C_{ch,SF/2,n \bmod SF/2}$ if alternative scrambling code is used (see subclause 5.2.2);

where $C_{ch,SF,n}$ is the channelisation code used for non-compressed frames.

For F-DPCH, the spreading factor is always 256.

In case the OVSF code on the PDSCH varies from frame to frame, the OVSF codes shall be allocated in such a way that the OVSF code(s) below the smallest spreading factor will be from the branch of the code tree pointed by the code with smallest spreading factor used for the connection, which is called PDSCH root channelisation code. This means that all the codes for this UE for the PDSCH connection can be generated according to the OVSF code generation principle from the PDSCH root channelisation code i.e. the code with smallest spreading factor used by the UE on PDSCH.

In case of mapping the DSCH to multiple parallel PDSCHs, the same rule applies, but all of the branches identified by the multiple codes, corresponding to the smallest spreading factor, may be used for higher spreading factor allocation i.e. the multiple codes with smallest spreading factor can be considered as PDSCH root channelisation codes.

For HS-PDSCH, the spreading factor is always 16.

For HS-SCCH, the spreading factor is always 128.

Channelisation-code-set information over HS-SCCH is mapped in following manner: the OVSF codes shall be allocated in such a way that they are positioned in sequence in the code tree. That is, for P multicodes at offset O the following codes are allocated:

Cch,16,O … Cch,16, O+P-1

The number of multicodes and the corresponding offset for HS-PDSCHs mapped from a given HS-DSCH is signaled by HS-SCCH.

For E-HICH and for E-RGCH, the spreading factor shall always be 128. In each cell, the E-RGCH and E-HICH assigned to a UE shall be configured with the same channelisation code.

For E-AGCH, the spreading factor shall always be 256.

5.2.2 Scrambling code

A total of 2^{18}-1 = 262,143 scrambling codes, numbered 0…262,142 can be generated. However not all the scrambling codes are used. The scrambling codes are divided into 512 sets each of a primary scrambling code and 15 secondary scrambling codes.

The primary scrambling codes consist of scrambling codes n=16*i where i=0…511. The i:th set of secondary scrambling codes consists of scrambling codes 16*i+k, where k=1…15.

There is a one-to-one mapping between each primary scrambling code and 15 secondary scrambling codes in a set such that i:th primary scrambling code corresponds to i:th set of secondary scrambling codes.

Hence, according to the above, scrambling codes k = 0, 1, …, 8191 are used. Each of these codes are associated with a left alternative scrambling code and a right alternative scrambling code, that may be used for compressed frames. The left alternative scrambling code corresponding to scrambling code k is scrambling code number k + 8192, while the right alternative scrambling code corresponding to scrambling code k is scrambling code number k + 16384. The alternative scrambling codes can be used for compressed frames. In this case, the left alternative scrambling code is used if n<SF/2 and the right alternative scrambling code is used if nεSF/2, where $c_{ch,SF,n}$ is the channelisation code used for non-compressed frames. The usage of alternative scrambling code for compressed frames is signalled by higher layers for each physical channel respectively.

In case F-DPCH is configured in the downlink, the same scrambling code and OVSF code shall be used in F-DPCH compressed frames and normal frames.

The set of primary scrambling codes is further divided into 64 scrambling code groups, each consisting of 8 primary scrambling codes. The j:th scrambling code group consists of primary scrambling codes 16*8*j+16*k, where j=0..63 and k=0..7.

Each cell is allocated one and only one primary scrambling code. The primary CCPCH, primary CPICH, PICH, MICH, AICH, AP-AICH, CD/CA-ICH, CSICH and S-CCPCH carrying PCH shall always be transmitted using the primary scrambling code. The other downlink physical channels may be transmitted with either the primary scrambling code or a secondary scrambling code from the set associated with the primary scrambling code of the cell.

The mixture of primary scrambling code and no more than one secondary scrambling code for one CCTrCH is allowable. In compressed mode during compressed frames, these can be changed to the associated left or right scrambling codes as described above, i.e. in these frames, the total number of different scrambling codes may exceed two.

In the case of the CCTrCH of type DSCH, all the PDSCH channelisation codes that a single UE may receive shall be under a single scrambling code (either the primary or a secondary scrambling code). In the case of CCTrCH of type of HS-DSCH then all the HS-PDSCH channelisation codes and HS-SCCH that a single UE may receive shall be under a single scrambling code (either the primary or a secondary scrambling code).

In each cell, the E-RGCH, E-HICH and E-AGCH assigned to a UE shall be configured with same scrambling code.

The scrambling code sequences are constructed by combining two real sequences into a complex sequence. Each of the two real sequences are constructed as the position wise modulo 2 sum of 38400 chip segments of two binary *m*sequences generated by means of two generator polynomials of degree 18. The resulting sequences thus constitute segments of a set of Gold sequences. The scrambling codes are repeated for every 10 ms radio frame. Let *x* and *y* be the two sequences respectively. The *x* sequence is constructed using the primitive (over GF(2)) polynomial $1+X^7+X^{18}$. The y sequence is constructed using the polynomial $1+X^5+X^7+ X^{10}+X^{18}$.

The sequence depending on the chosen scrambling code number *n* is denoted z_n, in the sequel. Furthermore, let $x(i)$, $y(i)$ and $z_n(i)$ denote the *i*:th symbol of the sequence *x*, *y,* and z_n, respectively.

The *m*-sequences *x*and *y* are constructed as:

Initial conditions:

- x is constructed with x (0)=1, x(1)= x(2)=...= x (16)= x (17)=0.
- y(0)=y(1)= … =y(16)= y(17)=1.

Recursive definition of subsequent symbols:

- x(i+18) =x(i+7) + x(i) modulo 2, i=0,…,2^{18}-20.
- y(i+18) = y(i+10)+y(i+7)+y(i+5)+y(i) modulo 2, i=0,…, 2^{18}-20.

The n:th Gold code sequence z_n, $n=0,1,2,\ldots,2^{18}-2$, is then defined as:

- $z_n(i) = x((i+n) \text{ modulo } (2^{18} - 1)) + y(i) \text{ modulo } 2, i=0,\ldots, 2^{18}-2$.

These binary sequences are converted to real valued sequences Z_n by the following transformation:

$$Z_n(i) = \begin{cases} +1 & if\ z_n(i) = 0 \\ -1 & if\ z_n(i) = 1 \end{cases} \quad for \quad i = 0,1,\ldots,2^{18}-2.$$

Finally, the n:th complex scrambling code sequence $S_{dl,n}$ is defined as:

– $S_{dl,n}(i) = Z_n(i) + j\, Z_n((i+131072) \text{ modulo } (2^{18}-1))$, i=0,1,…,38399.

Note that the pattern from phase 0 up to the phase of 38399 is repeated.

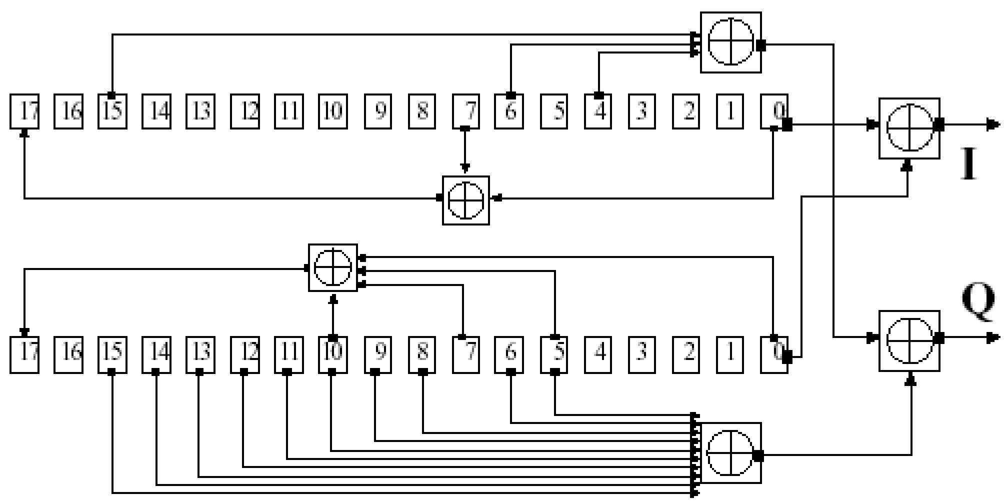

Figure 10: Configuration of downlink scrambling code generator

5.2.3 Synchronisation codes

5.2.3.1 Code generation

The primary synchronization code (PSC), C_{psc} is constructed as a so-called generalised hierarchical Golay sequence.
The PSC is furthermore chosen to have good a periodic auto correlation properties.

Define:

– a = <x_1, x_2, x_3, …, x_{16}> = <1, 1, 1, 1, 1, 1, -1, -1, 1, -1, 1, -1, 1, -1, -1, 1>

The PSC is generated by repeating the sequence *a* modulated by a Golay complementary sequence, and creating a complex-valued sequence with identical real and imaginary components. The PSC C_{psc} is defined as:

– $C_{psc} = (1 + j) \cdot \langle a, a, a, -a, -a, a, -a, -a, a, a, a, -a, a, -a, a, a \rangle$;

where the leftmost chip in the sequence corresponds to the chip transmitted first in time.

The 16 secondary synchronization codes (SSCs), $\{C_{ssc,1},\ldots,C_{ssc,16}\}$, are complex-valued with identical real and imaginary components, and are constructed from position wise multiplication of a Hadamard sequence and a sequence *z*, defined as:

– $z = \langle b, b, b, -b, b, b, -b, -b, b, -b, b, -b, -b, -b, -b, -b \rangle$, where

– $b = \langle x_1, x_2, x_3, x_4, x_5, x_6, x_7, x_8, -x_9, -x_{10}, -x_{11}, -x_{12}, -x_{13}, -x_{14}, -x_{15}, -x_{16} \rangle$ and $x_1, x_2, \ldots, x_{15}, x_{16}$ are same as in the definition of the sequence *a* above.

The Hadamard sequences are obtained as the rows in a matrix H_8 constructed recursively by:

$$H_0 = (1)$$
$$H_k = \begin{pmatrix} H_{k-1} & H_{k-1} \\ H_{k-1} & -H_{k-1} \end{pmatrix}, \quad k \geq 1$$

The rows are numbered from the top starting with row *0* (the all ones sequence).

Denote the *n*:th Hadamard sequence as a row of H_8 numbered from the top, n = 0, 1, 2, …, 255, in the sequel.

Furthermore, let $h_n(i)$ and $z(i)$ denote the *i*:th symbol of the sequence h_n and *z,* respectively where *i* = 0, 1, 2, …, 255 and *i* = 0 corresponds to the leftmost symbol.

The *k*:th SSC, $C_{ssc,k}$, *k* = 1, 2, 3, …, 16 is then defined as:

– $C_{ssc,k} = (1 + j) \cdot \langle h_m(0) \cdot z(0), h_m(1) \cdot z(1), h_m(2) \cdot z(2), \ldots, h_m(255) \cdot z(255) \rangle$;

where $m = 16 \cdot (k - 1)$ and the leftmost chip in the sequence corresponds to the chip transmitted first in time.

5.2.3.2 Code allocation of SSC

The 64 secondary SCH sequences are constructed such that their cyclic-shifts are unique, i.e., a non-zero cyclic shift less than 15 of any of the 64 sequences is not equivalent to some cyclic shift of any other of the 64 sequences. Also, a non-zero cyclic shift less than 15 of any of the sequences is not equivalent to itself with any other cyclic shift less than 15. Table 4 describes the sequences of SSCs used to encode the 64 different scrambling code groups. The entries in table 4 denote what SSC to use in the different slots for the different scrambling code groups, e.g. the entry "7" means that SSC $C_{ssc,7}$ shall be used for the corresponding scrambling code group and slot.

Table 4: Allocation of SSCs for secondary SCH

Scrambling Code Group	slot number														
	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14
Group 0	1	1	2	8	9	10	15	8	10	16	2	7	15	7	16
Group 1	1	1	5	16	7	3	14	16	3	10	5	12	14	12	10
Group 2	1	2	1	15	5	5	12	16	6	11	2	16	11	15	12
Group 3	1	2	3	1	8	6	5	2	5	8	4	4	6	3	7
Group 4	1	2	16	6	6	11	15	5	12	1	15	12	16	11	2
Group 5	1	3	4	7	4	1	5	5	3	6	2	8	7	6	8
Group 6	1	4	11	3	4	10	9	2	11	2	10	12	12	9	3
Group 7	1	5	6	6	14	9	10	2	13	9	2	5	14	1	13
Group 8	1	6	10	10	4	11	7	13	16	11	13	6	4	1	16
Group 9	1	6	13	2	14	2	6	5	5	13	10	9	1	14	10
Group 10	1	7	8	5	7	2	4	3	8	3	2	6	6	4	5
Group 11	1	7	10	9	16	7	9	15	1	8	16	8	15	2	2
Group 12	1	8	12	9	9	4	13	16	5	1	13	5	12	4	8
Group 13	1	8	14	10	14	1	15	15	8	5	11	4	10	5	4
Group 14	1	9	2	15	15	16	10	7	8	1	10	8	2	16	9
Group 15	1	9	15	6	16	2	13	14	10	11	7	4	5	12	3
Group 16	1	10	9	11	15	7	6	4	16	5	2	12	13	3	14
Group 17	1	11	14	4	13	2	9	10	12	16	8	5	3	15	6
Group 18	1	12	12	13	14	7	2	8	14	2	1	13	11	8	11
Group 19	1	12	15	5	4	14	3	16	7	8	6	2	10	11	13
Group 20	1	15	4	3	7	6	10	13	12	5	14	16	8	2	11
Group 21	1	16	3	12	11	9	13	5	8	2	14	7	4	10	15
Group 22	2	2	5	10	16	11	3	10	11	8	5	13	3	13	8
Group 23	2	2	12	3	15	5	8	3	5	14	12	9	8	9	14
Group 24	2	3	6	16	12	16	3	13	13	6	7	9	2	12	7
Group 25	2	3	8	2	9	15	14	3	14	9	5	5	15	8	12
Group 26	2	4	7	9	5	4	9	11	2	14	5	14	11	16	16
Group 27	2	4	13	12	12	7	15	10	5	2	15	5	13	7	4
Group 28	2	5	9	9	3	12	8	14	15	12	14	5	3	2	15
Group 29	2	5	11	7	2	11	9	4	16	7	16	9	14	14	4
Group 30	2	6	2	13	3	3	12	9	7	16	6	9	16	13	12
Group 31	2	6	9	7	7	16	13	3	12	2	13	12	9	16	6
Group 32	2	7	12	15	2	12	4	10	13	15	13	4	5	5	10
Group 33	2	7	14	16	5	9	2	9	16	11	11	5	7	4	14
Group 34	2	8	5	12	5	2	14	14	8	15	3	9	12	15	9
Group 35	2	9	13	4	2	13	8	11	6	4	6	8	15	15	11
Group 36	2	10	3	2	13	16	8	10	8	13	11	11	16	3	5
Group 37	2	11	15	3	11	6	14	10	15	10	6	7	7	14	3
Group 38	2	16	4	5	16	14	7	11	4	11	14	9	9	7	5
Group 39	3	3	4	6	11	12	13	6	12	14	4	5	13	5	14
Group 40	3	3	6	5	16	9	15	5	9	10	6	4	15	4	10
Group 41	3	4	5	14	4	6	12	13	5	13	6	11	11	12	14
Group 42	3	4	9	16	10	4	16	15	3	5	10	5	15	6	6
Group 43	3	4	16	10	5	10	4	9	9	16	15	6	3	5	15
Group 44	3	5	12	11	14	5	11	13	3	6	14	6	13	4	4
Group 45	3	6	4	10	6	5	9	15	4	15	5	16	16	9	10
Group 46	3	7	8	8	16	11	12	4	15	11	4	7	16	3	15
Group 47	3	7	16	11	4	15	3	15	11	12	12	4	7	8	16
Group 48	3	8	7	15	4	8	15	12	3	16	4	16	12	11	11
Group 49	3	8	15	4	16	4	8	7	7	15	12	11	3	16	12

Scrambling Code Group	slot number														
	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14
Group 50	3	10	10	15	16	5	4	6	16	4	3	15	9	6	9
Group 51	3	13	11	5	4	12	4	11	6	6	5	3	14	13	12
Group 52	3	14	7	9	14	10	13	8	7	8	10	4	4	13	9
Group 53	5	5	8	14	16	13	6	14	13	7	8	15	6	15	7
Group 54	5	6	11	7	10	8	5	8	7	12	12	10	6	9	11
Group 55	5	6	13	8	13	5	7	7	6	16	14	15	8	16	15
Group 56	5	7	9	10	7	11	6	12	9	12	11	8	8	6	10
Group 57	5	9	6	8	10	9	8	12	5	11	10	11	12	7	7
Group 58	5	10	10	12	8	11	9	7	8	9	5	12	6	7	6
Group 59	5	10	12	6	5	12	8	9	7	6	7	8	11	11	9
Group 60	5	13	15	15	14	8	6	7	16	8	7	13	14	5	16
Group 61	9	10	13	10	11	15	15	9	16	12	14	13	16	14	11
Group 62	9	11	12	15	12	9	13	13	11	14	10	16	15	14	16
Group 63	9	12	10	15	13	14	9	14	15	11	11	13	12	16	10

5.3 Modulation

5.3.1 Modulating chip rate

The modulating chip rate is 3.84 Mcps.

5.3.2 Modulation

Modulation of the complex-valued chip sequence generated by the spreading process is shown in Figure 11 below.

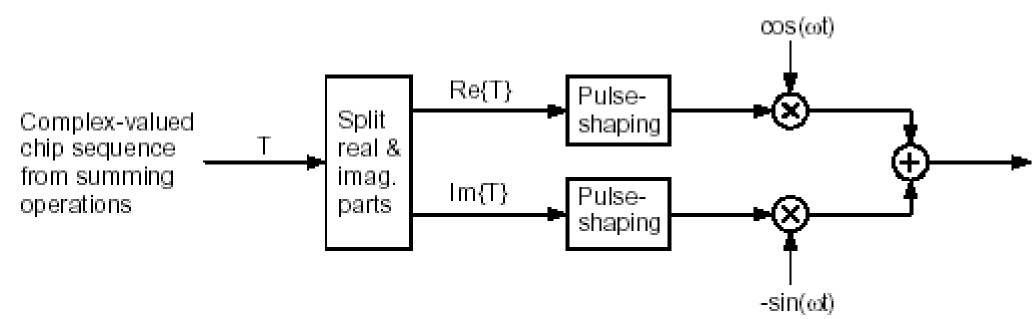

Figure 11: Downlink modulation

The pulse-shaping characteristics are described in [4].