Theory of Operations [1]

The transceiver is described in the block diagram of Figure 1. In receive mode, I and Q baseband signals are digitized at 528 MS/s by 5b ADCs. The packet detection and frame synchronization sequence is detected, and appropriate gain settings are provided to the RF transceiver. Channel estimation, phase tracking, and signal demapping is performed after transformation by a 128-point FFT. Different data rates are implemented through variations in the coding rate, coding type, and modulation. Convolutional codes with rates of 1/3, 1/2, 5/8, and 3/4 are supported, along with Dual-Carrier Modulation (DCM) and QPSK modulation. In addition, tone and symbol interleaving improve performance in fading channels. Soft decisions from the demapper are resolved by the Viterbi decoder and the decoded data is output at the MAC/PHY interface. For transmission, the process is reversed, except that I and Q signals sent to the 5b DACs are up-sampled to 1056 MS/s. A clock generation circuit provides clock signals for the digital PHY and data converters. In frequency-hopping mode, a band-select signal provides indication to the RF transceiver of the appropriate operating frequency

A block diagram of the direct-conversion RF transceiver is shown in Figure 2. In order to enable agile frequency hopping, this design utilizes three separate RF blocks for each operating frequency in Band Group #1 [2]. Each block consists of a tuned amplifier stage, I/Q mixers, and integer-N frequency synthesizer. In frequency-hopping mode, the appropriate RF block is selected for each OFDM symbol, as indicated by the *Band Select* signal. Each mixer shares a common output connection to the RX baseband circuitry. Direct-conversion receivers are sensitive to LO carrier leakage. In addition, 13 on-chip linear voltage regulators are employed to provide circuit isolation and further limit coupling through package bondwires. Each voltage regulator design has a programmable output voltage, requires no external components, and occupies $0.007mm^2$. The receiver baseband circuitry is comprised of 5^{th}-order channel selection filters, PGAs, RSSI circuitry, and DC offset compensation. The fast-frequency hopping in this system places additional constraints on the design of a direct-conversion receiver. AC coupling cannot be employed reliably because DC offsets are in part carrier-frequency dependent, and the fast settling requirement of 9ns in the system prevents resettling of AC coupling circuitry. Furthermore, different frequency bands have different RF path loss parameters, resulting in different receiver gain settings. Therefore, any DC offset correction must remain effective for different gain and carrier frequency settings.

The transmitter section employs many of the same concepts as the receiver for implementing frequency hopping. Figure 3 shows a simplified circuit diagram of the modulator circuit (one channel), and the shared switched-inductor load. Capacitors tuned with MOS switches result in high-Q tuning elements, but at the expense of additional parasitic capacitance at the output node. In this system, the 528-MHz channel bandwidth makes the use of high-Q resonant circuits undesirable. The balanced switch configuration used in this design allows the use of a smaller switch for a given parasitic resistance. Furthermore, the parasitic capacitance of the switch is partially transformed by the inductor when referred to the output node. The use of switched inductors also allows

each inductor to be optimized separately, potentially allowing a wider operating range than a single inductor, switched-capacitor method.

References

[1] T. Aytur, et al., "A Fully Integrated UWB PHY in 0.13 um CMOS," *Proc. ISSCC Conf*., San Francisco, pp. 124-125, Feb. 2006

[2] B. Razavi, et al., "A 0.13-µm CMOS UWB Transceiver," *ISSCC Dig. Tech. Papers*, pp. 216-217, Feb. 2005.

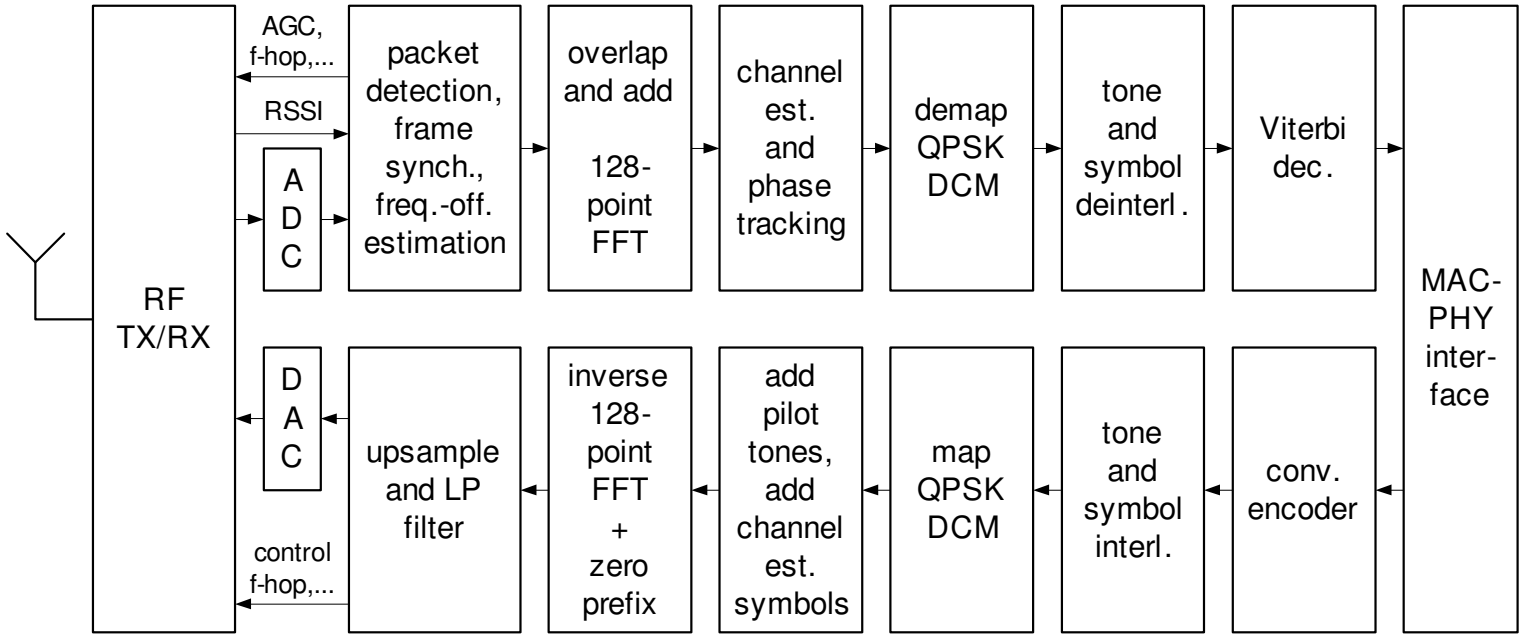

Figure 1: Block diagram of an integrated UWB OFDM PHY

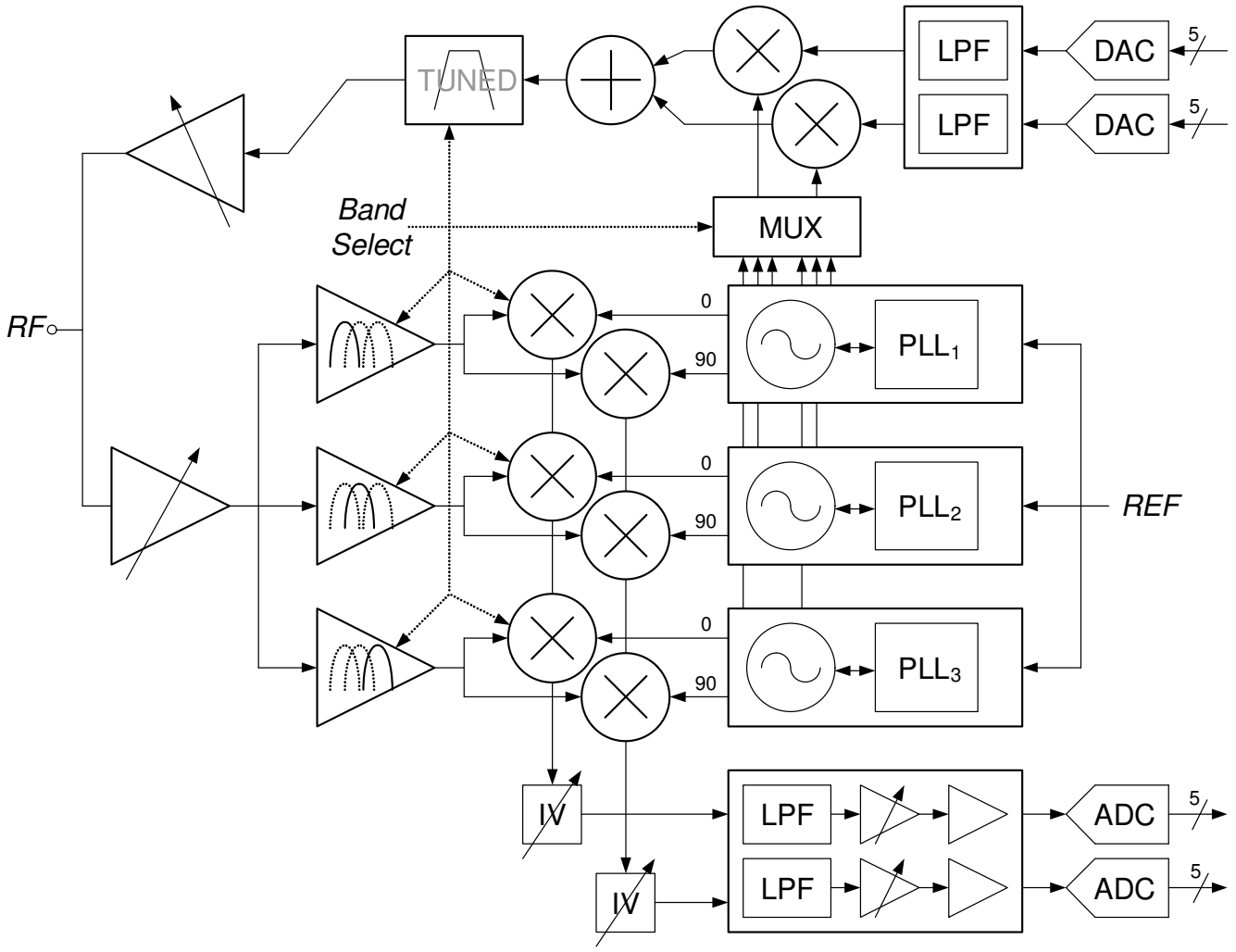

Figure 2: Block diagram of a direct-conversion transceiver

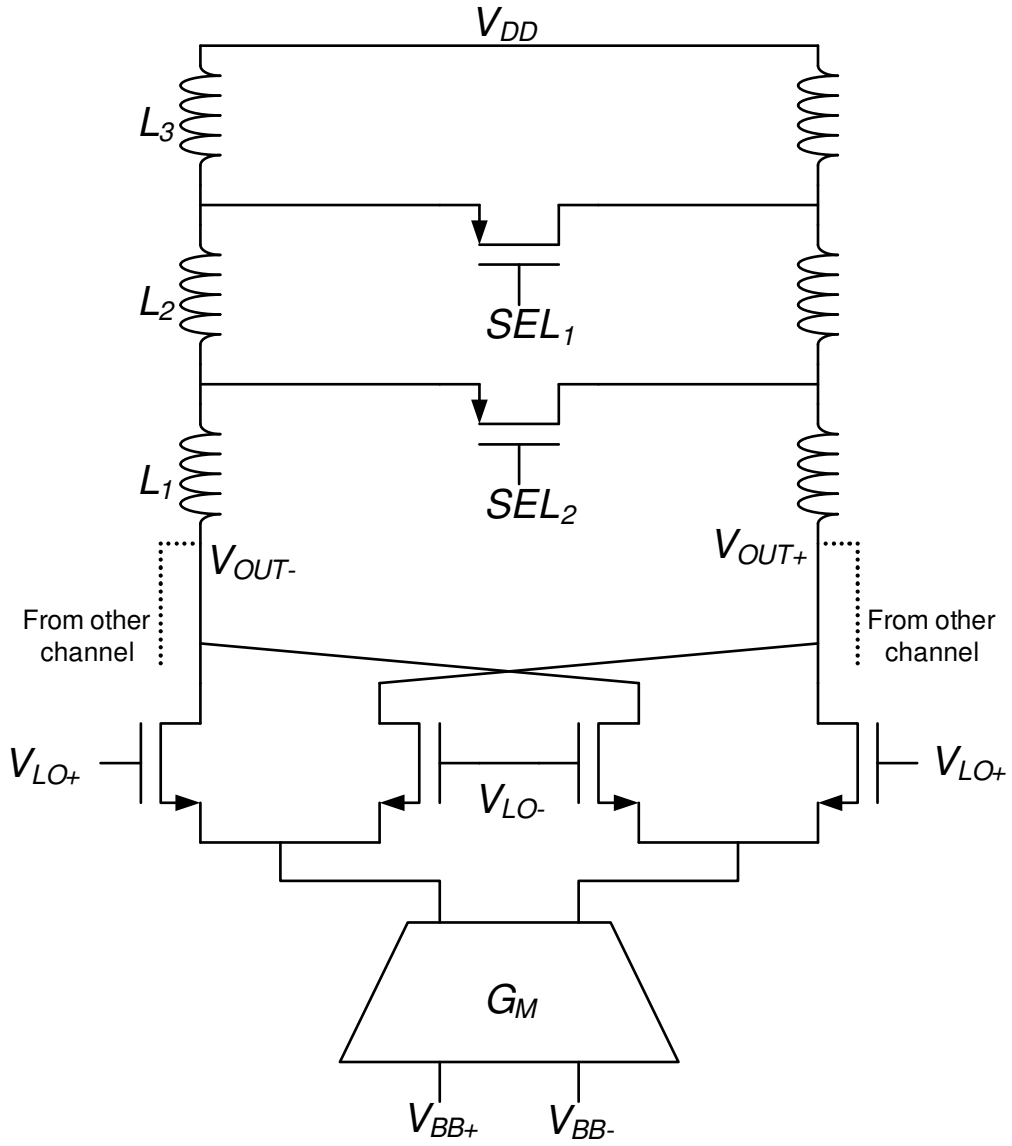

Figure 3: Simplified modulator circuit (one channel) and inductive load