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Harman Becker Automotive Systems GmbH
Becker-Görling-Straße 16
76307 Karlsbad



Declaration of Similarity

To whom it may concern:

We, **Harman Becker Automotive Systems GmbH**, located in BECKER-GOERING-STR. 16, 76307 Karlsbad Germany, declare under our sole responsibility that the that the following products:

- **IDC23H ,**
- **IDC2385H**

are using the identical BT/WLAN module with the same layout and schematic. From radio transmitter perspective and from RF point of view the above products can be considered as identical.

All 2 products are identical within the BT/WLAN interface, therefore, the conducted test results performed over one product can be leveraged among the rest.

The differences between the IDC23H and the IDC2385H are limited to the SIP board, which I've circled below in red. The SIP is soldered to the main board, which hasn't changed. Attached an Excel with all differences between both microprocessors.

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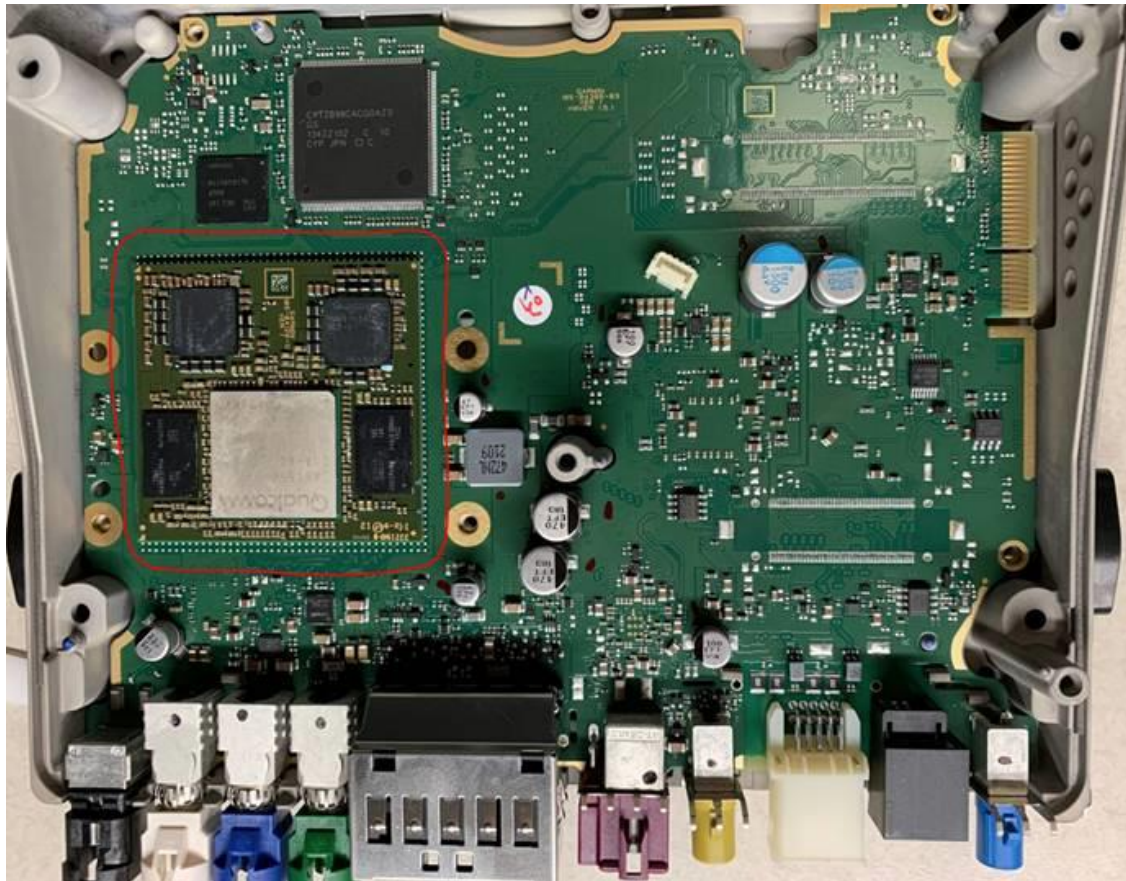
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	RF FEATURES			Microprocessor			I/O controller	
TCU MODEL	GNSS	Bluetooth EDR/BT 5.0 + Wlan 802.11 abgn/ac/ax - MIMO 2x2 [Chipset NXP 88w9098]	Bluetooth EDR/BT 5.0 [Chipset NXP 88W8987]	Qualcomm SA8155P	Qualcomm SA8185P	Qualcomm SA8150	Cypress CYT2B9	Cypress CYT3BB
IDC23H	x	x		x				x
IDC2385H	x	x			x			x

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Vorsitzender des Aufsichtsrats: Marko Ferdinand
Sitz der Gesellschaft: Karlsbad | Amtsgericht Mannheim: HRB-Nr. 361395

Differences between SA8155P and SA8185P (Confidential)			
Area:	SA8155P	SA8185P (IDC)	Comment
Processor Cores:	Applications Kryo 485 – 64-bit applications processor with a 2 MB L3 cache Three Kryo Gold cores with a 256 KB L2 cache per core, targeting up to 2.1312 GHz One Kryo Gold prime core with a 512 KB L2 cache, targeting 2.4192 GHz Quad low-power Kryo Silver cores with a 128 KB L2 cache per core targeting up to 1.7856 GHz	Applications Kryo 495 – 64 bit applications processor with a 4 MB L3 cache Quad high-performance Kryo Gold Prime cores with a 512 KB L2 cache per core, targeting up to 2.496 GHz Quad low-power Kryo Silver cores with a 128 KB L2 cache per core targeting up to 1.766 GHz	IDC's SA8185P has enhanced display computing capability for cabin support as well as infotainment, but clock frequencies are similar.
Display Processing (DPU)	Adreno DPU 895 Two 4-lane MIPI DSI with VESA DSC v1.1 D-PHY v1.2: 2.5 Gbps/lane on four lanes per port, 10 Gbps/port, up to 20 Gbps total C-PHY v1.0: 5.7 Gbps/trio on three trios per port, 17 Gbps/port, up to 34 Gbps total DisplayPort v1.4 at 8.1 Gbps/lane, 32.4 Gbps/port, over USB 3.1 with support for MST and VESA DSC v1.1 and forward error correction (FEC). Concurrent DisplayPort USB3 and USB2 are supported. Display processing Up to a maximum of 24 MP; example configurations:	Adreno DPU 899, 530 MHz Two 4-lane MIPI DSI with VESA DSC v1.1 D-PHY v1.2: 2.5 Gbps/lane on four lanes per port, 10 Gbps/port, up to 20 Gbps total C-PHY v1.0: 5.7 Gbps/trio on three trios per port, 17 Gbps/port, up to 34 Gbps total One Embedded DisplayPort (eDP) 1.4b with VESA DSC v1.1 Three DisplayPort v1.4 at 8.1 Gbps/lane, 32.4 Gbps/port, with two DisplayPort over USB 3.1.MST and VESA DSC v1.1 and forward error correction (FEC). Up to a maximum of 40 MP	Similar MIPI performance

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	3x 4K or 4x 2880 × 1080 or 2x 4K + 1x 2880 × 1080		
Camera Support	Qualcomm Spectra 380 ISP Pixel processing: 2 × IFE + 2 × IFE_L Data formats: Bayer RGB, YUV, zzHDR, iHDR, RCCB, 10/8 bit YUV output Statistics: Exposure, white balance, focus (HDR BHist, Tintless BG, AWB BG, Bhist, Row/Col SUM) 14 bit depth max, multiple pixel raw dump channels per CSID/IFE Processing features: Bayer processing, offset correction, lens roll off correction, bad pixel corrections, directional scalers, color LUTs, color space transform, noise reduction, and local tone mapping. Four 4-lane MIPI CSI configurable in 4 + 4 + 4 + 4 or split 2s configuration D-PHY v1.2: 2.5 Gbps/lane on four lanes per port, 10 Gbps/port, up to 40 Gbps total C-PHY v1.0: 5.7 Gbps/trio on three trios per port, 17 Gbps/port, up to 68 Gbps total	Qualcomm Spectra 390 ISP Pixel Processing: 4 × IFE + 4 × IFE_L Data Formats: Bayer RGB, YUV, zzHDR, iHDR, RCCB, 10/8bit YUV output Statistics: Exposure, white balance, focus (HDR BHist, Tintless BG,AWB BG, Bhist, Row/Col SUM) 14 bit depth max, multiple pixel raw dump channels per CSID/IFE. Processing features: Bayer processing, offset correction, lens roll off correction, bad pixel corrections, directional scalers, color LUTs, color space transform, noise reduction, local tone mapping, dewarp. Four 4-lane MIPI CSI configurable in 4 + 4 + 4 + 4 or split 2s configuration D-PHY v1.2: 2.5 Gbps/lane on four lanes per port, 10 Gbps/port, up to 40 Gbps total C-PHY v1.0: 5.7 Gbps/trio on three trios per port, 17 Gbps/port, up to 68 Gbps total	Similar camera support.

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Number of I/O Ports	175 – GPIO_0 to GPIO_174	190 – GPIO_0 to GPIO_189	SA8185 has extra GPIO pins, but they aren't utilized as every I/O is mapped for similar functions in eac SiP socket design. So, they have the same I/O.
External NV Memory Support	UFS 2.1 gear 3 – 2 lanes for on-board memory (UFS 3.0 gear 4 supported) NOR flash	2x UFS 3.0 gear 4 – 2 lanes for on-board memory NOR Flash	Only one UFS is used for each design, as this is related to the SiP socket I/O mapping between designs. Will be operating UFS at Gear 4 rate

And as evidence thereof, I hereby issue this letter in Bucharest on 12/02/2024.

Authorized Signature by:

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