FCC ID: T7P35210

Technical Description :

The brief circuit description is listed as follows :
- U1 SNC12120 acts as MCU with Voice Synthesizer.
- U2 HL5232, XTAL, R2, C12, C13 and associated circuit act as 13.56 MHz Oscillator and RFID reader.
- L1, L2, C1, C2 and C3 act as Loop Antenna and Matching Circuit.
- S2 acts as Control Key.

Antenna Used :

A Loop antenna has been used.

Features

- Low standby current.
- Low power consumption.
- Simple application circuit.
- Stable performance.
- The system and oscillator can be enable separately.
- 3 kinds of Decoder outputs.
- Level hold mode and one shot Trigger mode.
- High Active and low Active output selectable.

Applications

- Toy RFID.
- Asset control.
- Contactless entry control.
- Education.

General Description

HL5232 is a CMOS IC used to perform the function of a RFID Reader. A RFID contains two parts: RFID TAG (HL5230) and RFID Reader (HL5232). HL5232 contains of a 13.56MHz crystal oscillator, a 13.56MHz output buffer, a preamplifier and data decoder. The output buffer drives an antenna which can transmits RF signal to the RFID TAG.

If TAG is close enough to the Reader, the encoder of TAG will send out a data train. The data train is used to modulate the RF signal in the TAG, and the amplitude of RF signal in the Reader will be modulated also. Preamplifier is used to amplify the modulating signal. The decoder is used to decoder the encoded data transmitted from TAG.

There are three kinds of output data: Synchronous, Asynchronous and direct drive outputs. In order to interface to most of power Speech IC, the data rate of the outputs is slower than the data rate of the RFID TAG.

Block Diagram
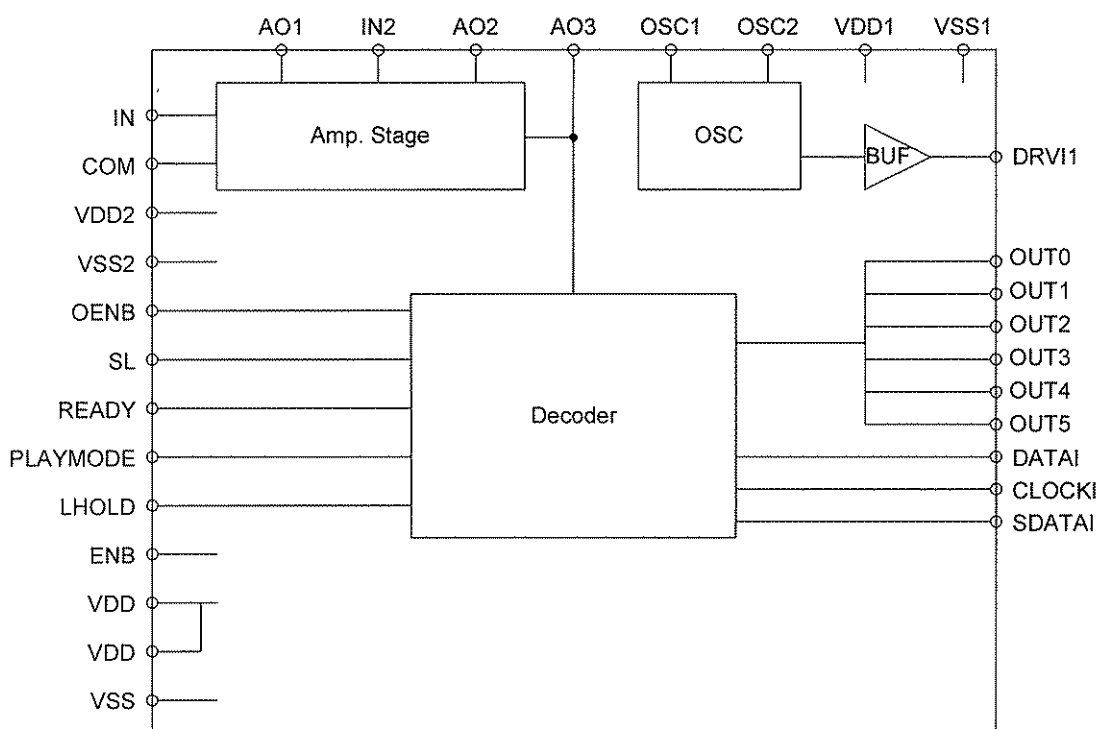
15	DRIV1	Buffer output of 13.56MHz oscillator.
16	VSS1	Negative power supply terminal.
17	VDD	Positive power supply terminal.
18	VDD2	Positive power supply terminal of preamplifier.
19	OENB	Enable input pin. When OENB = 0 system will disable except oscillator.
20	ENB	Enable input pin of the whole system.
21	OSC2	Oscillator output pin.
22	OSC1	Oscillator input pin.
23	AO3	Output pin of 3rd stage of preamplifier.
24	AO2	Output pin of 2nd stage of preamplifier.
25	IN2	Inverting input pin of 2nd stage of preamplifier.
26	AO1	Output pin of 1st stage of preamplifier.
27	IN1	Inverting input pin of 1st stage of preamplifier.
28	COM	Common input pin of preamplifier.
29	VSS2	Negative power supply terminal of preamplifier.
30	VSS	Negative power supply terminal.

Absolute Maximum Ratings

Power Supply 5V
Input Voltage .... VSS-0.3V to VDD+0.3V
Operating Temperature .... 0°C to 60°C
Storage Temperature .... -65°C to 125°C

Electrical Characteristics

SYSTEM	DESCRIPTION	TEST CONDITION	LIMIT			UNIT
			MIN.	TYP.	MAX.	
VDD	Supply Voltage		3	4.5	5	V
VIL	Input Voltage Low	VDD=4.5V			0.3VDD	V
VIH	Input Voltage High	VDD=4.5V	0.7VDD			V
VOSC	Oscillator Starting Voltage			2.2		V
IOP	Operating Current	VDD=4.5V		12*		mA
IST	Stand-by Current	VDD=4.5V		0.5		uA
IOSC	Oscillator Operating Current	VDD=4.5V		0.4		mA

* IOP depends on external coil.

Functional Description

There are three major function provided by HL5232: support a 13.56MHz driver, to transform DATA Bit rate for easy interface with MCU or power Speech IC and to provide direct decoder output.

After received the modulating signal from the RFID TAG, the modulating signal is amplified and filtered by preamplifier.   There is decoder and error detector built in the HL5232.   The decoded output can be sent to output pin directly, or encoded again at a slower bit rate.   Slower bit rate is necessary for most of power Speech IC.   When PLAYMODE = 1, there are 8 direct output provided.   Besides the 3 bits which is used as decoder inputs, there is 1 bit, which is used as parity check bit.   The output will be activated only when parity is correct.   In HL5232 even parity is used, Bit0~Bit2 is used as decoder input and Bit7 is parity Bit.

1. INTRODUCTION

SNC12120 is a one-channel voice synthesizer IC with Push-Pull direct drive circuit. It built in a 4-bit tiny controller with four 4-bit I/O ports. By programming through the tiny controller in SNC12120, user's varied applications including voice section combination, key trigger arrangement, output control, and other logic functions can be easily implemented.

2. FEATURES

- Single power supply 2.4V – 5.5V
- 120 seconds voice capacity are provided (@6KHZ sample rate)
- Built in a 4-bit tiny controller
- I/O Port
    - Four 4-bit I/O ports P1, P2, P3 and P6 are provided.
    - The driving/sink current of P3.2 & P3.3 is up to 8mA/16mA
    - The IO pins P3.3 can be modulated with 38.5Khz carry signal to implement IR function.
- 128*4 bits RAM are provided
- Maximum 16k program ROM is provided
- 384K*10 shared ROM for voice data and program
- Readable ROM code data
- Built in one channel speech synthesizer
- Adaptive playing speed from 2.5k-20kHz is provided
- Built in an 8-level volume control Push-Pull Direct Drive circuit output, can directly connected to Speaker for sound output.
- System clock: 2MHz
- Event Mark function supported
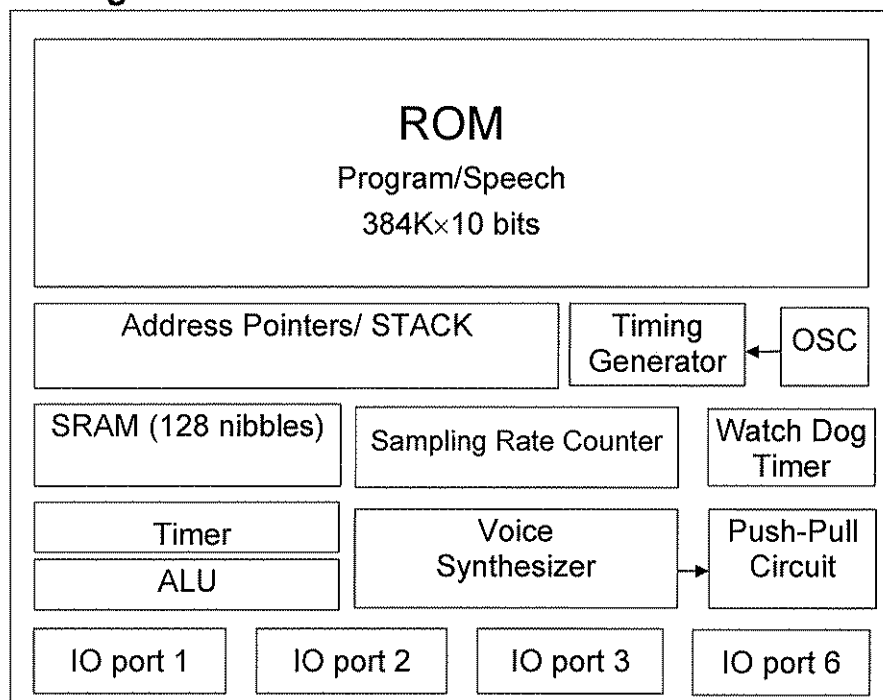- Low Power Reset
- Watch Dog Timer Supported

3. PIN ASSIGNMENT

Symbol	I/O	Function Description
P10~P13	I/O	I/O port 1: IO
P20~P23	I/O	I/O port 2: IO
P30~P33	I/O	I/O port 3: IO
P60~P63	I/O	I/O port 6: IO
Rosc	I	Oscillation component connection pin
BUO1	O	Push-Pull output 1
BUO2	O	Push-Pull output 2
RST	I	RST=1→ Reset Chip (Active H)
VDD	I	Positive power supply
GND	I	Negative power supply

Test	I	Test pin

4. Block Diagram


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┌─────────────────────────────────────────────────────┐
│  ┌───────────────────────────────────────────────┐  │
│  │                                               │  │
│  │                    ROM                        │  │
│  │              Program/Speech                   │  │
│  │               384K×10 bits                    │  │
│  │                                               │  │
│  └───────────────────────────────────────────────┘  │
│  ┌──────────────────────────┐ ┌──────────┐ ┌──────┐ │
│  │ Address Pointers/ STACK   │ │ Timing   │ │ OSC  │ │
│  │                           │ │ Generator│ │      │ │
│  └──────────────────────────┘ └──────────┘ └──────┘ │
│  ┌──────────────────┐ ┌───────────────────┐ ┌──────┐│
│  │ SRAM (128 nibbles)│ │Sampling Rate Counter│ │Watch Dog│
│  │                   │ │                    │ │ Timer ││
│  └──────────────────┘ └───────────────────┘ └──────┘│
│  ┌──────────────────┐ ┌───────────────────┐ ┌──────┐│
│  │      Timer        │ │      Voice         │ │Push-Pull│
│  ├──────────────────┤ │   Synthesizer      │ │Circuit││
│  │      ALU          │ │                    │ │      ││
│  └──────────────────┘ └───────────────────┘ └──────┘│
│  ┌────────┐ ┌────────┐ ┌────────┐ ┌────────┐         │
│  │IO port 1│ │IO port 2│ │IO port 3│ │IO port 6│      │
│  └────────┘ └────────┘ └────────┘ └────────┘         │
└─────────────────────────────────────────────────────┘
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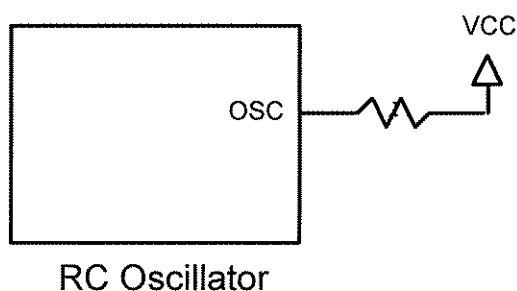
5. FUNCTION DESCRIPTIONS

5.1 Oscillator

SNC12120 accepts RC type oscillator for system clock. The typical circuit diagram for oscillator is listed as follows.

RC Oscillator

5.2 ROM

SNC12120 contains a substantial 384K words (10-bit) internal ROM, which is shared by program and resource data. Program, voice and data are shared within this same 384K words ROM.

5.3 RAM

SNC12120 contains 128 nibble RAM (128 x 4-bits). The 128 nibble RAM is divided into eight pages (page 0 to page 7, 16 nibble RAM on each page). In our programming structure, users can use the instructions, PAGE n (n=0 to 7) to switch and indicate the RAM page. Besides, users can use direct mode, M0 ~ M15 in the data transfer type instructions, to access all 16 nibbles of each page

5.4 Power Down Mode

"End" instruction makes the IC entering into Stop Mode will stop the system clock for power savings (<3uA @VDD=3V and <6uA @VDD=4.5V.) Any valid data transition (L→H or H→L) occurring on any IO pin can be used to start the system clock and return to normal operating mode.

5.5 Sampling Rate Counter

The unique sampling rate counter is designed in voice channel to be able to play diverse voices at different sample playing rates. The playing rate can be adaptively set up among from the wide ranges of 2.5KHz to 20KHz. This architecture yields a high-quality voice synthesis that sounds very close to its original source when played through the same amplifier and speaker circuitry.

5.6 I/O Ports

There are four 4-bit I/O ports P1, P2, P3, and P6. Any I/O can be individually programmed as either input pull low or output. Any valid data transition (H→ L or L→H) of P1, P2, P3, and P6 can reactivate the chip when it is in power-down stage.
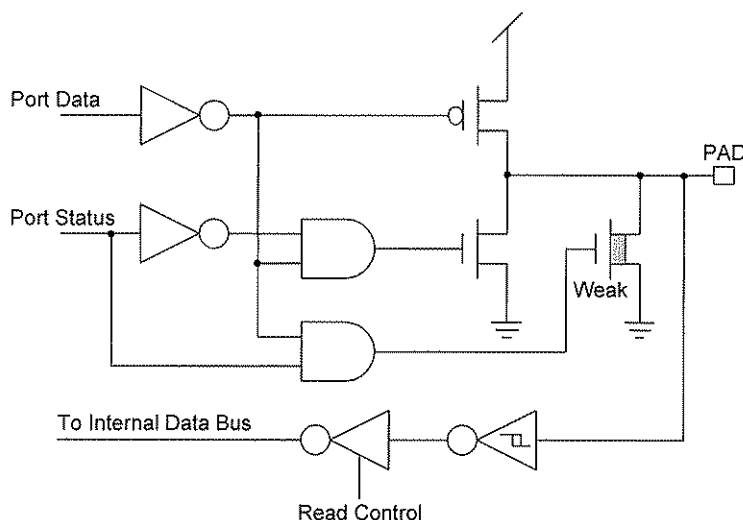

I/O Port Configuration

Note:
(1) *Weak N-MOS can serve as pull-low resistor.*
(2) *The driving/sink current of P3.3 & P3.2 is up to 8mA/16mA*

5.7 Push-Pull Output

An 8-level volume control Push-Pull Direct Drive circuit is built-in SNC12120. The maximum resolution of Push-Pull is 7 bits. Two huge output stage circuits are designed in SNC12120. With this advanced circuit, the chip is capable of driving speaker directly without external transistors.

BUO1

BUO2
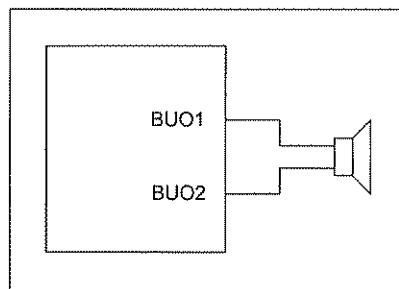
Push-Pull Output

5.8 Watch Dog Timer

SNC12120 built an internal WDT (Watch Dog Timer). This Watchdog timer would issue resets signal to this chip if it is not cleared before reaching terminal count (1sec). The watchdog timer is enabled at reset and cannot be disabled.

5.9 IR Function

P33 can be modulated with 38.5KHz square wave before sent out to P33 pin. The IR signal can be achieved by this modulated signal.

6. ABSOLUTE MAXIMUM RATING

Items	Symbol	Min	Max	Unit.
Supply Voltage	V_{DD}-V	-0.3	6.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	0	55.0	°C
Storage Temperature	T_{STG}	-55.0	125.0	°C