FCC ID: T5706007

Technical Description :

The brief circuit description is listed as follows :

The main unit (reader):
- L2, L4 and L6 act as Loop Antennas.
- TC1 ~ TC3, C67 ~ C69 and associated circuit act as Antenna Matching Circuit.
- U4 and associated circuit act as 13.56 MHz RFID Reader.
- Q11 ~ Q13, Q15 ~ Q17 and associated circuit act as RF Control Circuit.
- U6 acts as Sound Controller & MCU.
- U5 acts as RAM.
- U6 acts as ROM.
- U3 acts as Audio Amplifier.
- Q2 ~ Q10 and associated circuit act as LED Driver.
- J1 acts as Audio Line in Jack.
- SW1, SW2, Mode, Down and Up act as Key Panel.
- U1 acts as Voltage Regulator.
- L701 ~ L704 and C701 act as Noise Filter.

For Tags:
- L19 ~ L20 act as Loop Antennas.
- U12 ~18 act as RFID Transponder.

Antenna Used :

Loop antennas has been used.

Winbond Electronics Corp.

1. GENERAL DESCRIPTION

Winbond *MFID*^{WB} (Magnetic Field Identification) series is used in all areas of automatic data capture allowing contactless identification of objects using magnetic field. From ticketing to industrial automation and access control, the applications of MFID are burgeoning. In recent years automatic identification procedures have become very popular in many service industries, purchasing and distribution logistics, industry, manufacturing companies and material flow systems.

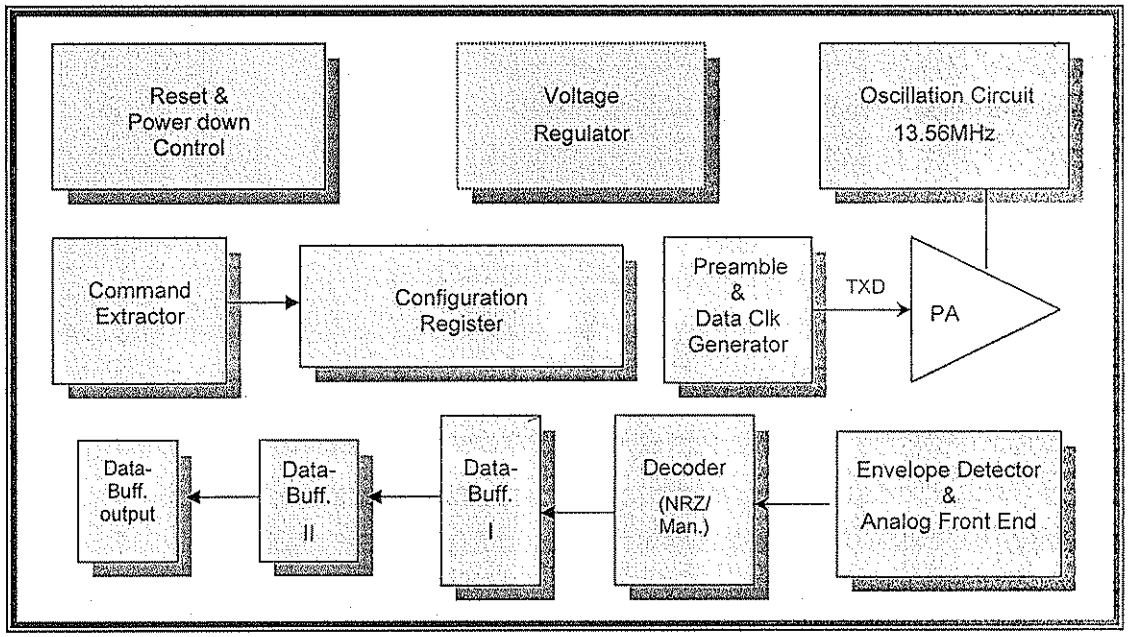
W55MID50 is one of series in Winbond *MFID*^{WB} family that supports multi-functional Reader solution and especially focus on toy, security, and consumer related applications. The applications with Winbond *MFID*^{WB} Tag series such as W55MID10 that provides read-only mask ROM-ID version transponder for mass production solution in toy industrial, meanwhile W55MID15 provides the other solution for manufacture option, which is 243 bonding-ID selection transponder. Besides the single tag transponder application, W55MID35 offers multi-transponder recognition function for intelligent and smart toy applications.

W55MID50 provides a wide variety of applications for toy, security, and consumer market meanwhile the W55MID50 is the most cost effective solution on current *MFID*^{WB} related application market

2. FEATURES

- Magnetic field resonance frequency: 13.56 MHz
- Data clock: 22 ~ 66KHz
- Inductive coupled power supplies for transponder's no battery operation
- On-chip rectifier, voltage limiter, clock extraction, power management, µC interface
- Provides NRZ and Manchester coding data format
- Adjustable 4-level of Reader transmission power selection
- Provides serial and parallel mode µC interface
- µC data output rate ≥ 1Mbps
- Low power, low voltage operation
- Supports power-down mode ≤ 1µA
- Operating distance: 0 ~ 10cm
- Operating voltage: 2.4V ~ 5.5V
- Operating temperature: 0 ~ 70 °C
- Package: Dice form, PDIP-20, SOP-20
- Reference design PC board Size: 2.0 x 2.0cm2 (without PCB antenna)
- Winbond patented "Automatic Reader Transmission Power Adjustment" for Reader optimum transmission power adjust
- Minimize external components

4. BLOCK DIAGRAM



5. FUNCTIONAL DESCRIPTION

5.1 Transmission Power Amplifier (PA)

It provides 4 different selectable transmission power for Reader chip to support *MFID*^{WB} Tag's radiation power supply. The external inductor coupling circuit is designed for 13.56MHz magnetic field resonance. The coupled center frequency will depend on equivalent value of external PCB inductor and capacitor.

5.2 Envelope Detector & Analog Front End

The major function of this unit provides *MFID*^{WB} Tag's data can be extracted.

5.3 Voltage Regulator

The voltage regulator generates the system needs of device power supply.

5.4 Configuration Register

System configuration register controls the all functional settings of W55MID50 such as Tag data format, Tag detection cycle, output data format, and PA transmission power selection.

5.5 Reset and Power-down Control

The function of system power-down control mode is normally used for power consumption saving.

5.6 Crystal Oscillation

The 13.56MHz system clock generator generates the need of device system clock.

5.7 Decoder NRZ/Manchester

This unit is in charge of Tag data format decoder, which can provide Tag-ID data format decoding of NRZ or Manchester.

5.8 Data Buffer and Output

This unit buffers the Tag-ID data, which is under de-frame processing.

Introduction

MFID^{WB} (Magnetic Field Identification) is used in all areas of automatic data capture allowing contactless identification of objects using magnetic field. From ticketing to industrial automation and access control, the applications of MFID are burgeoning. In recent years automatic identification procedures have become very popular in many service industries, purchasing and distribution logistics, industry, manufacturing companies and material flow systems.

W55MID15 is one of Winbond *MFID*^{WB} (Magnetic Field Identification) series in *WinRF*^{WB} family that focus on toy and consumer related applications meanwhile W55MID15 provides manufacture bonding-ID transponder. Regarding the *MFID*^{WB} Reader series, the W55MID50 supports multi-functional *MFID*^{WB} Reader solution. Besides the single transponder application, W55MID35 offers multi-transponder recognition function for intelligent and smart toy applications.

W55MID15 provides total 243 different bonding-IDs in manufacture and 10bit ID length in each ID. That can extremely save customer's design investment in consumer MFID related products.

1.1 W55MIDxx Series Selection Guide

W55MID Series Selection Guide

	W55MID15	W55MID35	W55MID50	W55MID20	W55MID55
Category	Single-tag	Multi-tag	Reader	R/W-tag	R/W-Reader
Frequency	13.56MHz			13.56MHz	
ID type	Bonding-ID		X	Programmable-ID	X
# of available IDs	243 IDs		X	Infinite	X
ID length	10-bit		X	64-bit	X
Anti-collision	X	5 ~ 8 Tags	X	5 ~ 8 Tags	X
TX power	X		4-level option	X	4-level option
uC interface	X		Serial/Parallel	X	Serial/Parallel
Package	Dice form		Dice/SOP-20	Dice form	Dice/SOP-20
E/S	Now			Apr. 2003	
Production	Jan./E, 2003			May, 2003	

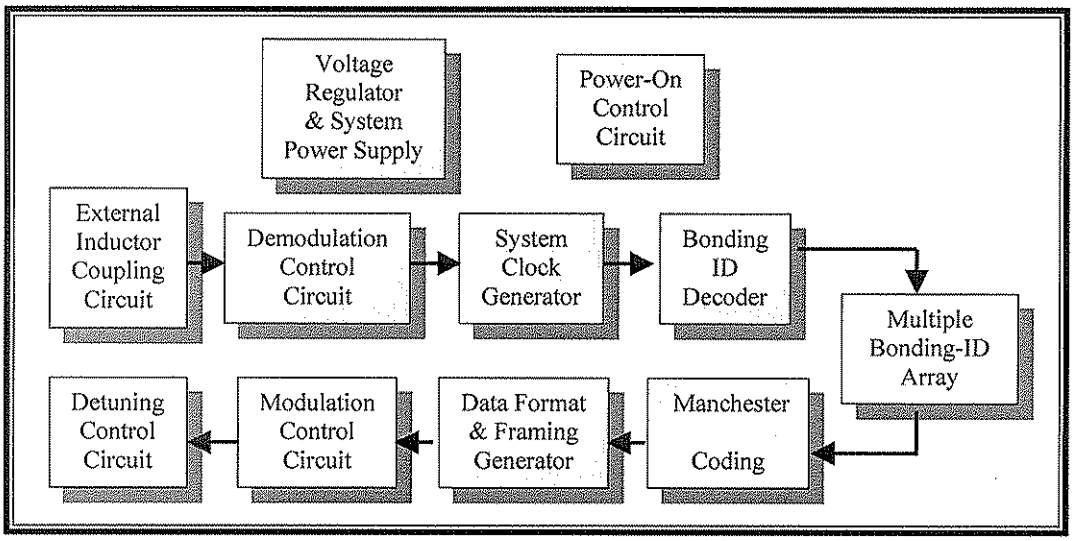
Features

2.1 W55MID15 Features List

- Magnetic field resonance frequency: 13.56MHz
- Data clock: 32KHz
- Read-only bonding-ID transponder
- Inductive coupled power supply for no battery operation
- On-chip rectifier, voltage limiter, clock extraction
- 10bit bonding-ID length
- Provides Manchester coding data format
- RS0, RS1, RS2, RS3, and RS4 the 3-state bonding finger for the total 243 bonding-ID option in manufacture
- Low power, low voltage operation
- Operating distance: 0 ~ 5cm
- Operating temperature: 0 ~ 70 °C
- Package: Dice form
- Reference design PC board Size: 1.0x1.0cm^2 (with PCB antenna)
- Winbond patented "3-state Bonding Finger" for multiple bonding-ID option
- Minimize external component: capacitor and PCB antenna only

Architecture Overview

3.1 W55MID15 System Block Diagram



3.2 W55MID15 System Functional Description

External Inductor Coupling Circuit

The external inductor coupling circuit is designed for 13.56MHz magnetic field resonance. The coupled center frequency will depend on equivalent inductor of external PCB inductor and a paralleled capacitor.

Voltage Regulator & System Power Supply

The voltage regulator generates the need of device power supply.

Power-On Control Circuit

System power-on control circuit initiates the device to get into initial state.

Demodulation Control Circuit

The demodulation control circuit demodulates the signal of command, which is magnetic field coupling from W55MID50 *MFID*^{WB} Reader system.

System Clock Generator

The system clock generator generates the need of device system clock.

Bonding-ID Decoder

The memory array decoder circuit decodes the mapping location of memory array, which indicates by external RS0, RS1, RS2, RS3, and RS4 the 3-state Bonding Finger (Winbond patented).

Multiple Bonding-ID Arrays

The multiple Bonding-IDs array provides total up to 243 different bonding-ID and 10bit in each ID.

Data Format and Framing Generator

The data format and framing generator is in charge of the entire bonding-ID and command data into a Winbond defined *MFID*^{WB} tag format.

Modulation Control Circuit

The modulation control circuit modulates the Winbond defined *MFID*^{WB} transponder format into the magnetic field resonation.

3.3 W55MID15 Pad Functional Description

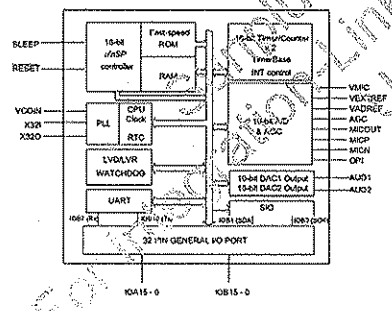
Symbol	Pad No.	I/O	Pad Functional Description
NC	1	--	Testing only, no connection
RS4	2	I	3-state bonding finger
RS3	3	I	3-state bonding finger
RS2	4	I	3-state bonding finger
RS1	5	I	3-state bonding finger
RS0	6	I	3-state bonding finger
VSS	7	Ground	Ground return path
COIL0	8	I/O	Coupling energy input and customer-ID output
COIL1	9	I/O	Coupling energy input and customer-ID output
NC	10	--	Testing only, no connection
VDD	11	Power	Power path

16-BIT SOUND CONTROLLER WITH 24K X 16 ROM

1. GENERAL DESCRIPTION

The SPCE040A, a 16-bit architecture product, carries the newest 16-bit microprocessor, *μ'nSP™* (pronounced as *micro-n-SP*), developed by SUNPLUS Technology. This high processing speed assures the *μ'nSP™* is capable of handling complex digital signal processes easily and rapidly. Therefore, the SPCE040A is applicable to the areas of digital sound process and voice recognition. The operating voltage of 2.4V through 3.6V and speed of 0.32MHz through 49.152MHz yield the SPCE040A to be easily used in varieties of applications. The memory capacity includes 24K-word fast-speed ROM plus a 2K-word working SRAM. Other features include 32 programmable multi-functional I/Os, two 16-bit timers/counters, 32768Hz Real Time Clock, Low Voltage Reset/Detection, eight channels 10-bit ADC (one channel built-in MIC amplifier with auto gain controller), 10-bit DAC output and many others.

2. BLOCK DIAGRAM



3. FEATURES

- 16-bit *μ'nSP™* microprocessor
- CPU clock: 0.32MHz - 49.152MHz
- Operating voltage: 3.0V - 3.6V @CPU clock = 49.152Mhz
  Operating voltage: 2.4V - 3.6V @CPU clock <=40.96Mhz
- IO PortA & B operating voltage: 2.4V - 5.5V
- 24K-word fast-speed ROM
- 2K-word working SRAM
- Software-based audio processing
- Crystal Resonator
- Standby mode (Clock Stop mode) for power savings, Max. 2.0μA @ VDD = 3.6V
- Two 16-bit timers/counters
- Two 10-bit DAC outputs
- 32 general I/Os (bit programmable)
- 14 INT sources with two priority levels
- Key wakeup function (IOA0 - 7)
- Approx. 158 sec speech @ 2.4Kbit/per sec with SACM_S240
- PLL feature for system clock
- 32768Hz Real Time Clock (RTC)
- Eight channels 10-bit AD converter
- ADC external top reference voltage
- 2.0V voltage regulator output, 5mA of driving capability
- Serial interface I/O (SIO)
- Built-in microphone amplifier and AGC function
- UART receiver and transmitter (full duplex)
- Low voltage reset and low voltage detection
- Watchdog enable (bonding option)

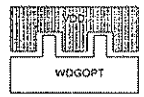
4. APPLICATION FIELD

- Voice recognition products
- Intelligent interactive talking toys
- Advanced educational toys
- Kids learning products
- Kids storybook
- General speech synthesizer
- Long duration audio products
- Recording / playback products

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
IOA [15:8] IOA [7:0]	46 - 39 34 - 27	I/O I/O	IOA [15:8]: bi-directional I/O ports IOA [7:0] can be software programmed to wakeup I/O pins IOA [6:0] can be optioned as ADC Line-in input
IOB [15:11]	50 - 54	I/O	IOB [15:11]: bi-directional I/O ports
IOB 10	57	I/O	IOB10 can also be selected as UART Transmitter (Tx).
IOB 9	58	I/O	IOB9 can also be Multi-duty cycle output of TimerB (BPWMO).
IOB 8	59	I/O	IOB8 can also be Multi-duty cycle output of TimerA (APWMO).
IOB 7	60	I/O	IOB7 can also be selected as UART receiver (Rx).
IOB 6	61	I/O	IOB6 is a bi-directional I/O ports.
IOB 5	62	I/O	IOB5 can also be selected as feedback signal with EXT2.
IOB 4	63	I/O	IOB4 can also be selected as feedback signal with EXT1.
IOB 3	64	I/O	IOB3 can also be selected as an external interrupt input pin (EXT2)(Negative-edge Triggered).
IOB 2	65	I/O	IOB2 can also be selected as an external interrupt input pin (EXT1)(Negative-edge Triggered).
IOB 1	66	I/O	IOB1 can also be selected as a serial interface data. (SDA)
IOB 0	67	I/O	IOB0 can also be selected as a serial interface clock (SCK)
DAC1	12	O	Audio DAC1 output
DAC2	13	O	Audio DAC2 output
X32I	2	I	Oscillator Crystal input
X32O	1	O	Oscillator Crystal output
VCOIN	70	I	RC filter connection for PLL
AGC	16	I	AGC control pin
MICN	19	I	Microphone differential input (negative)
MICP	21	I	Microphone differential input (positive)
V2VREF	14	O	2.0V output voltage, 5.0mA of driving capability (can be used as external ADC Line_IN top reference voltage)
MICOUT	18	O	Microphone 1st amplifier output
OPI	17	I	Microphone 2nd amplifier input
VEXTREF	23	I	ADC Line_IN top external reference voltage input pin
VMIC	25	O	Microphone power supply
VADREF	22	O	AD reference voltage (generated by internal AD converter).
VDD	5, 69	I	Positive supply for logic
VSS	8, 10, 26, 71	I	Ground reference for logic and I/O pins
VDDIO	37, 38, 56	I	Positive supply for I/O pins
VSSIO	35, 36, 48	I	Ground reference for I/O pins
AVDD	24	I	Positive supply for analog circuit including ADC, DAC and 2.0V regulator
AVSS	15	I	Ground reference for analog circuit including ADC, DAC and 2.0V regulator
RESET	68	I	An active low reset to the chip
SLEEP	49	O	Sleep mode (active high)
TEST	3	I	Connected to high for test mode, normally connected to GND (test mode disabled) or unconnected.
N/C	7, 9, 11, 20, 47, 55	I	Not used.
N/C	4	I	Do NOT bonding and connect this pin, if user binding this pin, IC will not work
WDGOPT*	6	I	Connected to high for watchdog disabled, unconnected for watchdog enabled.

Note*: WDGOPT is the watchdog option pin, selected by bonding option. Remain WDGOPT float (unconnected to VDD) to enable the watchdog. In contrast, connecting WDGOPT to VDD will disable watchdog. The reason of placing WDTOPT adjacent to VDD is to facilitate connection between VDD and WDGOPT when disabling watchdog is necessary. The layout of WDOGPT option pin is drawn in the right.



6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

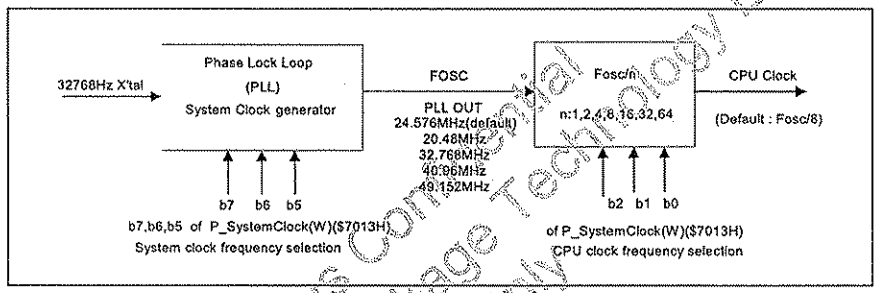
The SPCE040A is equipped with a 16-bit *μ'nSP™*, the newest 16-bit microprocessor by SUNPLUS and pronounced as *micro-n-SP*. Eight registers are involved in *μ'nSP™*: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) and SR (Segment Register). The interrupts include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK.

Moreover, a high performance hardware multiplier with the capability of FIR filter is also built in to reduce the software multiplication loading.

6.2. Memory

6.2.1. SRAM

The amount of SRAM is 2K-word (including Stack) ranged from $0000 through $07FF with access speed of two CPU clock cycles.



6.2.2. ROM

The SPCE040A provides a 24K-word fast-speed ROM with access speed of two CPU clock cycles.

6.3. PLL, Clock, Power Mode

6.3.1. PLL (Phase Lock Loop)

The purpose of PLL is to provide a base frequency (32768Hz) and to pump the frequency from 20.48MHz to 49.152MHz for system clock (Fosc). The default PLL frequency is 24.576MHz.

6.3.1.1. System clock

Basically, the system clock is provided by PLL and programmed by the Port_SystemClock (W) to determine the frequency of clock for system. The default system clock Fosc = 24.576MHz and CPU clock is Fosc/8 if not specified. The initial CPU clock is Fosc/8 after system wakes up and to be adjusted to desired CPU clock by programming the Port_SystemClock (W).

6.3.1.2. 32768Hz RTC

The Real Time Clock (RTC) is normally used in watch, clock or other time related products. A 2Hz-RTC (1/2 second) function is loaded in SPCE040A. The RTC counts the timing as well as to wake CPU up whenever RTC occurs. Since the RTC is generated in every 0.5 seconds, time can be traced by the numbers of RTC occurrence. In addition, SPCE040A supports 32768Hz oscillator in strong mode and auto_weak mode. In strong mode, 32768Hz OSC always runs at the highest power consumption. In auto_weak mode, however, it runs in strong mode for the first 7.5 seconds and changes back to auto_weak mode automatically to save powers.

6.4. Power Savings Mode

The SPCE040A also offers a power savings mode (standby mode) for low power application needs. To enter standby mode, the desired key wakeup port(IOA[7:0]) must be configured to input first. And read the Port_IOA_Latch(R) to latch the IOA state before entering the standby mode. Also remember to enable the corresponding interrupt source(s) for wakeup. After that, stop the CPU clock by writing the STOP CLOCK Register (b0~b2 of Port_SystemClock (W)) to enter standby mode. In such mode, SRAM and I/Os remain in the previous states till CPU being awoken. The wakeup sources in SPCE040A include Port IOA7 - 0 and IRQ1 - IRQ6. After SPCE040A is awoken, the CPU will continue to execute the program. Programmer can also enable or disable the 32768Hz OSC when CPU is in standby mode.

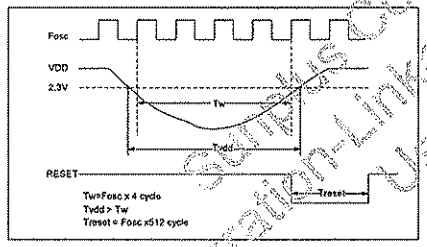
6.5. Low Voltage Detection and Low Voltage Reset

6.5.1. Low voltage detection (LVD)

The Low Voltage Detection (LVD) reports the circumstance of present voltage. There are four LVD levels to be selected: 2.5V, 2.9V, and 3.3V. These levels can be programmed via Port_LVD_Ctrl (W). As an example, suppose LVD is given to 2.9V. When the voltage drops below 2.9V, the b15 of Port_LVD_Ctrl is read as HIGH. In such state, program can be designed to react to this condition.

6.5.2. Low voltage reset

In addition to the LVD, the SPCE040A has another important function, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below 2.3V for 4 consecutive clock cycles. Without LVR, the CPU becomes unstable and malfunction when the operating voltage drops below 2.3V. The LVR will reset all functions to the initial operational (stable) states when the voltage drops below 2.3V. A LVR timing diagram is given as follows:



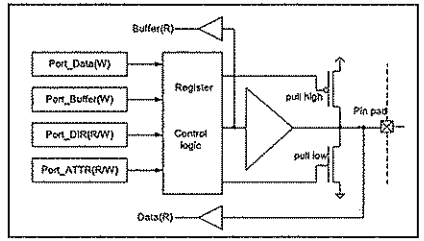
6.6. Interrupt

The SPCE040A has 14 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources.

Interrupt Source	Interrupt Name	Priority
Fosc/1024	FIQ_PWM/IRQ0_PWM	High(FIQ)
Timer A	FIQ_TMA/ IRQ1_TMA	High(FIQ)
Timer B	FIQ_TMB/ IRQ2_TMB	High(FIQ)
EXT2	IRQ3_EXT2	Low
EXT1	IRQ3_EXT1	Low
Key change wakeup	IRQ3_KEY	Low
4096Hz	IRQ4_4KHz	Low
2048Hz	IRQ4_2KHZ	Low
1024Hz	IRQ4_1KHz	Low
4Hz	IRQ5_4Hz	Low
2Hz	IRQ5_2Hz	Low
Time-base 1	IRQ6_TMB1	Low
Time-base 2	IRQ6_TMB2	Low
UART (TxRDY or RxRDY)	UART IRQ	Low

6.7. I/O

Two I/O ports are built in SPCE040A, PortA and PortB. The PortA is an ordinary I/O with programmable wakeup capability. In addition to the regular IO function, the PortB can also perform some special functions in certain pins. Suppose operating voltage is running at 3.6V (VDD) and VDDIO (power for I/O) operates from 3.6V (VDD) to 5.5V. In such condition, the I/O pad is capable of operating from 0V through VDDIO. The following diagram is an I/O schematic.



Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R). The IOA [7:0] is the key wakeup port. To activate key wakeup function, latch data on PORT_IOA_Latch and enable the key wakeup function. Wakeup is triggered when the PortA state is different from at the time latched. In addition to an ordinary I/O port, PortB carries some special functions. A summary of PortB special functions is listed as follows:

Special function in PortB

PortB	Special Function	Function Description	Note
IOB0	SCK	Serial interface clock	Refer to see SIO section
IOB1	SDA	Serial interface data	Refer to see SIO section
IOB2	EXT1	External interrupt source 1(Negative-edge Triggered)	IOB2 set as input mode
	Feedback Output1	Works with IOB4 by adding a RC circuit between them to get an OSC to EXT1 interrupt	IOB2 set as inverted output
IOB3	EXT2	External interrupt source 2(Negative-edge Triggered)	IOB3 set as input mode
	Feedback Output2	Works with IOB5 by adding a RC circuit between them to get an OSC to EXT2 interrupt	IOB3 set as inverted output
IOB4	Feedback Input1		
IOB5	Feedback Input2		
IOB7	Rx	UART Receiver	Refer to see UART section
IOB8	APWMO	TimerA PWM output	Refer to Timer/Counter section
IOB9	BPWMO	TimerB PWM output	Refer to Timer/Counter section
IOB10	Tx	UART Transmitter	Refer to UART section

Default state: Pull Low
PWM: Pulse Width Modulation

Refer to the above table, the configuration of IOB2, IOB3, IOB4, and IOB5 involves feedback function in which an OSC frequency can be obtained from EXT1 (EXT2) by simply adding a RC circuit between IOB2 (IOB3) and IOB4 (IOB5).

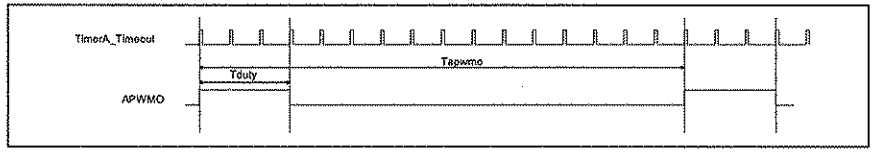
6.8. Timer/Counter

The SPCE040A provides two 16-bit timers/counters, TimerA and TimerB. The TimerA is called a universal counter. TimerB is a general-purpose counter. The clock source of TimerA comes from the combination of clock source A and clock source B. In TimerB, the clock source is given from source C. When timer overflows, an INT signal is sent to CPU to generate a time-out signal.

Clock of Source A	Clock of Source B	Clock of Source C
Fosc/2	2048Hz	Fosc/2
Fosc/256	1024Hz	Fosc/256
32768Hz	256Hz	32768Hz
8192Hz	TMB1	8192Hz
4096Hz	4Hz	4096Hz
1	2Hz	1
0	1	0
EXT1	EXT2	EXT1

Initially, write a value of N into a timer and select a desired clock source, timer will start counting from N, N+1, N+2, ... through FFFF. An INT (TimerA/TimerB) signal is generated at the next clock after reaching "FFFF" and the INT signal is transmitted to INT controller for further processing. At the same time, N will be reloaded into timer and start all over again. The clock source A is a high frequency source and clock source B is a low frequency source. The combination of clock source A and B provides a variety of speeds to TimerA. A "1" represents pass signal and not gating. In contrast, "0" indicates deactivating timer. The EXT1 and EXT2 are the external clock sources. Moreover, counter can generate time-out signal for input clock source to a four bits (16 levels) PWM pulse width counter. A variety of clock duration can be generated and exported from IOB8 (APWMO) and IOB9 (BPWMO).

The following example is a 3/16-duration cycle. The APWMO waveform is made by selecting a pulse width through Port_TimerA_Ctrl (W) [9:6]. As a result, each 16 cycles will generate a pulse width defined in control port. These PWM signals can be applied for controlling the speed of motor or other devices.



Generally speaking, the clock source A and C are fast clock sources and source B comes from RTC system (32768Hz). Therefore, clock source B can be utilized as a precise counter for time counting, e.g., the 2Hz clock can be used for real time counting.

6.8.1. Timebase

Timebase, generated by 32768Hz, is a combination of frequency selections. The outputs of timebase block are named to TMB1 and TMB2. TMB1 is frequency for TimerA (Clock source B). The TMB1 and TMB2 are the sources for Interrupt (IRQ6). Furthermore, timebases generates additional 2Hz to 4096Hz interrupt sources (IRQ4 and IRQ5) for Real-Time-Clock (RTC).

TMB2	TMB1
128Hz	8Hz
256Hz	16Hz
512Hz	32Hz
1024Hz	64Hz
Default: 128Hz	Default: 8Hz

6.9. Sleep, Wakeup and Watchdog

6.9.1. Wakeup and sleep

1) Sleep: After power-on reset, IC starts running until a sleep command occurs. When a sleep command is accepted, IC will turn the system clock (PLL) off. After all, it enters sleep mode.

2) Wakeup: CPU waking up from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The IRQ signal makes CPU to complete the wakeup process and initialization. The key wakeup and interrupt sources (IRQ1 - IRQ6) can be used for wakeup sources.

6.9.2. Watchdog

The purpose of watchdog is to monitor if the system operates normally. Within a certain period, watchdog must be cleared. If watchdog is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. The watchdog function can be removed by bonding option. In SPCE040A, the clear period is 0.75 seconds. If watchdog is cleared within each 0.75 seconds, the system will not be reset. To clear watchdog, simply write "0bxxxx xxxx xxxx xx01" to Port_Watchdog_Clear(W). The content written to Port_Watchdog_Clear (W) for watchdog clearance must be exactly the same as the one illustrated above (0bxxxx xxxx xxxx xx01). Other values given to the Port_Watchdog_Clear (W) for watchdog clearance may end up with system reset. The watchdog function remains enabled during standby mode if the 32768Hz is turned on.

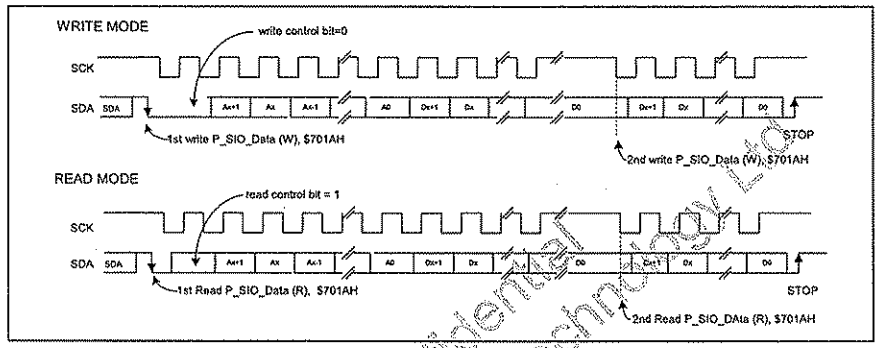
6.10. ADC (Analog to Digital Converter) / DAC

The SPCE040A has eight channels 10-bit ADC (Analog to Digital Converter). The function of an ADC is to convert analog signal to digital signal, e.g. a voltage level into a digital word. The eight channels of ADC can be seven channels of line-in from IOA [6:0] or one channel microphone (MIC) input through amplifier and AGC controller. The MIC amplifier circuit is capable of reducing common mode noise by transmitting signals through differential MIC inputs (MICN, MICP). Moreover, an external resistor can be applied to adjust microphone gain and time of AGC operating. The AD needs to select source of line-in before conversion. The ADC is able to choose the external or internal (=AVDD) top reference voltage. If constant voltage source is unavailable, SPCE040A offers a constant voltage 2.0V with 5.0mA driving ability with a capacitor connected.

The SPCE040A has two 10-bit D/A with 2.0mA or 3.0mA driving current for audio outputs, DAC1 and DAC2.

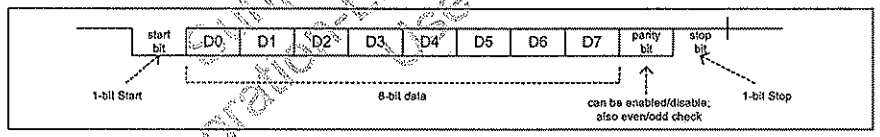
6.11. Serial interface I/O (SIO)

Serial interface I/O offers a one-bit serial interface for communication. This serial interface is capable of transmitting or receiving data via two I/O pins, IOB0 (SCK) and IOB1 (SDA).



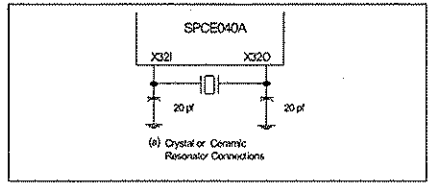
6.12. UART

UART block provides a full-duplex standard interface that facilitates the communication with other devices. With this interface, SPCE can transmit and receive simultaneously. The maximum baud-rate can be up to 115200bps. This function can be accomplished by using PortB and Interrupt (UART IRQ). The Rx and Tx of UART are shared with IOB7 and IOB10. When SPCE040A receives and/or transmits a frame of data, the b7 (RxRDY) and/or b6 (TxRDY) in Port_UART_Command2(R) will be set to "1" and the UART IRQ is activated at the same time.



6.13. Audio Algorithm

The following speech types can be used in SPCE040A: PCM, LOG PCM, SACM_A3200, SACM_S240, SACM_S480, SACM_S530, SACM_S720, SACM_A1600, SACM_A2000, and SACM_A2000_DVR (Digital Voice Recorder). For melody synthesis, the SPCE040A supports SACM_MS01 (FM) and SACM_MS02 (wave-table) synthesizers.



6.14. Bonding Option Summary

The SPCE040A has the following bonding options:

1). Watchdog function

凌陽科技
SUNPLUS

DATA SHEET

SPRS256B

256K-bit Serial RAM

SEP. 20, 2001

Version 1.0

256K-BIT SERIAL RAM

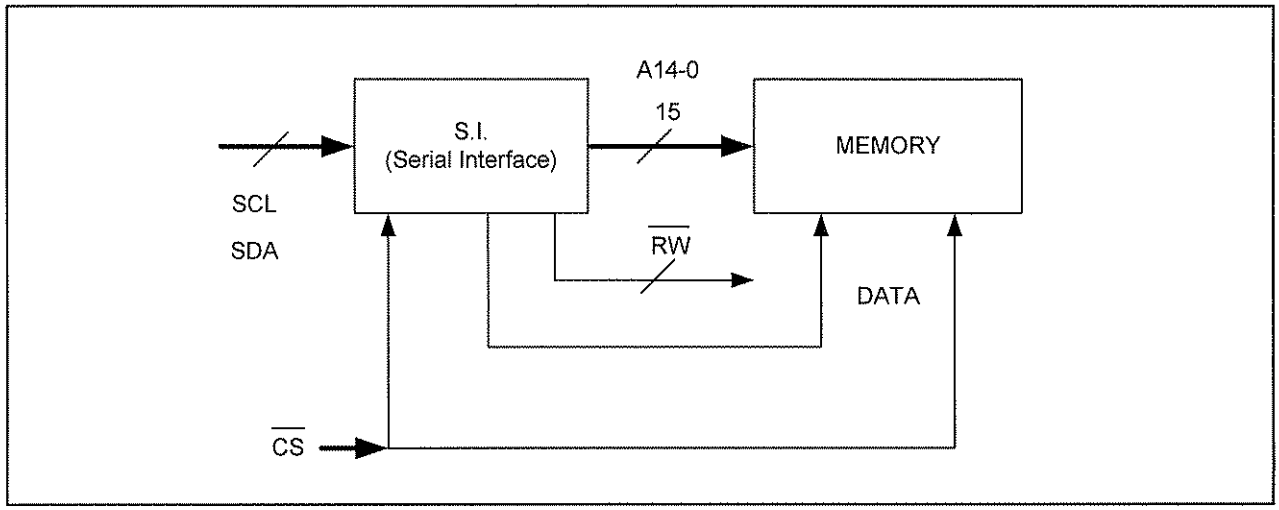
1. GENERAL DESCRIPTION

The SPRS256B is a low power 256K-bit serial static RAM. It is ideal for applications requiring long operating time or non-volatile storage with back-up batteries. The output port is a 3-state output that allows easy expansion of memory capacity.

2. FEATURES

- Fast Access time ---- 250ns @ VDD = 3.0V
- Low supply current ---- operation:
  250μA (Typ) @ VDD = 3.0V and F_{SCL} = 2.0MHz
  Standby: 5μA (Typ)
- Completely static ---- two-pin access
- Single power supply ---- 2.4V to 3.6V
- Non-volatile storage with back-up batteries

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
$\overline{CS}$	1	I	Chip select, Low Active
SCL	2	I	Serial clock input
SDA	3	I/O	Serial Input / Output data
VSS	4	I	Ground
VDD	5	I	Power input
LP	6	I/O	Must be floating

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 4.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Ratings table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

5.2. DC Characteristics (VDD = 2.4V - 3.6V, T_A = 0℃ to 60℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Low Current	I_{IL}	-1.0	-	1.0	μA	V_{IN} = 0 to VDD
Output Low Current	I_{OL}	-1.0	-	1.0	μA	Chip disable
Output High Voltage	V_{OH}	2.0	-	-	V	I_{OH} = 100μA
Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 400μA
Standby Current	I_{STBY}	-	5.0	-	μA	Chip disable
Operating Current	I_{DD}	-	0.1	1.0	mA	F_{SCL} = 2.0MHz, no load

5.3. AC Characteristics (VDD = 2.4V - 3.6V, T_A = 0℃ to 60℃)

Test Condition V_{IH} = VDD, V_{IL} = 0V

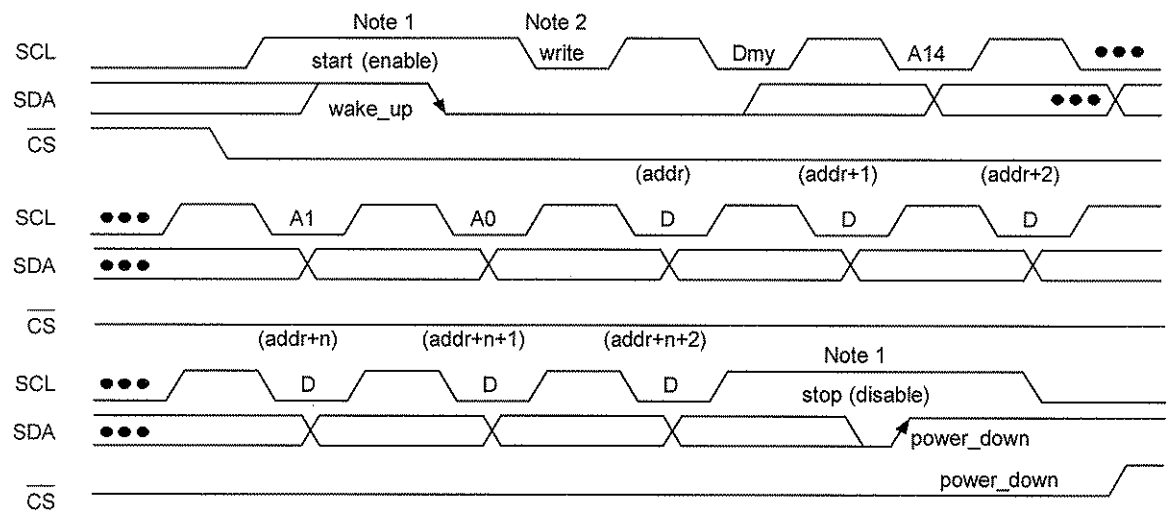
Input Rise and Fall Times = 10ns

I/O Timing Reference Level = 1.5V

Output Load: C_{LOAD} = 50pF

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
SCL setup time	T_{CS}	100	-	-	ns	
SDA setup time	T_{DS}	100	-	-	ns	
SDA hold time	T_{DH}	10	-	-	ns	
Access time	T_{ACC}	-	-	700	ns	VDD = 2.4V
				250	ns	VDD = 3.0V
SCL frequency	f_C	-	-	500K	Hz	VDD = 2.4V
		-	-	2000K	Hz	VDD = 3.0V

5.4. Write Mode



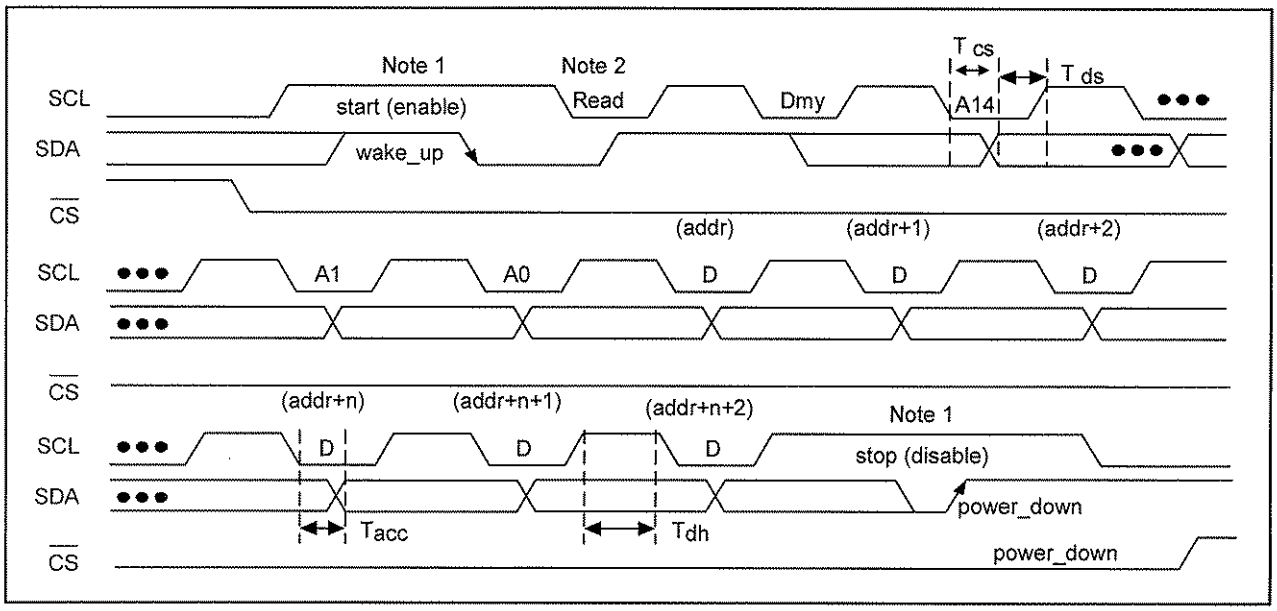
Note1: At the positive half cycle of the SCL clock cycle ,

Start operation	SCL = " H " and SDA changes from " H " to " L "
Stop operation	SCL = " H " and SDA changes from " L " to " H " , or when $\overline{CS}$ = " H "

Note2: At the next SCL clock cycle of the start operation ,

Write operation	SCL = " H " and SDA = " L "
Read operation	SCL = " H " and SDA = " H"

5.5. Read Mode



SUNPLUS

DATASHEET

SPR23L822A

8M-Bit Serial ROM

Preliminary

MAR. 25, 2003

8M-BIT SERIAL ROM (8 BIT OUTPUT)

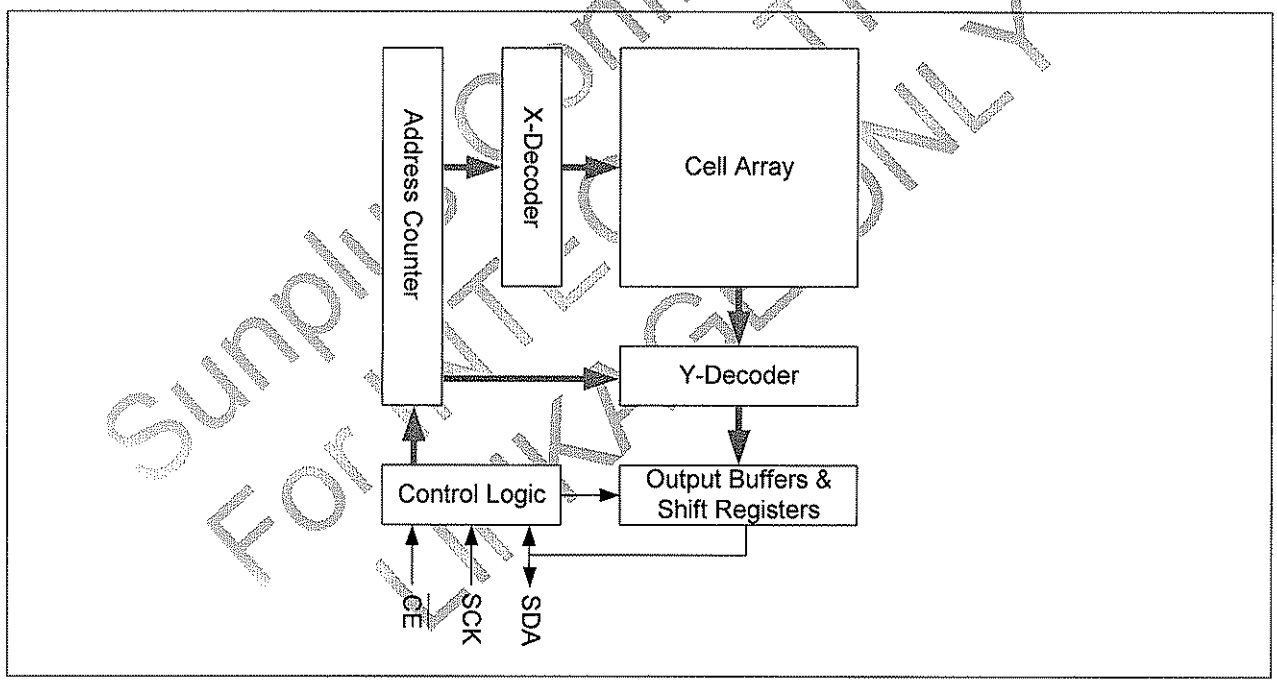
1. GENERAL DESCRIPTION

This device is a mask programmable Serial ROM fabricated by advance CMOS technology. It is organized as 1M x 8b. $\overline{CE}$ pin polarity can be set as high active or low active by mask option and is selected from confirm sheet. This device operates with low power supply voltage, 2.4V - 3.6V and can be accessed with only 2 pins (SDA & SCK), which assure extremely easy operation.

2. FEATURES

- Bit organization
  - 1M x 8
- Fast access time
  - 166ns(max.) @ 2.4V - 3.6V
- Current
  - Operating: 2.0mA
  - Standby: 2.0μA
- Supply voltage
  - 2.4V - 3.6V
  - All inputs and outputs TTL compatible

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	Type	Description
$\overline{CE}$	I	Chip Enable *
SCK	I	Serial accessing clock
SDA	I/O	Serial Address input / Data output
VSS	I	Ground
VDD	I	Power
NC	I	NC

Note: * $\overline{CE}$ pin polarity can be set by mask option.

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Voltage on any Pin Relative to VSS	V_{IN}	-0.3V to 4.3V
Ambient Operating Temperature	T_{OPR}	0℃ to 70℃
Storage Temperature	T_{STG}	-65℃ to 125℃

Note1: Minimum DC voltage on input or I/O pins is -0.5V.
During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VDD+0.5V. During voltage transitions, input may overshoot VDD to VDD+2.0V for periods of up to 20ns.

Note2: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

5.2. DC Characteristics (VDD = 2.4V - 3.6V, T_A = 0°C - 70°C)

Characteristics	Symbol	Min.	Max.	Conditions
Output High Voltage	V_{OH}	2.2V	-	I_{OH} = -0.4mA
Output Low Voltage	V_{OL}	-	0.4V	I_{OL} = 1.6mA
Input High Voltage	V_{IH}	2.2V	VDD+0.3V	
Input Low Voltage	V_{IL}	-0.3V	0.2 x VDD	
Input Leakage Current	I_{LI}	-	2.0μA	0V, VDD*
Output Leakage Current	I_{LO}	-	2.0μA	0V, VDD*
Operating Current	I_{CC1}	-	2.0mA	t_{CK} = 166ns, all output open
Standby Current	I_{STB}	-	2.0μA	$\overline{CE}$ **> VDD-0.2V or $\overline{CE}$ ***<0.2V All inputs=GND
Input Capacitance	C_{IN}	-	10pF	T_A = 25°C, f = 1.0MHz
Output Capacitance	C_{OUT}	-	10pF	T_A = 25°C, f = 1.0MHz

Note: *Input leakage current of SDA exists when input voltage is not VSS or VDD. Maximum leakage current is 280uA(SDA=1.6V) and –110uA(SDA=2V) when VDD=3.6V.

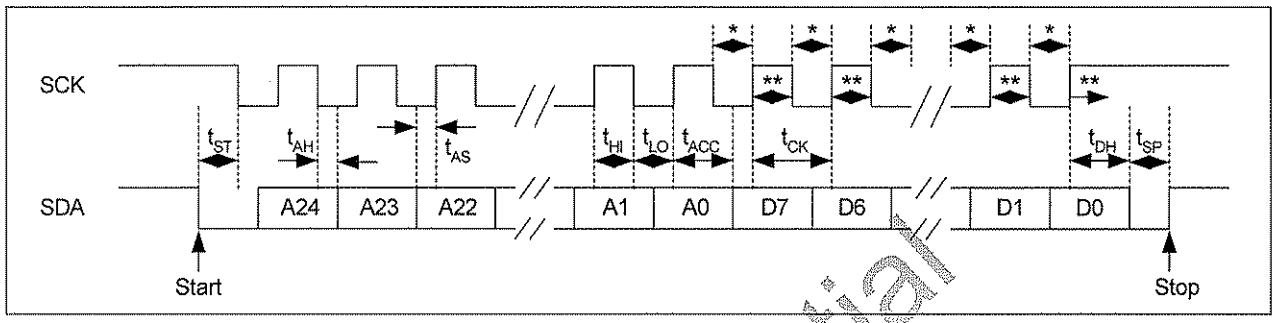
** $\overline{CE}$ polarity defined as low active, *** $\overline{CE}$ polarity defined as high active.

5.3. AC Characteristics (VDD=2.4V - 3.6V, T_A = 0°C - 70°C)

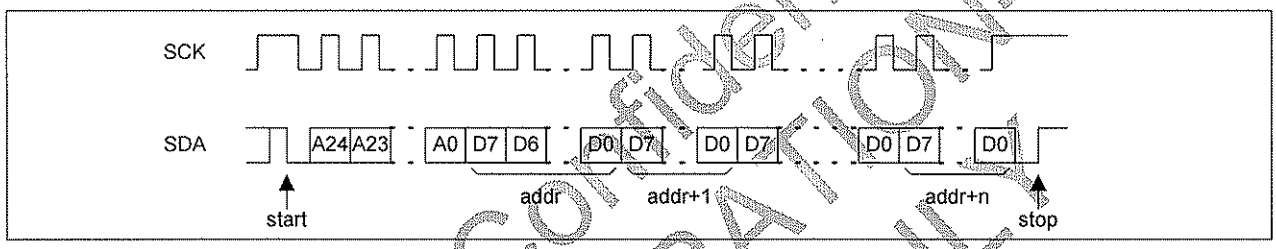
Characteristics	Symbol	Min.	Max.	Unit
Period of SCK	t_{CK}	166	-	ns
Low period of SCK clock	t_{LO}	70	-	ns
High period of SCK clock	t_{HI}	70	-	ns
Address setup time	t_{AS}	15	-	ns
Address hold time	t_{AH}	15	-	ns
READ access time	t_{ACC}	-	166	ns
Start setup time	t_{ST}	70	-	ns
Stop setup time	t_{SP}	70	-	ns
READ data hold time	t_{DH}	-	15	ns
Rise time of SCK	t_{RSCL}	-	10	ns
Fall time of SCK	t_{FSCL}	-	10	ns
Rise time of SDA	t_{RSDA}	-	10	ns
Fall time of SDA	t_{FSDA}	-	10	ns

5.4. Timing Diagram

5.4.1. Read command



5.4.2. Successive read command



Note: *Master terminal of Serial Interface (SIF) must keep Hi-Z to avoid bus contention.

**Serial ROM (Slave terminal of SIF) will stop driving output to avoid bus contention.