Operational Description

1 PRODUCT OVERVIEW

The **Segway PT (Personal Transporter)** is a two-wheeled, self-balancing transportation device. Computers and motors in the base keep the Segway upright at all times. Gyroscopes are used to detect departures from perfect balance.

There is a InfoKey Controller that uses 2.4 GHz spread spectrum technology to communicate with the Segway PT. The InfoKey Controller has four buttons around the outer edge and a display in the center. The controller is used to turn on the Segway PT and set the operating modes. The controller operates from 2405 to 2475 MHz.

2 ANTENNA REQUIREMENT FOR FCC 15.203

The antennas are internal to the EUT and not readily available to be modified by the end user. Therefore it meets the 15.203 Requirement.

The FOB Antenna is permanently installed inside of the EUT. The antenna is a trace on the circuit board.

The UIC Antenna is permanently installed inside of the EUT. It has a unique Connector and cannot be readily accessed by the end user.

3 RF CIRCUIT DESCRIPTION

Product Description

The ***CC2420*** is a true single-chip 2.4 GHz IEEE 802.15.4 compliant RF transceiver designed for low-power and low-voltage wireless applications. ***CC2420*** includes a digital direct sequence spread spectrum baseband modem providing a spreading gain of 9 dB and an effective data rate of 250 kbps.

The ***CC2420*** is a low-cost, highly integrated solution for robust wireless communication in the 2.4 GHz unlicensed ISM band. It complies with worldwide regulations covered by ETSI EN 300 328 and EN 300 440 class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan).

The ***CC2420*** provides extensive hardware support for packet handling, data buffering, burst transmissions, data encryption, data authentication, clear channel assessment, link quality indication and packet timing information. These features reduce the load on the host controller and allow ***CC2420*** to interface low-cost microcontrollers.

The configuration interface and transmit / receive FIFOs of ***CC2420*** are accessed via an SPI interface. In a typical application ***CC2420*** will be used together with a microcontroller and a few external passive components.

CC2420 is based on Chipcon's SmartRF®-03 technology in 0.18 µm CMOS.

Key Features

- True single-chip 2.4 GHz IEEE 802.15.4 compliant RF transceiver with baseband modem and MAC support
- DSSS baseband modem with 2 MChips/s and 250 kbps effective data rate.
- Suitable for both RFD and FFD operation
- Low current consumption (RX: 18.8 mA, TX: 17.4 mA)
- Low supply voltage (2.1 – 3.6 V) with integrated voltage regulator
- Low supply voltage (1.6 – 2.0 V) with external voltage regulator
- Programmable output power
- No external RF switch / filter needed
- I/Q low-IF receiver
- I/Q direct upconversion transmitter
- Very few external components
- 128(RX) + 128(TX) byte data buffering
- Digital RSSI / LQI support
- Hardware MAC encryption (AES-128)
- Battery monitor
- QLP-48 package, 7x7 mm
- Complies with ETSI EN 300 328, EN 300 440 class 2, FCC CFR-47 part 15 and ARIB STD-T66
- Powerful and flexible development tools available

3 Features

- 2400 – 2483.5 MHz RF Transceiver
  - Direct Sequence Spread Spectrum (DSSS) transceiver
  - 250 kbps data rate, 2 MChip/s chip rate
  - O-QPSK with half sine pulse shaping modulation
  - Very low current consumption (RX: 18.8 mA, TX: 17.4 mA)
  - High sensitivity (-95 dBm)
  - High adjacent channel rejection (30/45 dB)
  - High alternate channel rejection (53/54 dB)
  - On-chip VCO, LNA and PA
  - Low supply voltage (2.1 – 3.6 V) with on-chip voltage regulator
  - Programmable output power
  - I/Q low-IF soft decision receiver
  - I/Q direct up-conversion transmitter
- Separate transmit and receive FIFOs
  - 128 byte transmit data FIFO
  - 128 byte receive data FIFO
- Very few external components
  - Only reference crystal and a minimised number of passives
  - No external filters needed
- Easy configuration interface
  - 4-wire SPI interface
  - Serial clock up to 10 MHz
- 802.15.4 MAC hardware support:
  - Automatic preamble generator
  - Synchronisation word insertion/detection
  - CRC-16 computation and checking over the MAC payload
  - Clear Channel Assessment
  - Energy detection / digital RSSI
  - Link Quality Indication
  - Full automatic MAC security (CTR, CBC-MAC, CCM)
- 802.15.4 MAC hardware security:
  - Automated security operations within the receive and transmit FIFOs.
  - CTR mode encryption / decryption
  - CBC-MAC authentication
  - CCM encryption / decryption and authentication
  - Stand-alone AES encryption
- Development tools available
  - Fully equipped development kit
  - Demonstration board reference design with microcontroller code
  - Easy-to-use software for generating the ***CC2420*** configuration data
- Small size QLP-48 package, 7 x 7 mm
- Complies with EN 300 328, EN 300 440 class 2, FCC CFR47 part 15 and ARIB STD-T66

8 Circuit Description

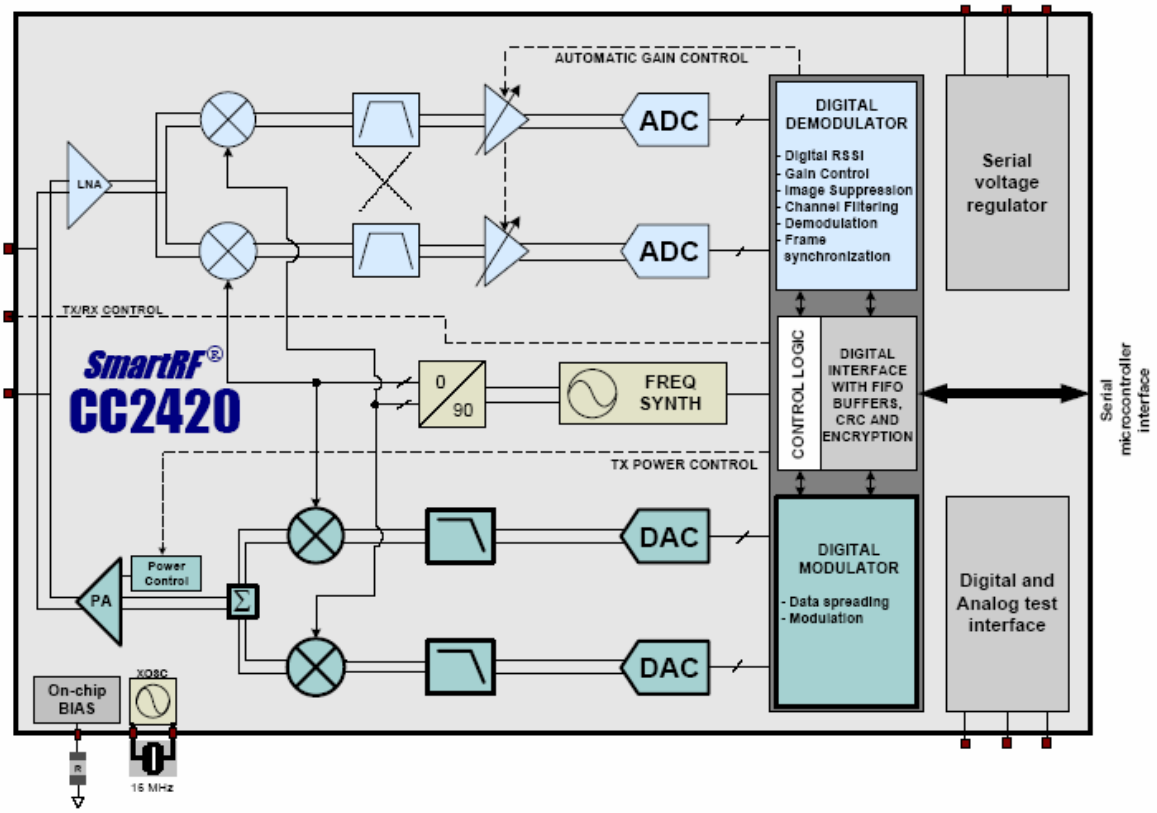

Figure 2. *CC2420* simplified block diagram

A simplified block diagram of ***CC2420*** is shown in Figure 2.

CC2420 features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF (2 MHz), the complex I/Q signal is filtered and amplified, and then digitized by the ADCs. Automatic gain control, final channel filtering, de-spreading, symbol correlation and byte synchronisation are performed digitally.

When the SFD pin goes high, this indicates that a start of frame delimiter has been detected. ***CC2420*** buffers the received data in a 128 byte receive FIFO. The user may read the FIFO through an SPI interface. CRC is verified in hardware. RSSI and correlation values are appended to the frame. CCA is available on a pin in receive mode. Serial (unbuffered) data modes are also available for test purposes.

The ***CC2420*** transmitter is based on direct up-conversion. The data is buffered in a 128 byte transmit FIFO (separate from the receive FIFO). The preamble and start of frame delimiter are generated by hardware. Each symbol (4 bits) is spread using the IEEE 802.15.4 spreading sequence to 32 chips and output to the digital-to-analog converters (DACs).

An analog lowpass filter passes the signal to the quadrature (I and Q) upconversion mixers. The RF signal is amplified in the power amplifier (PA) and fed to the antenna.

The internal T/R switch circuitry makes the antenna interface and matching easy. The RF connection is differential. A balun may be used for single-ended antennas. The biasing of the PA and LNA is done by connecting TXRX_SWITCH to RF_P and RF_N through an external DC path.

The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase splitter for generating the I and Q LO signals to the down-conversion mixers in receive mode and up-conversion

mixers in transmit mode. The VCO operates in the frequency range 4800 – 4966 MHz, and the frequency is divided by two when split in I and Q.

A crystal must be connected to XOSC16_Q1 and XOSC16_Q2 and provides the reference frequency for the synthesizer. A digital lock signal is available from the PLL.

The digital baseband includes support for frame handling, address recognition, data buffering and MAC security.

The 4-wire SPI serial interface is used for configuration and data buffering.

An on-chip voltage regulator delivers the regulated 1.8 V supply voltage. The voltage regulator may be enabled / disabled through a separate pin.

A battery monitor may optionally be used to monitor the unregulated power supply voltage. The battery monitor is configurable through the SPI interface.