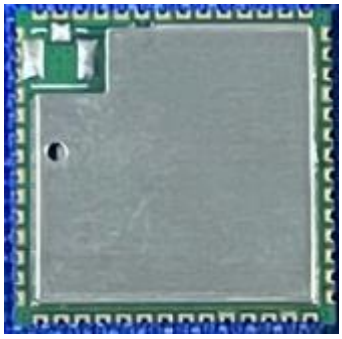
GOC-RG440-WZ



WIFI Module Hardware Specification

Document Type: WIFI Module Hardware SpecificationDocument Number: GOC-RG440-WZ

Document Version: V1.4

Release Date: 2020/08/13

NOTE:

1. The module must use ladder steel net, and recommend ladder steel net thickness 0.16--0.20mm. The adaptability of the products is adjusted accordingly.
2. Before the use of the module, bake at 60 degrees centigrade and bake for 12 hours.

Release Record

Version Number	Release Date	Comments
V1.0	2018/08/31	Initial draft
V1.1	2019/04/19	Update Module height
V1.2	2019/08/30	Increase packing methods and performance parameters, Cancel reference design
V1.3	2020/06/20	Update Pin Diagram and Electrical Characteristic
V1.4	2020/08/13	Update Bluetooth Standard

Contents

1. Introduction

GOC-RG440-WZ is a highly integrated module that support 802.11b/g/n, SDIO (SDIO 1.1/2.0/3.0) interface, and HS-UART mixed interface. It combines a WLAN MAC,a 1T1R capableWLAN baseband, and RF in s single chip. The RTL8821CS provides a complete solution for a high- performance integrated wireless device.

GOC-RG440-WZ baseband implements Or thogonal Frequency Division Multiplexing (OFDM) STA mode with one transmit and one receive path (1T1R). Features include one spatial stream transmission, short Guard Interval (GI) of 400ns, spatial spreading, and support for variant channel bandwidth. Moreover, GOC-RG440-WZ provides one spatial stream space-time block code (STBC), Transmit Low Density Parity Check (LDPC) to extend the range of transmission. As the recipient, the RTL8821CS also supports explicit sounding packetfeedback that helps senders capability. For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b, 802.11g and 802.11n data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability are available, and CCK provides support for legacy data rates, with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation of the individual subcarriers, and rate compatiblecoding rate of 1/2, 2/3, 3/4, and 5/6,.

GOC-RG440-WZ it supports scatterrnet topology and allows active links in slave mode, and active linksin master mode..

2. WIFI Features

- Support IEEE 802.11b/g/n
- Maximum PHY data rate up to 86.7Mbps using 20MHz bandwidth, 200Mbps using
- 40MHz bandwidth, and 433.3Mbps
- Backward compatible with 802.11b/g/n devices while operating at 802.11n data rates
- G-SPI interface for configurable endian for WLAN
- Complies with HS-UART with configurable baud rate
- IEEE 802.11b/g/n/ compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- IEEE 802.11k Radio Resource Measurement
- WAPI (Wireless Authentication Privacy Infrastructure) certified.
- Cisco Compatible Extensions (CCX) for WLAN devices MAC Features

3. Specification

Feature	Description
Model Name	GOC-RG440-WZ
WIFI	
Frequency Band	2.4GHz
Interface	SDIO1.1/2.0/3.0
Size	17mm*17mm*2.4mm
Operating temperature	-40℃~+85℃

Storage Temperature	-55℃~+125℃
VBAT	3.3V
VDD_PIO	1.8V or 3.3V
Working current	350mA
Max current	<700mA
Humidity	Operating Humidity 60% to 85% Non-Condensing

Table 1: Specifications

4. Pin Diagram And Description

6.1 Pin Diagram

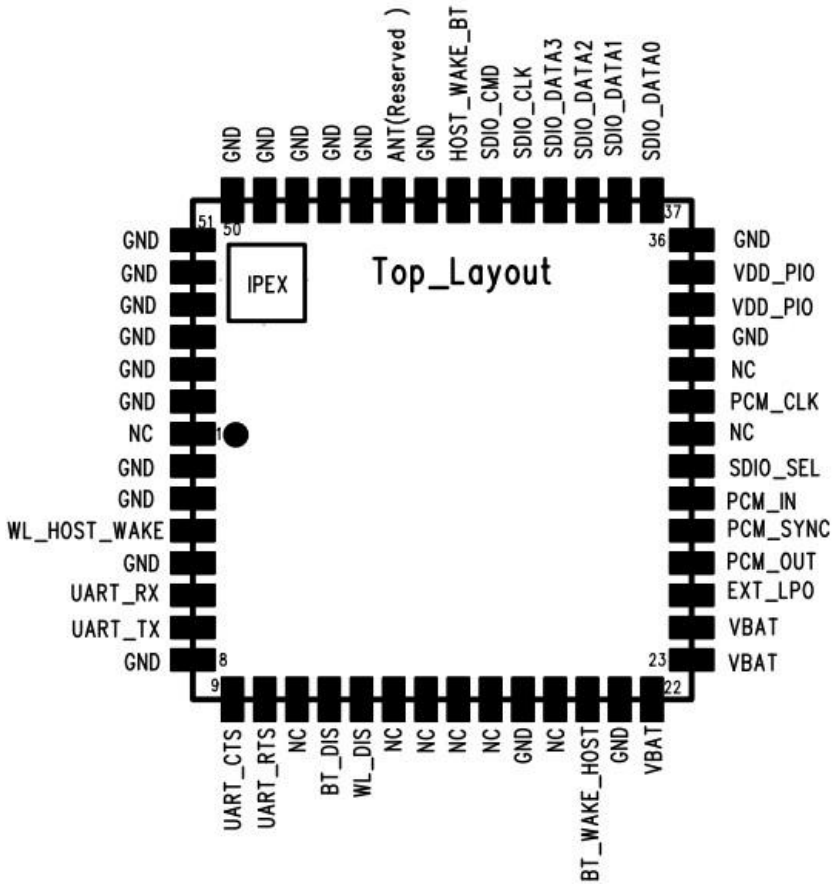


Figure 2: GOC-RG440-WZ Pin

6.2 Pin Description

Pin	Pin Name	**Type**	Description
1	NC	NC	NC
2	GND	Ground	Ground
3	GND	Ground	Ground
4	WL_HOST_WAKE	Input/Output	WL_HOST_WAKE
5	GND	Ground	Ground
6	UART_RX	Input	High-Speed UART Data In

7	UART_TX	Output	High-Speed UART Data Out
8	GND	Ground	Ground
9	UART_CTS	Input	High-Speed UART CTS
10	UART_RTS	Output	High-Speed UART RTS
11	NC	NC	NC
12	BT_DIS	Input	
13	WL_DIS	Input	WIFI enable
14	NC	NC	NC
15	NC	NC	NC
16	NC	NC	NC
17	NC	NC	NC
18	GND	Ground	Ground
19	NC	NC	NC
20	WAKE_HOST	Input/Output	device to wake-up HOST
21	GND	Ground	Ground
22	VBAT	POWER	3.3V Supply Voltage
23	VBAT	POWER	3.3V Supply Voltage
24	VBAT	POWER	3.3V Supply Voltage
25	EXT_LPO	Output	External sleep clock input (32.768 kHz)(Reserved)
26	PCM_OUT	Output	PCM data Output
27	PCM_SYNC	Output	PCM Synchronization control
28	PCM_IN	Input	PCM data Input
29	SDIO_SEL	Input/Output	General Purpose Input/ Output Pin(Reserved)
30	NC	NC	NC
31	PCM_CLK	Input/Output	PCM clock
32	NC	NC	NC
33	GND	Ground	Ground
34	VDD_PIO	POWER	1.8V~3.3V Supply Voltage
35	VDD_PIO	POWER	1.8V~3.3V Supply Voltage
36	GND	Ground	Ground
37	SDIO_DATA0	Input/Output	SDIO Data Line 0
38	SDIO_DATA1	Input/Output	SDIO Data Line 1
39	SDIO_DATA2	Input/Output	SDIO Data Line 2
40	SDIO_DATA3	Input/Output	SDIO Data Line 3
41	SDIO_CLK	Input	SDIO Clock Input
42	SDIO_CMD	Input/Output	SDIO Command Input
43	HOST_WAKE_BT	Input/Output	HOST_WAKE_BT
44	GND	Ground	Ground
45	ANT	RF	WIFI(2.4G) Antenna(Reserved)
46	GND	Ground	Ground
47	GND	Ground	Ground
48	GND	Ground	Ground
49	GND	Ground	Ground
50	GND	Ground	Ground
51	GND	Ground	Ground
52	GND	Ground	Ground
53	GND	Ground	Ground
54	GND	Ground	Ground
55	GND	Ground	Ground

56	GND	Ground	Ground

Table 2: Pin Description

6.3 PCB Layout Footprint

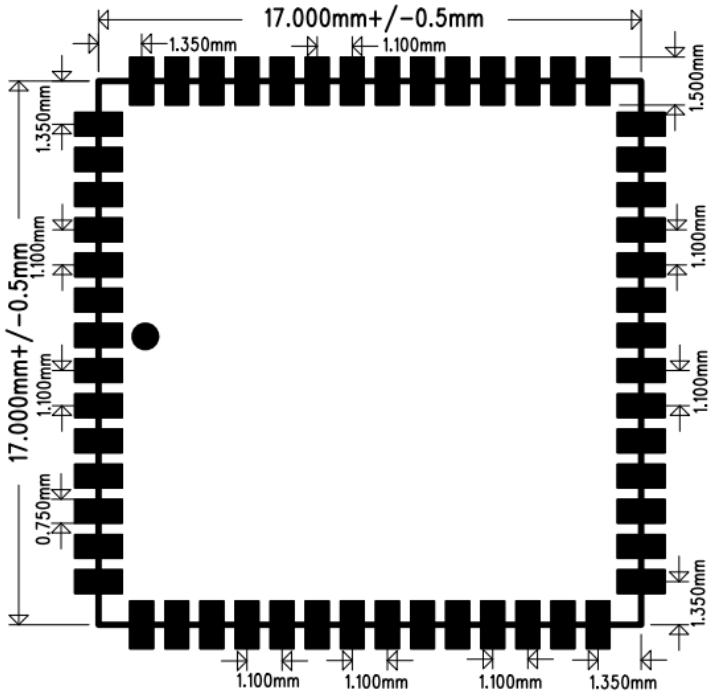


Figure 3: PCB Layout Footprint

6.4 Module Package

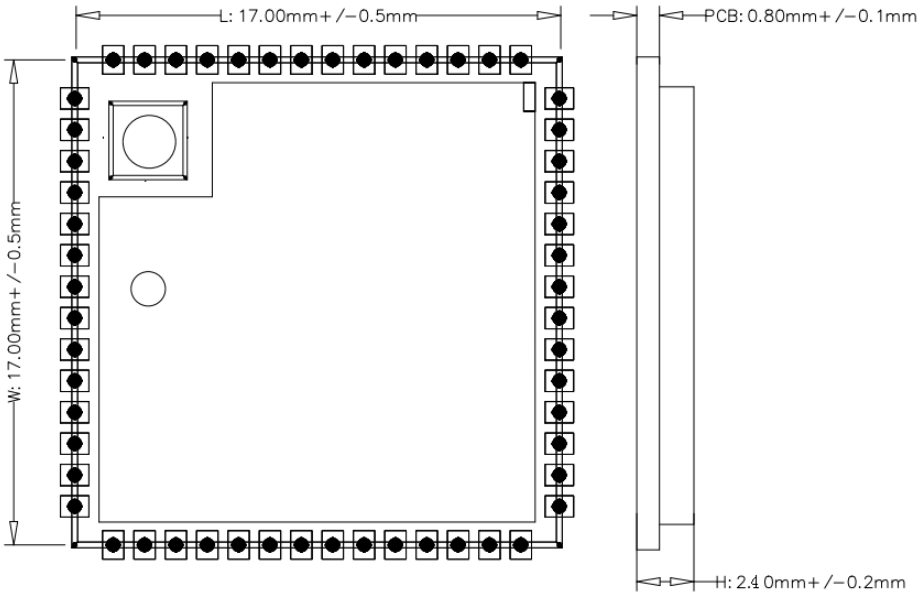


Figure 4: Module Package

5. Echo Cancellation Principle

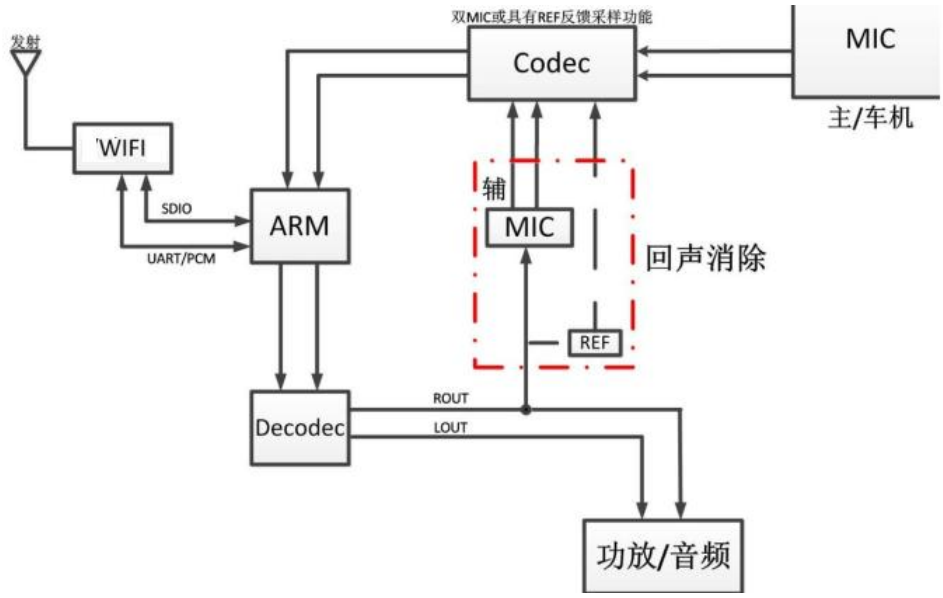


Figure 5: Echo Cancellation Principle

The left picture is a schematic diagram of the echo cancellation principle. After Decodec decoding of the leftand right channel sound, after data sampling and master MIC data comparison, echo cancellation can be processed. The right picture is a reference example, which can be designed according to the actual plan.

Flying echo cancellation design, priority to use the echo cancellation design of IFLYTEK.

6. Power Management Handshake Interface Signal Level

1) SD_RESET Signal Level

The SD_RESET signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the GOC-RG440-WZ via the VDD_IO pin.

2) BT_DIS Signal Level

The BT_DIS signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the GOC-RG440-WZ via the VDD_IO_1 pin.

3) WL_DIS_N Signal Level

The WL_DIS_N signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8821CS via the VDD_IO pin.

4) VBAT_EN Signal Level

The VBAT_EN signal level ranges from 1.8V to 3.3V

8.1 System Power On Sequence

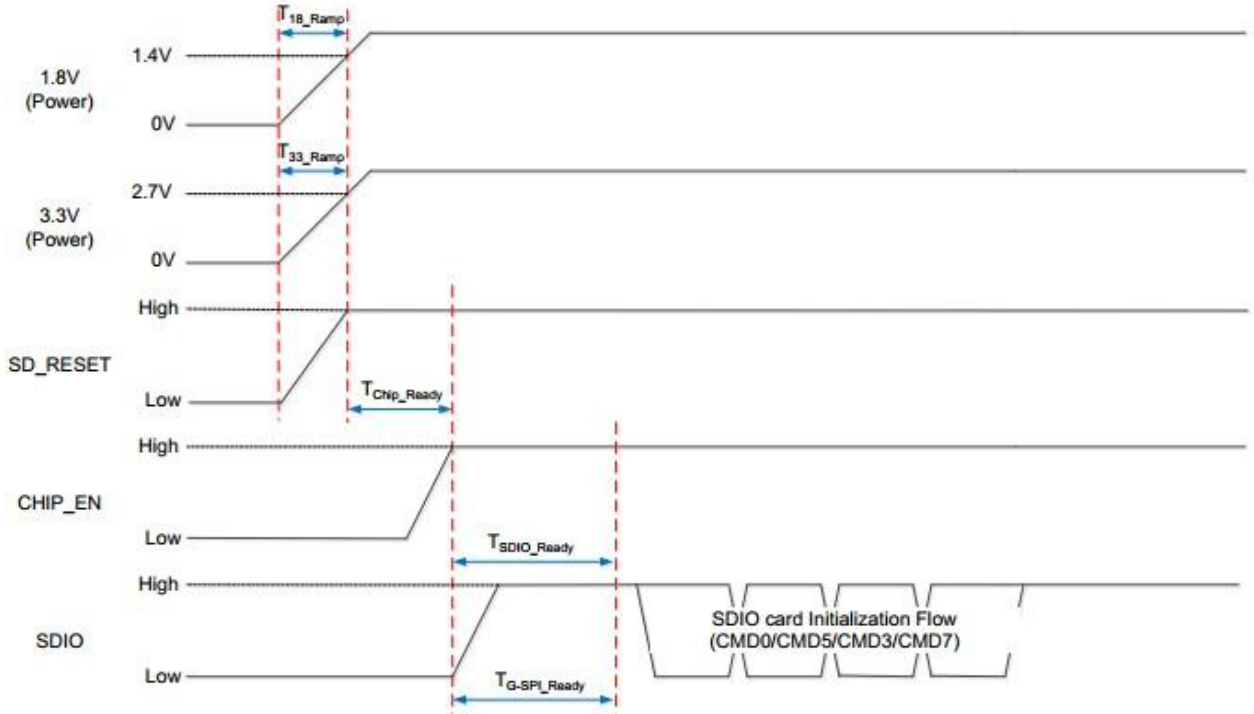


Figure 6: System Power-On Sequence

	Min	Typical	Max	Unit	Description
T_{18_Ramp}	0.1	0.5	2.5	ms	The 1.8V main power ramp up duration.
$T3_{3\_Ramp}$	0.1	0.5	2.5	ms	The 3.3V main power ramp up duration.
T_{Chip_Ready}	0	10	X	ms	CHIP_EN pull high timing
T_{SDIO_Ready}	1	2	10	ms	SDIO Not Ready Duration. In this state, the RTL8821CS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.

Table 3: System Power On Timing Parameters

NOTE:

1) SDIO Interface Power On Sequence

After power-on, the SDIO interface is selected by the RTL8821CS automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power-on sequence is recommended.

We recommend that the card detection procedures are divided into two phases: A 3.3V/1.8V power pre-charge phase and a formal power-up phase.

After main 3.3V ramp up and 1.8V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the SDIO block. eFUSE is then autoloaded to SDIO circuits during the TSDIO_Ready duration and then SDIO pins are pulled up.

After CMD5/5/3/7 procedures,card detection is executed.

2) SD_RESET Power On Sequence

To attain SD_RESET capability, the following power sequence is recommended.

After main 3.3V/1.8V ramp up, the power management unit is enabled by the power ready

detection circuit.

The power management unit enables the SD_RESET function. After power management unit being enabled, SD_RESET needs to keep high for ensuring WLAN and SDIO/G-SPI function being alive.

3) CHIP_EN Power On Sequence

To attain CHIP_EN capability, the following power sequence is recommended.

After main 3.3V/1.8V ramp up, the power management unit is enabled by the power ready detection circuit.

The power management unit enables the CHIP_EN function. After power management unit being enabled, CHIP_EN needs to keep high for ensuring RTL8821CS function being alive.

7. UART Interface

GOC-RG440-WZ UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The interfacesupports the UART HCI H4 and H5 specifications. The default baud rate is 115.2 kbaud. In order to support high and low speed baud rate, the GOC-RG440-WZ provides multiple UART clocks.

Desired BaudRate	Error	Desired Baud Rate	Error
1200	0%	1382400	-0.22%
9600	0%	1444400	-0.20%
14400	0%	1500000	-0.31%
19200	0.01%	1843200	-0.22%
28800	0.01%	2000000	0%
38400	0.04%	2100000	0.25%
57600	0.01%	2500000	0%
76800	0.04%	2764800	-0.22%
115200	-0.08%	3000000	-0.31%
128000	0%	3250000	0.47%
153600	-0.08%	3692300	-0.38%
230400	-0.08%	3710000	0.29%
460800	-0.08%	3750000	0.39%
500000	0%	3800000	0.25%
921600	-0.22%	4000000	0%
1000000	0%		

Table 4: UART Interface Power-On Timing Parameters

8. PCM Interface

GOC-RG440-WZ supports a PCM digital audio interface that is used for transmitting digital audio/voicedata to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/μ-law, and 13/16-bit linear PCM formats
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

9. Electrical Characteristic

11.1 Absolute Maximum Ratings

Maximum Ratings	Min	Typical	Max
VBAT	3.0V	3.3V	3.6V
VDD_PIO	1.71V	1.8V	1.89V
	3.16V	3.3V	3.46V

Table 5: Absolute Maximum Ratings

11.2 Recommended Operating Conditions

Operating Conditions	Min	Typical	Max
Operating Temperature	-40℃	/	+85℃
Storage Temperature	-55℃	/	+125℃
VBAT	3.16V	3.3V	3.46V
VDD_PIO	1.71V	1.8V	1.89V
	3.16V	3.3V	3.46V

Table 6: Recommended Operating Conditions

10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.
Peak package body temperature :<260℃.
Time of peak temperature for Pb-free assembly : 5~10sec.

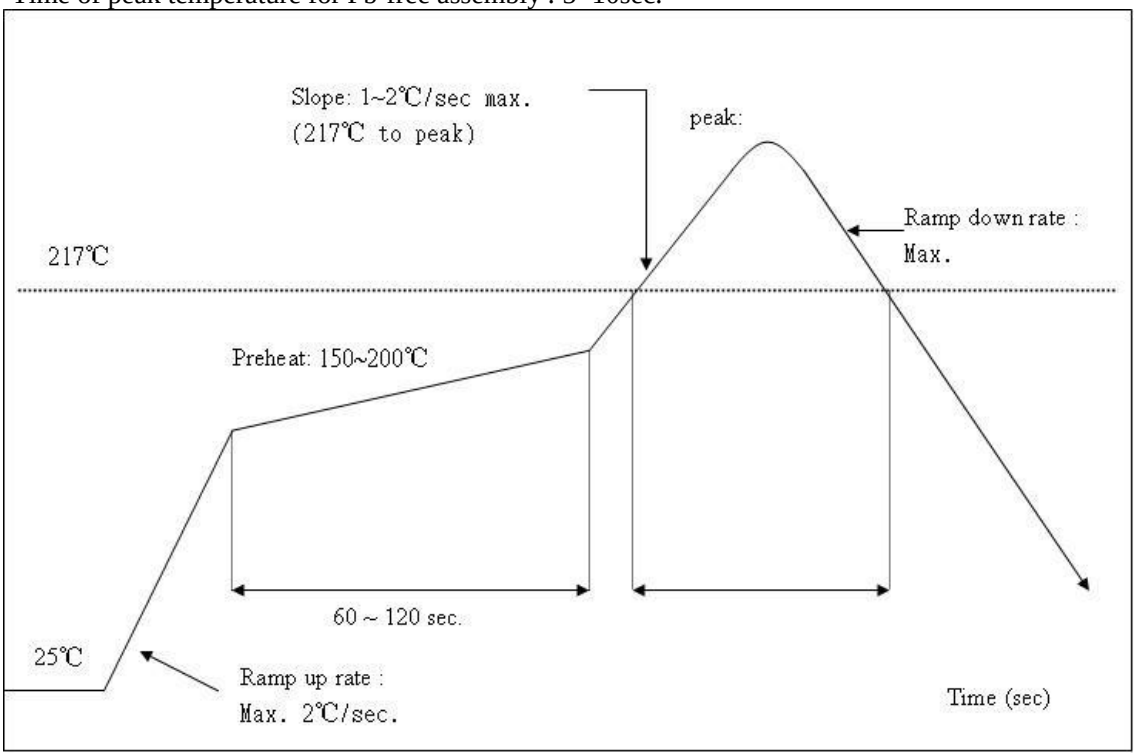


Figure 7 : Recommended Reflow Profile

11. PCB Layout Recommendation

13.1 Antenna

The module have own fixed antenna with max 5.54dBi gain.

13.2 HCI UART Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA.

UART_RX UART_TX UART_CTS UART_RTS

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

13.3 PCM Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 mA.

PCM_SYNC PCM_CLK PCM_OUT PCM_IN

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

13.4 Power Trace Lines Layout Guideline

VBAT Trace Width: 30mil

VDD_PIO Trace Width: 25mil

13.5 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to GOC-RG440-WZ Module Ground Pads.

Decoupling Capacitors close to GOC-RG440-WZ Module Power and Ground Pads.

12. Module Part Number Description

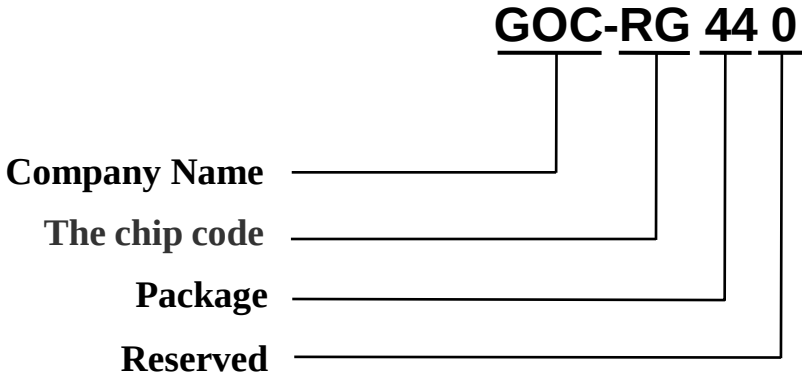


Figure 8: Module Part Number Description

For a list of available options (e.g. package, packing) and orderable part numbers or for further information on any aspect of this device, please go to *www.goodocom.com* or contact the GOODOCOM Sales Office nearest to you.

13. Ordering Information

Part Number	Description	Remark
GOC-RG440-WZ	2.4 GHz module	PIFA Antenna

Table 7: Ordering Information

14. Packaging Information

16.1 Net Weight

The module net weight: 1.3g±0.1g

16.2 Package

72pcs module in one tray 2000pcs modules into one pack 4000pcs Modules One Box Carton size:270mm*275mm*220mm
Tray size:225mm*205mm*7mm

16.3 Storage Requirements

1）Temperature: 22~28℃；

2）Humidity: <70%（RH）；

Vacuum packed and sealed in good condition to ensure 12 months of welding.

16.4 Humidity Sensitive Characteristic

1） MSL: 3 level

2） Once opened, SMT within 168 hours in the condition of temperature: 22~28℃ and humidity<60%(RH).

3） Handling, storage, and processing should follow IPC/JEDECJ-STD-033

§ 15.19 Labeling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

§ 15.21 Information to user.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

§ 15.105 Information to the user.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
-Reorient or relocate the receiving antenna.
-Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated withminimum distance 20cm between the radiator & your body.

2.2 List of applicable FCC rules

Module applicable FCC Part 15.247

2.3 Summarize the specific operational use conditions

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users' body. The host manufacturer installing this module into their product must ensure that the final composit product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operaition. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

2.4 Limited module procedures

Single module approval

2.5 Trace antenna designs

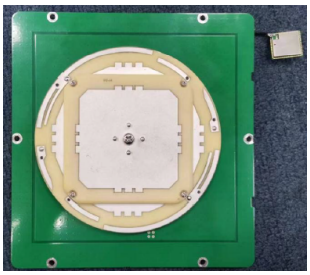
The module have own fixed antenna with max 5.54dBi gain(see below photo)

2.6 RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users' body; and if RF exposure statement or module layout is changed, then the host product manufacturer required to take responsibility of the module through a change in FCC ID or new application. The FCC ID of the module cannot be used on the final product. In these circumstances, the host manufacturer will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.7 Antennas

The module have own fixed antenna with max 5.54dBi gain(see below photo)



2.8 Label and compliance information

The host system using this module, should have label in a visible area indicated the following texts: "Contains FCC ID: SY4-RG440".

2.9 Information on test modes and additional testing requirements

Host manufacturer must perfom test of radiated & conducted emission and spurious emission, etc according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for FCC Part 15 Subpart C 15.247 & 15.207 & 15.209 and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.