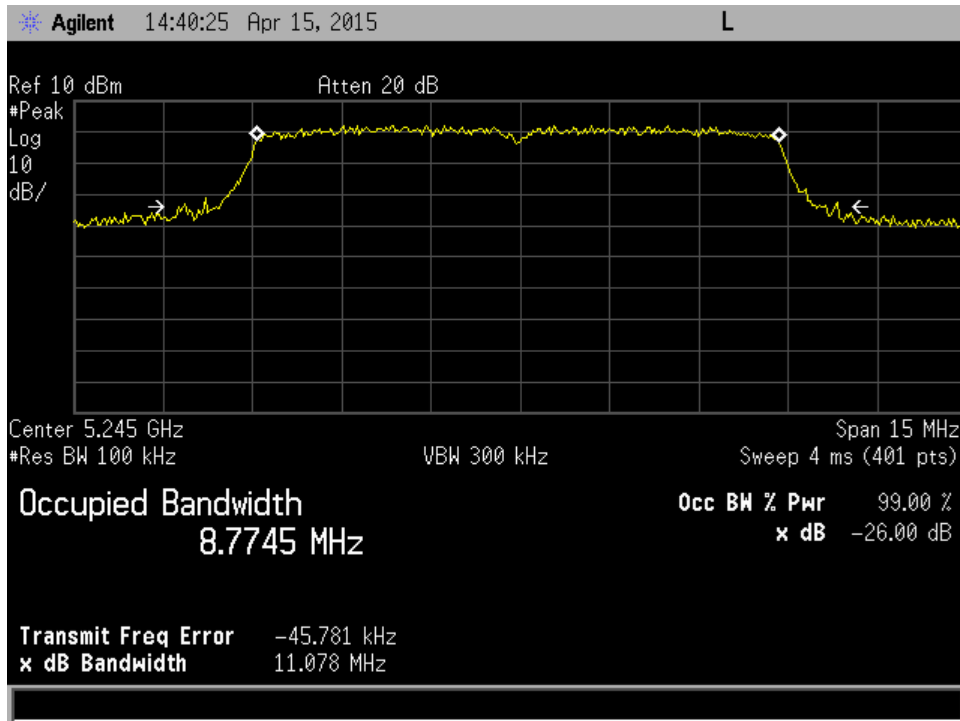




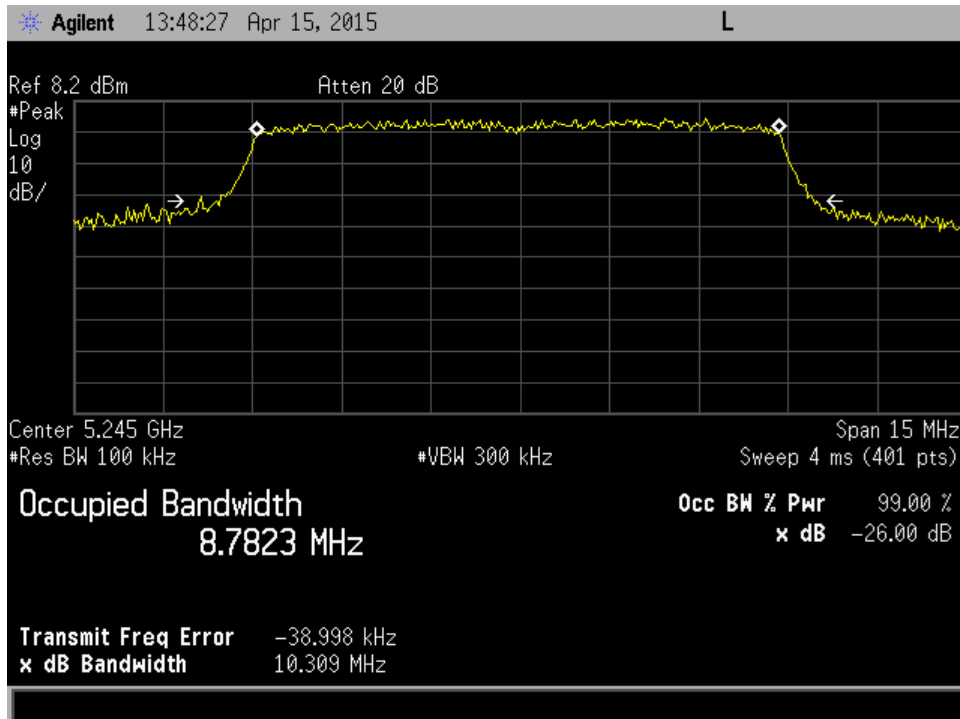
# **Annex D**

## **Occupied Bandwidth**

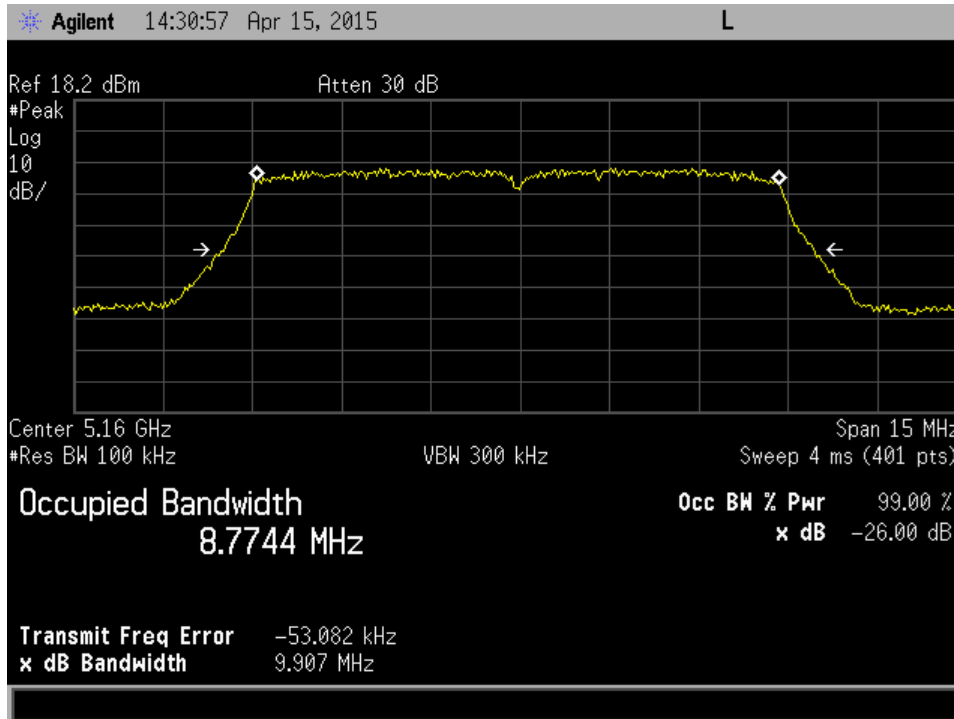
### **Ports J3 and J4**



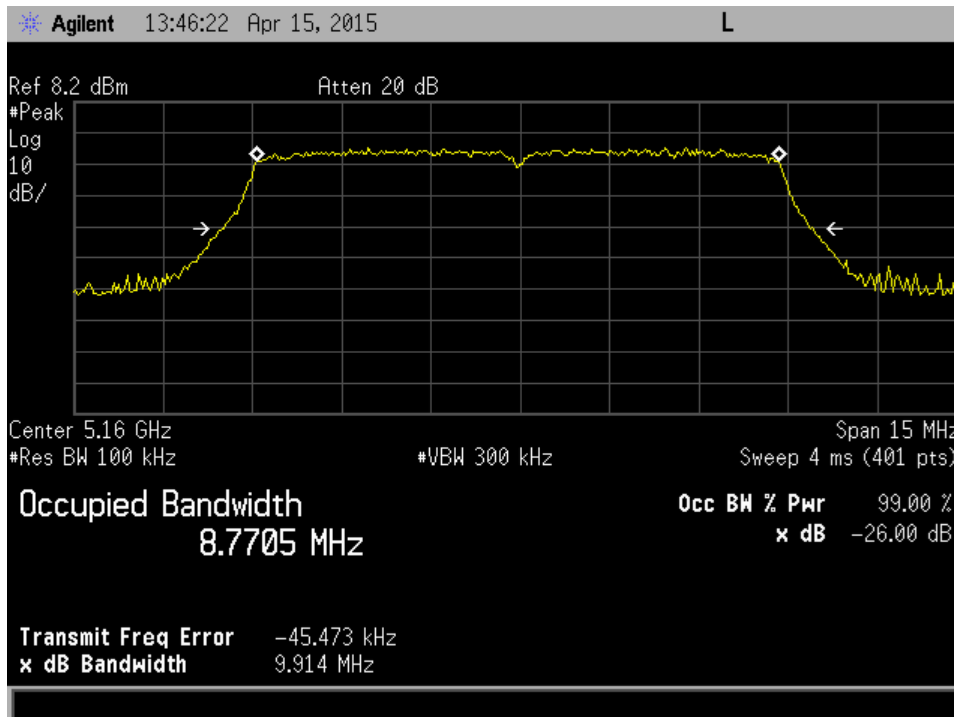
10 MHz high ch\_OCBW\_J3



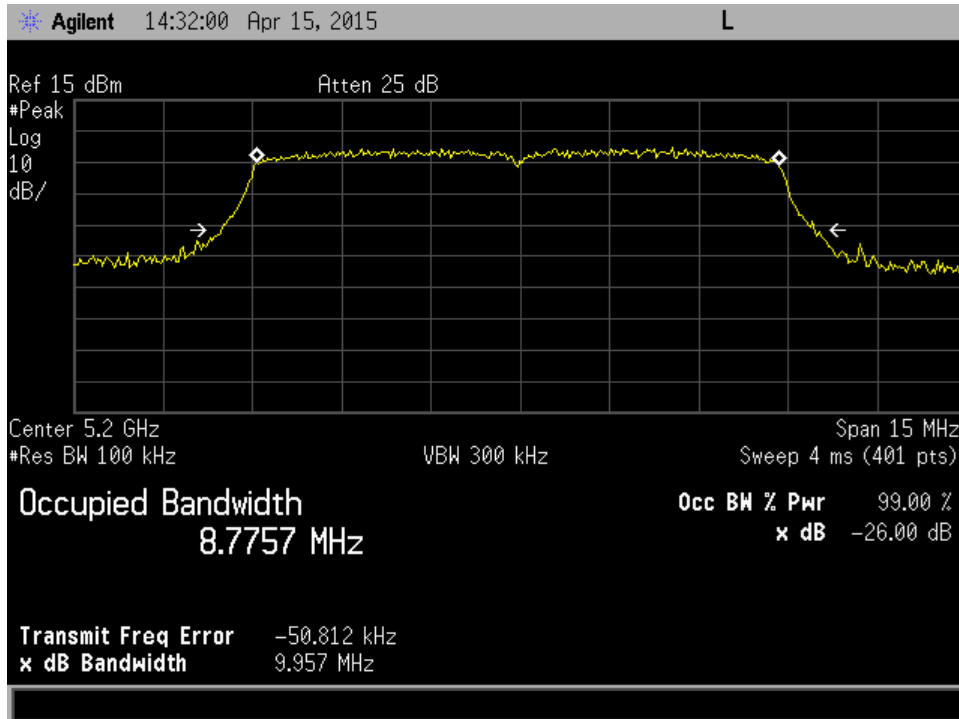
10 MHz high ch\_OCBW\_J4



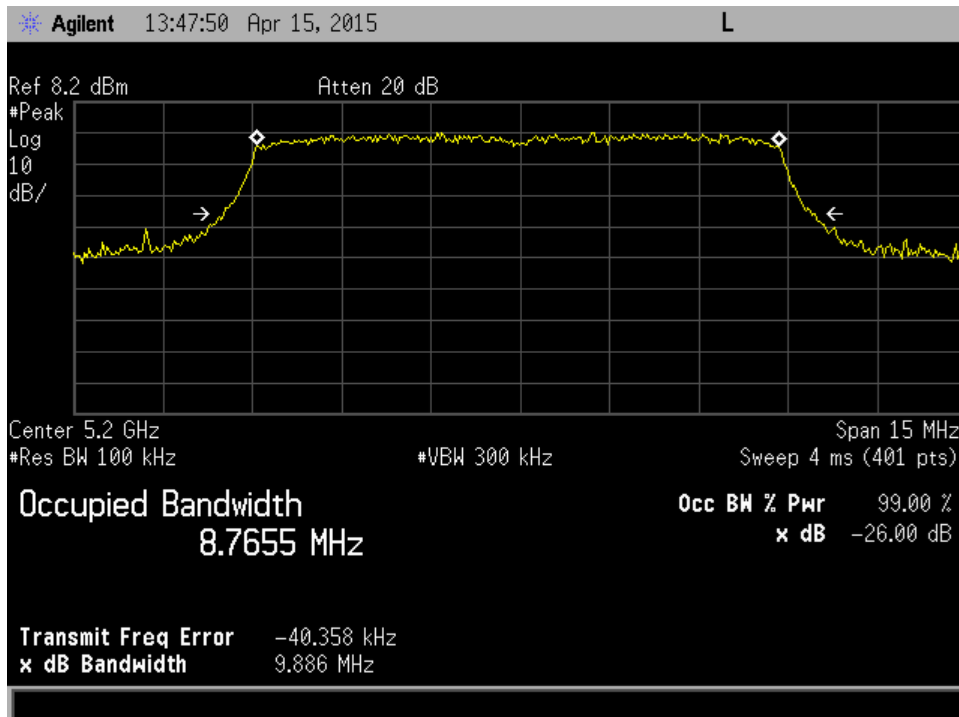
10 MHz low ch\_OCBW\_J3



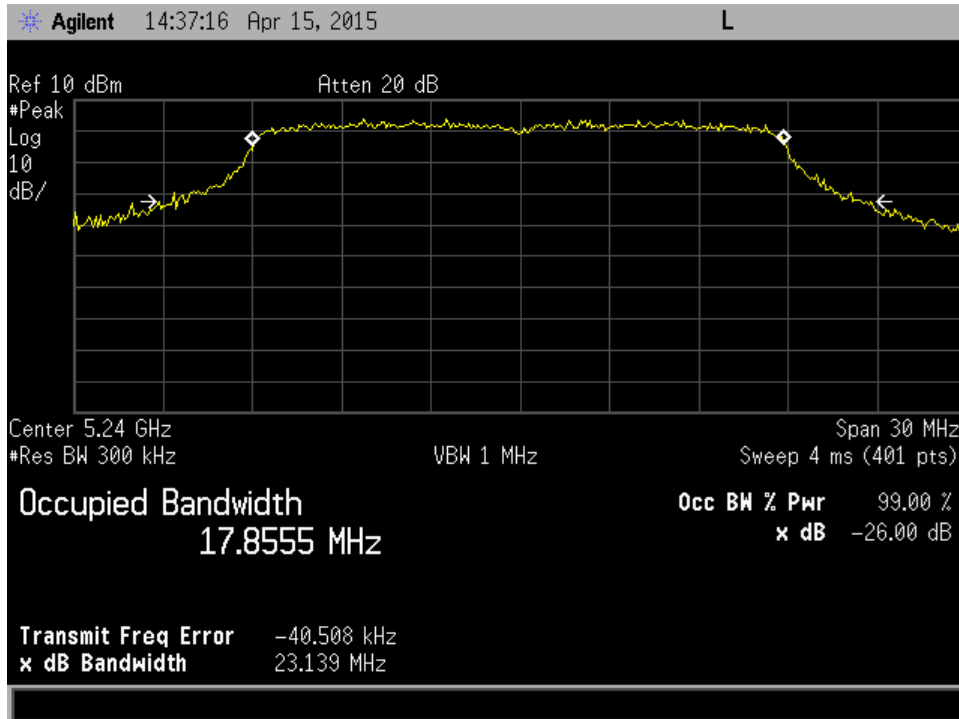
10 MHz low ch\_OCBW\_J4



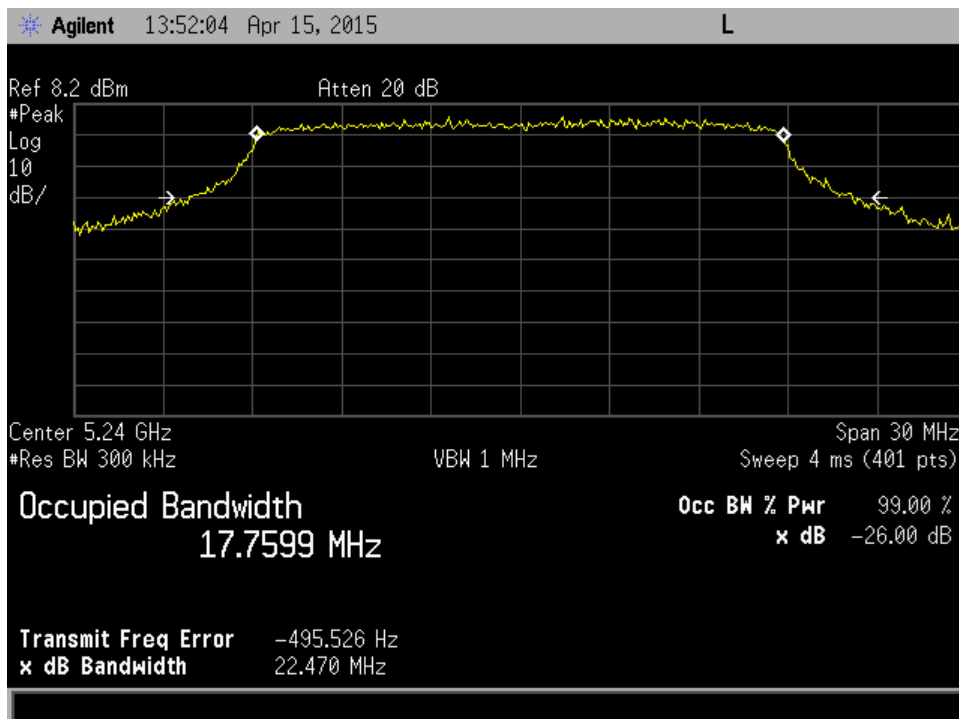
10 MHz mid ch\_OCBW\_J3



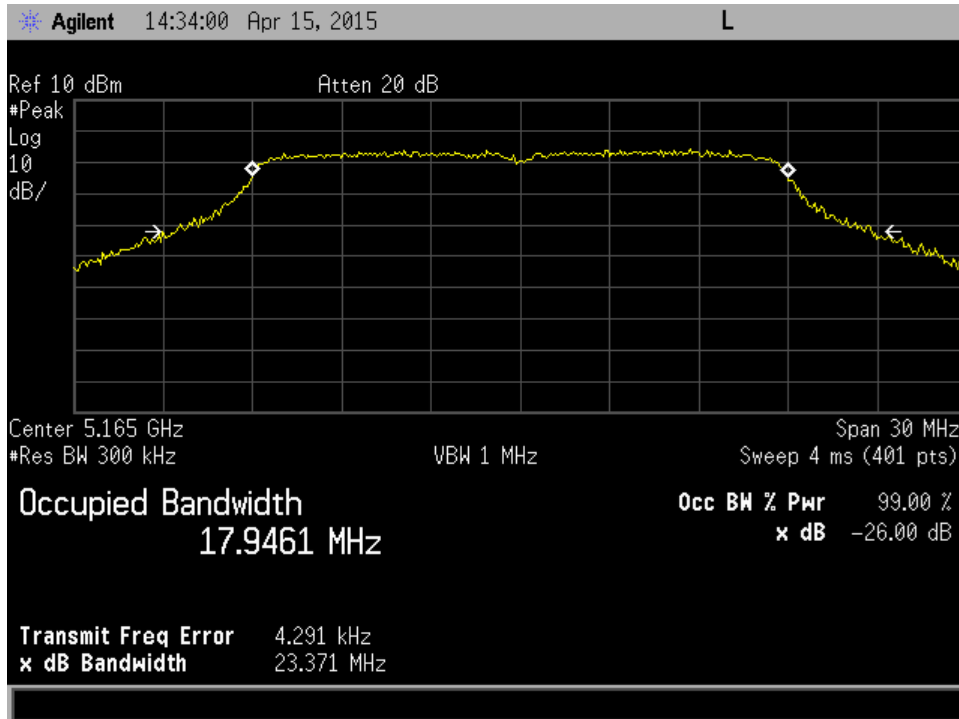
10 MHz mid ch\_OCBW\_J4



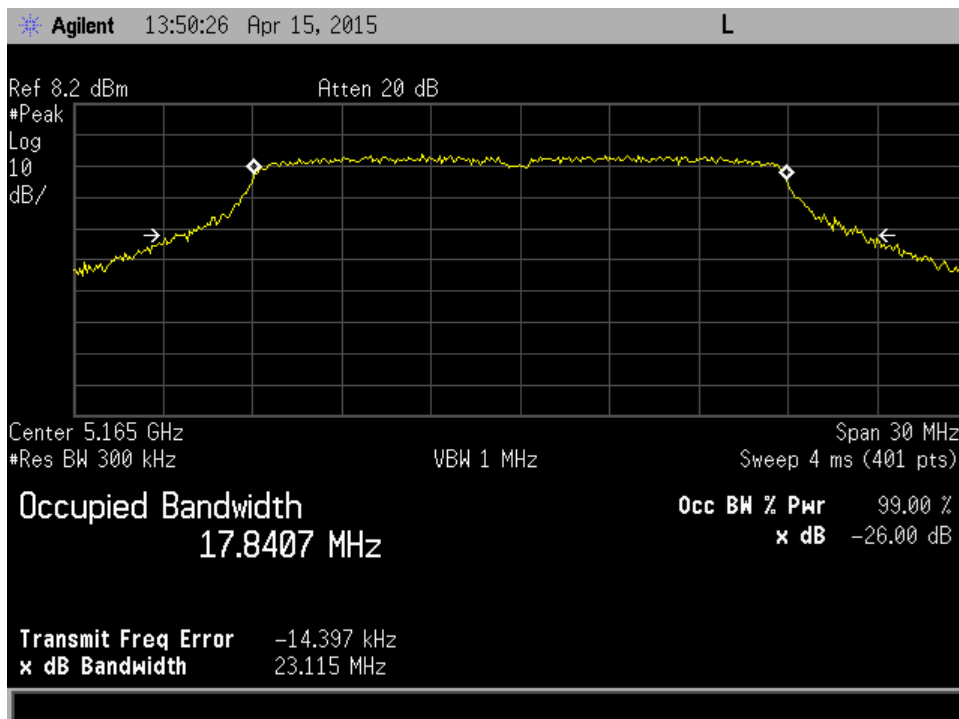
20 MHz high ch\_OCBW\_J3



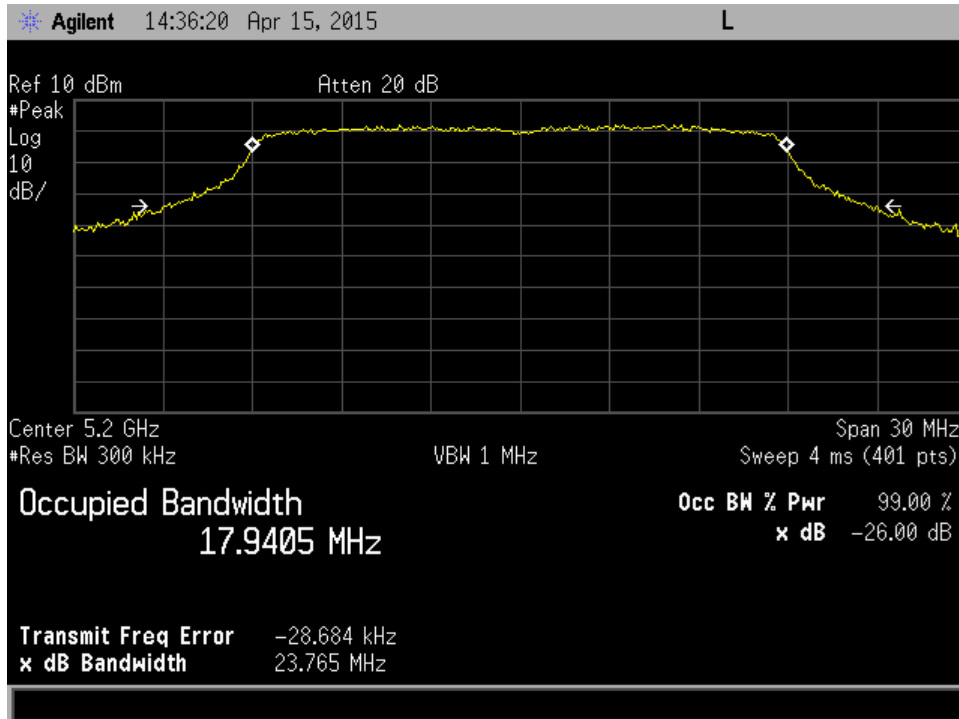
20 MHz high ch\_OCBW\_J4



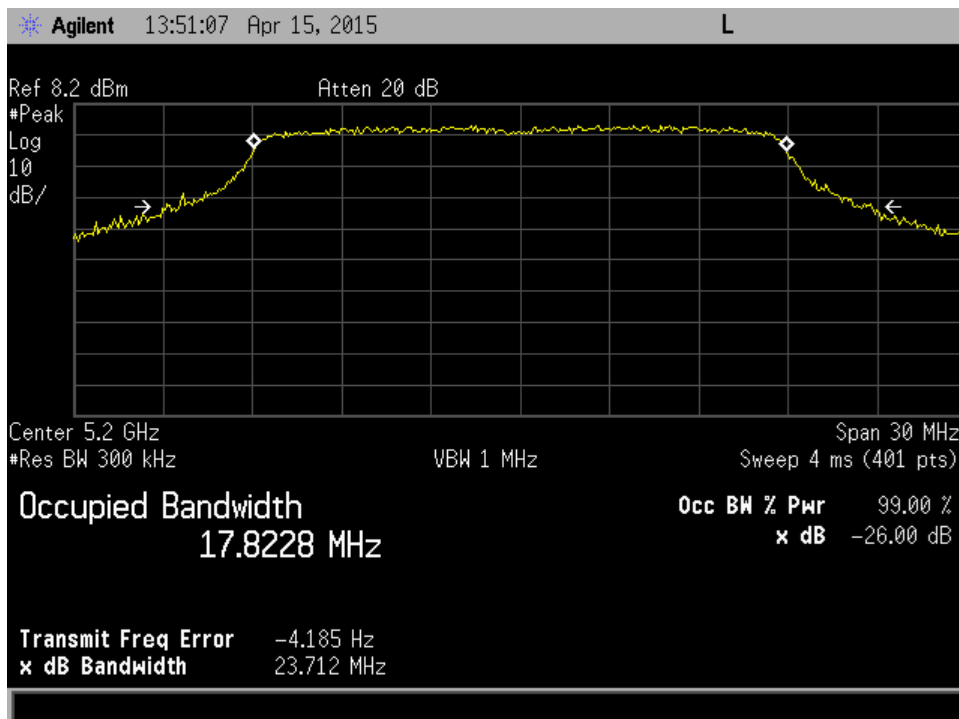
20 MHz low ch\_OCBW\_J3



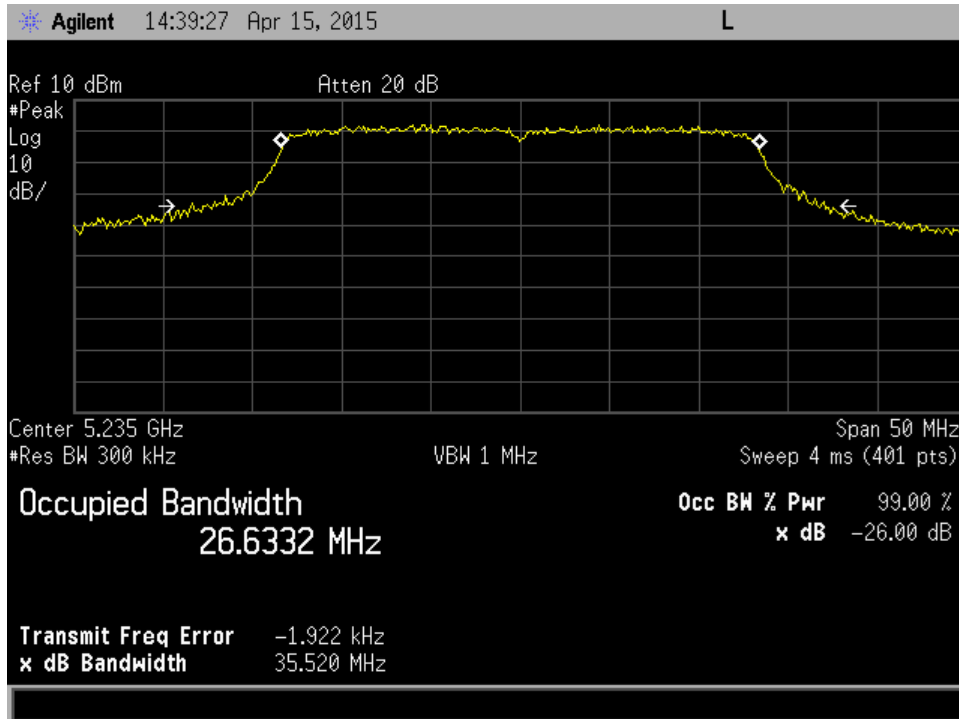
20 MHz low ch\_OCBW\_J4



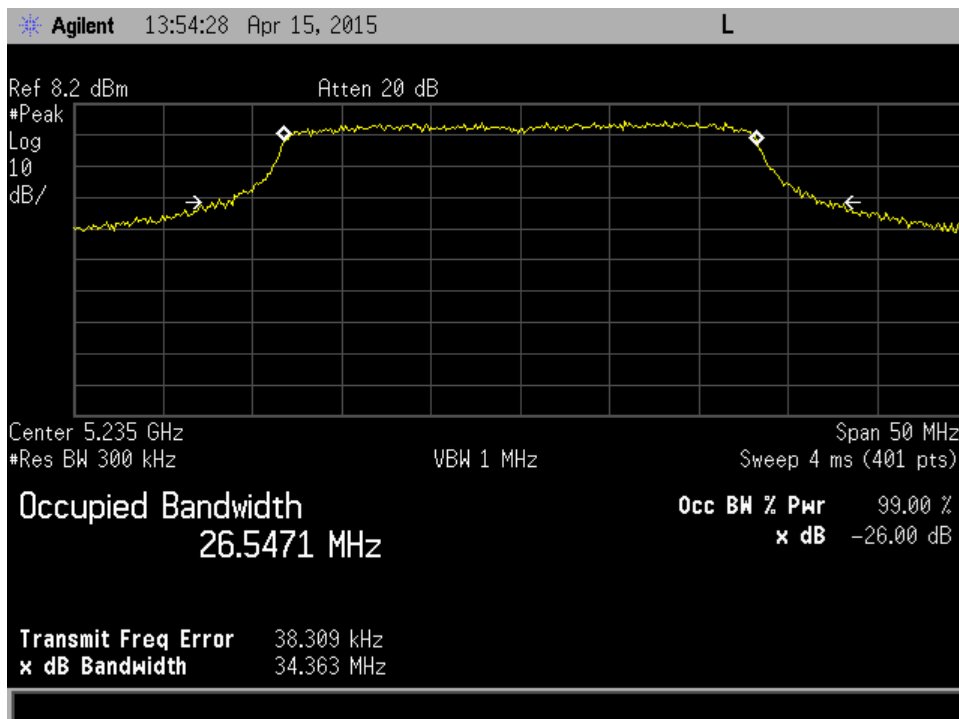
20 MHz mid ch\_OCBW\_J3



20 MHz mid ch\_OCBW\_J4

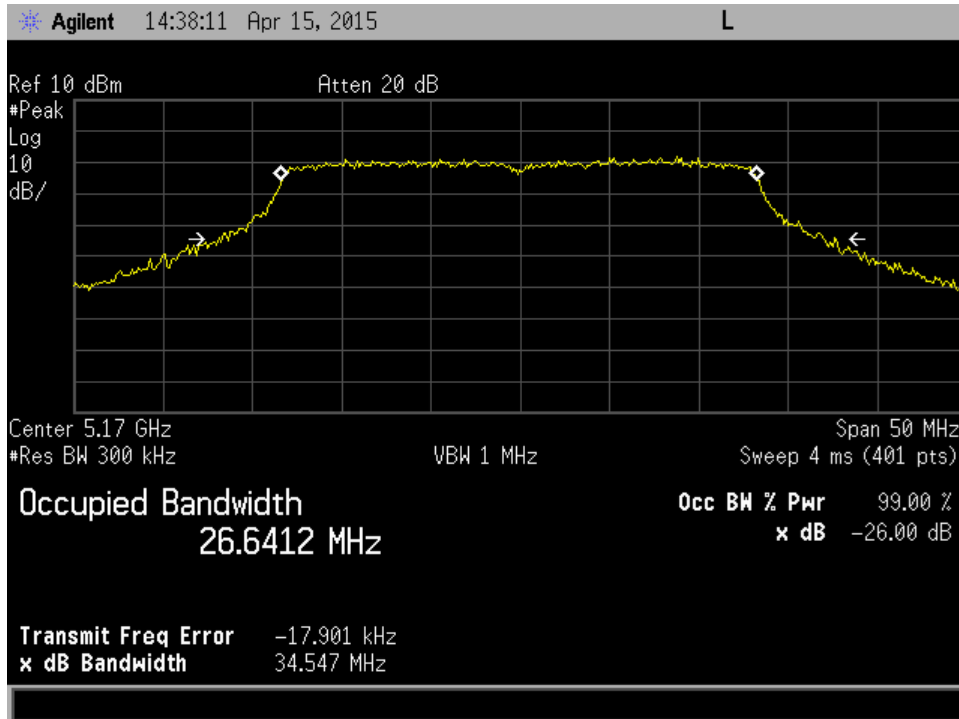


30 MHz high ch\_OCBW\_J3

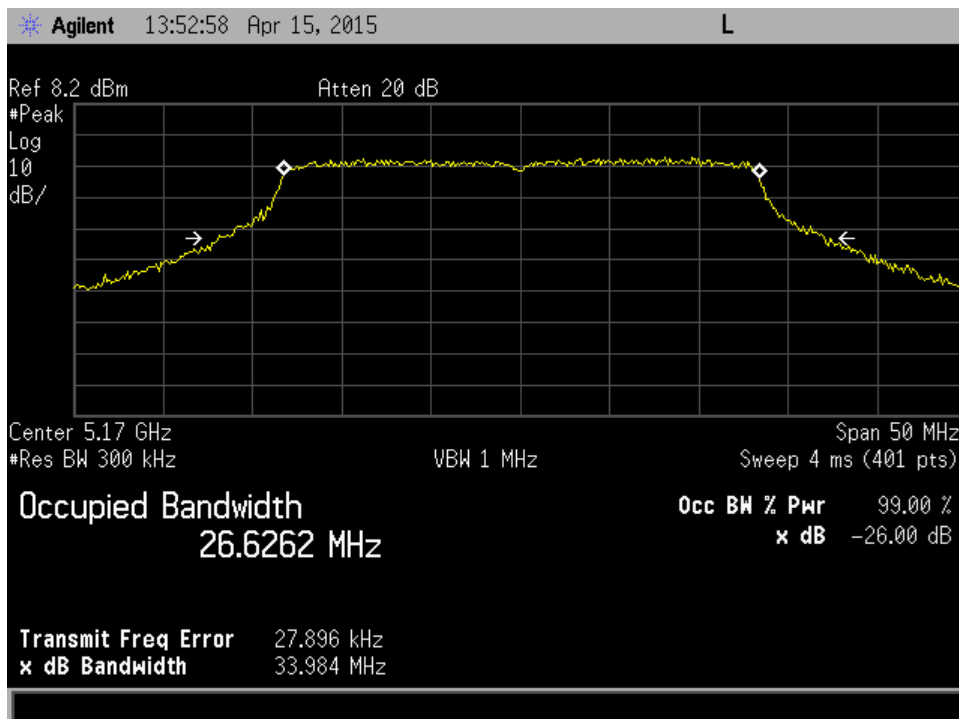


30 MHz high ch\_OCBW\_J4

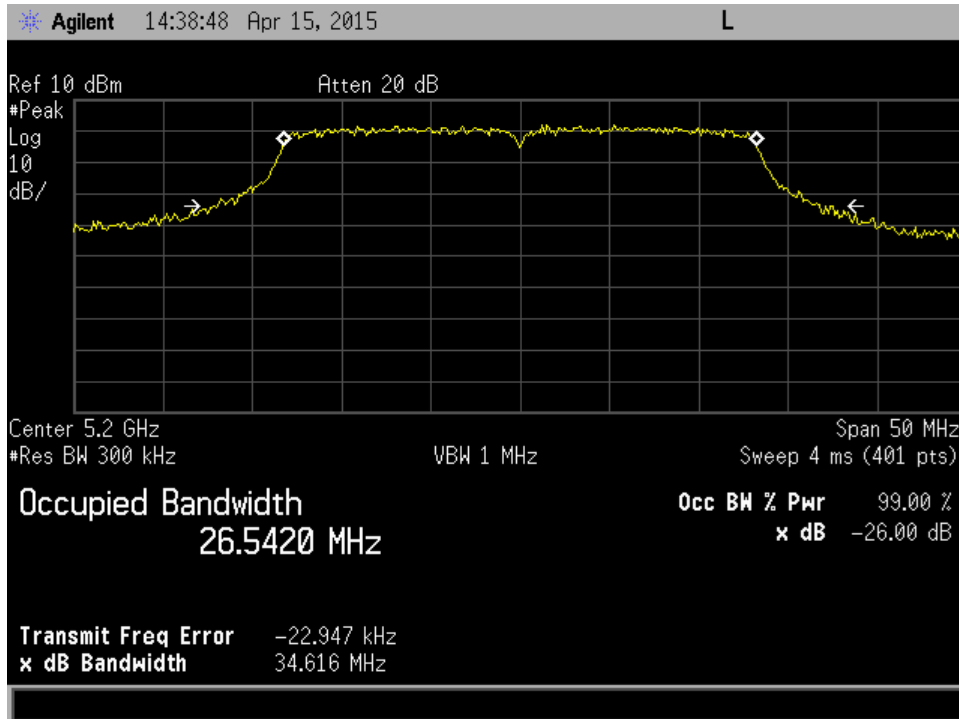




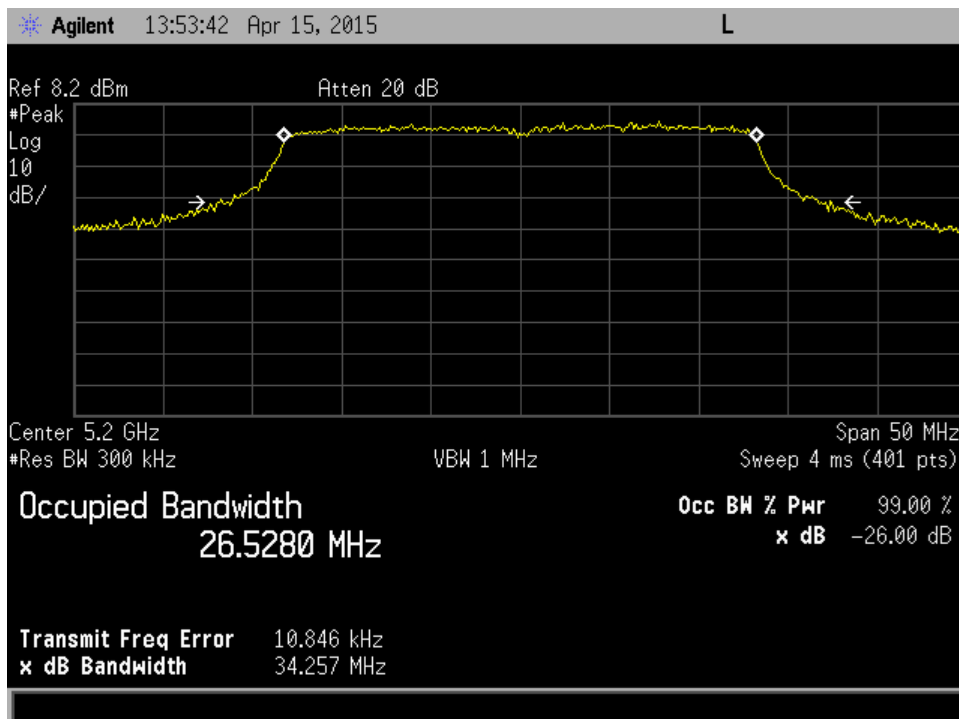
30 MHz low ch\_OCBW\_J3



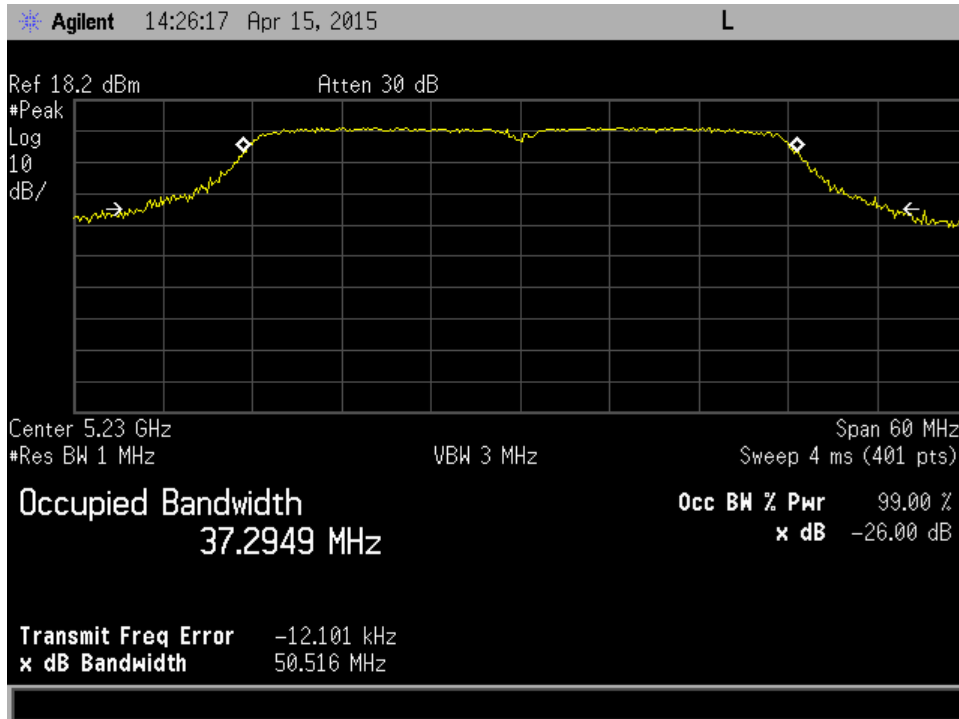
30 MHz low ch\_OCBW\_J4



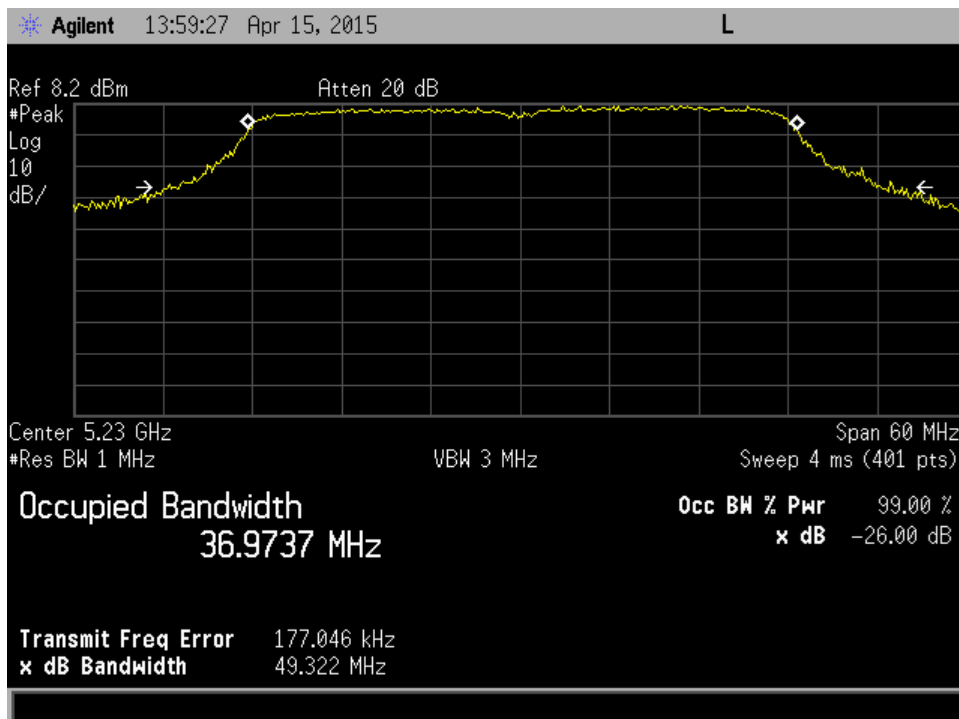
30 MHz mid ch\_OCBW\_J3



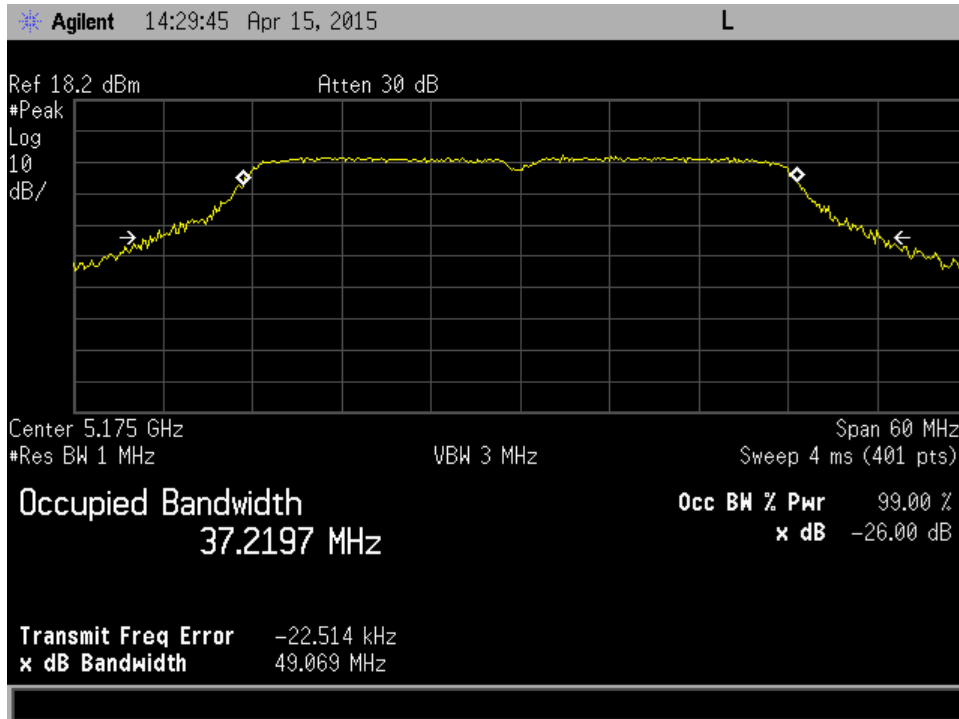
30 MHz mid ch\_OCBW\_J4



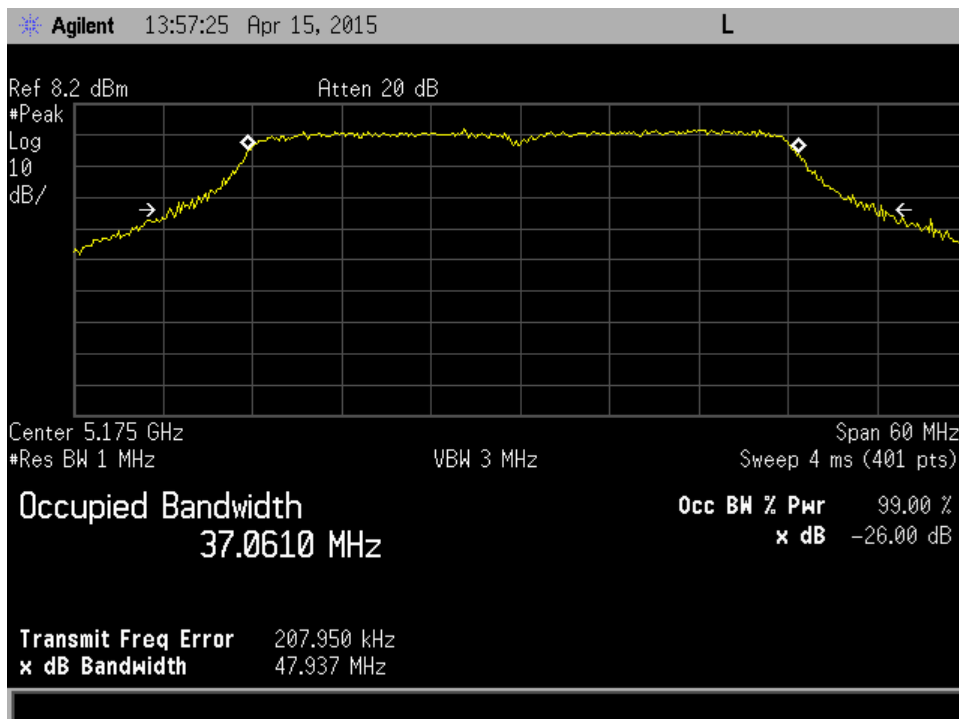
40 MHz high ch\_OCBW\_J3



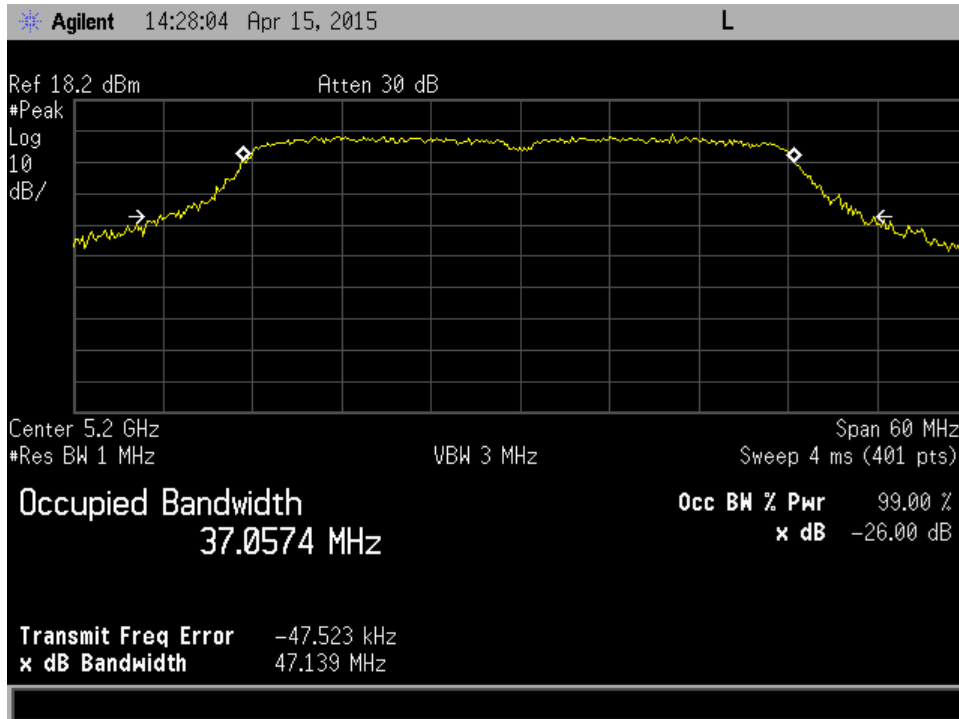
40 MHz high ch\_OCBW\_J4



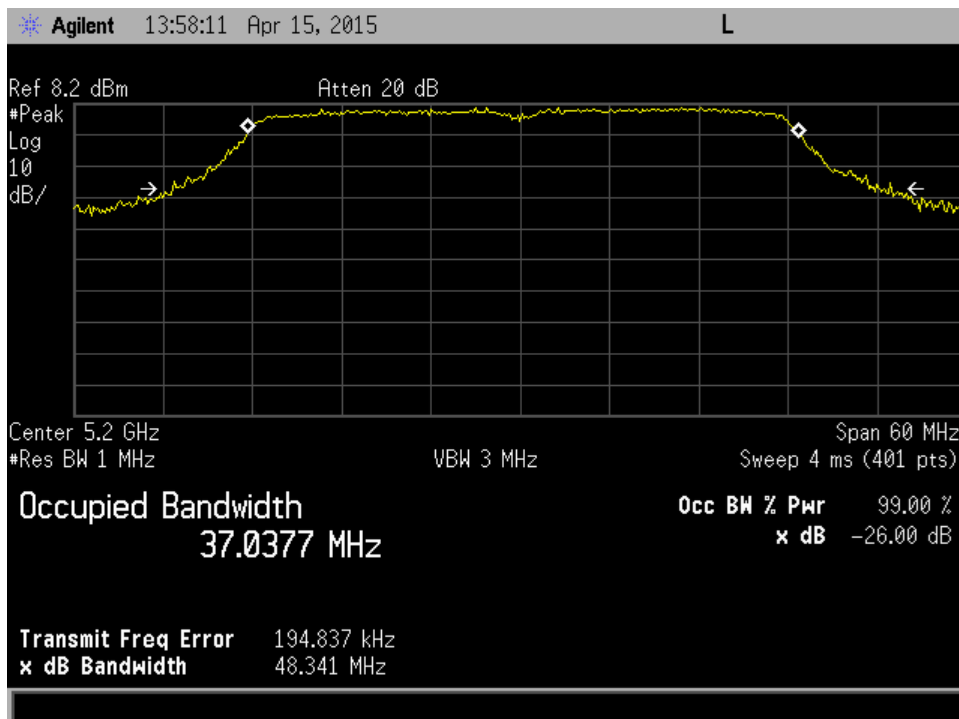
40 MHz low ch\_OCBW\_J3



40 MHz low ch\_OCBW\_J4



40 MHz mid ch\_OCBW\_J3



40 MHz mid ch\_OCBW\_J4