

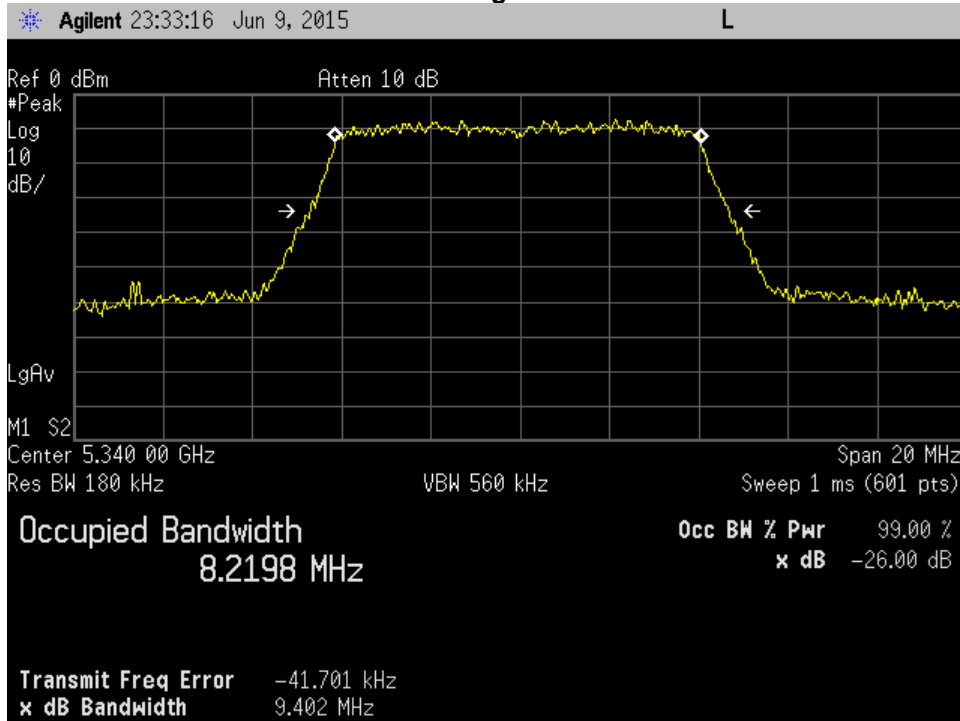


Annex C

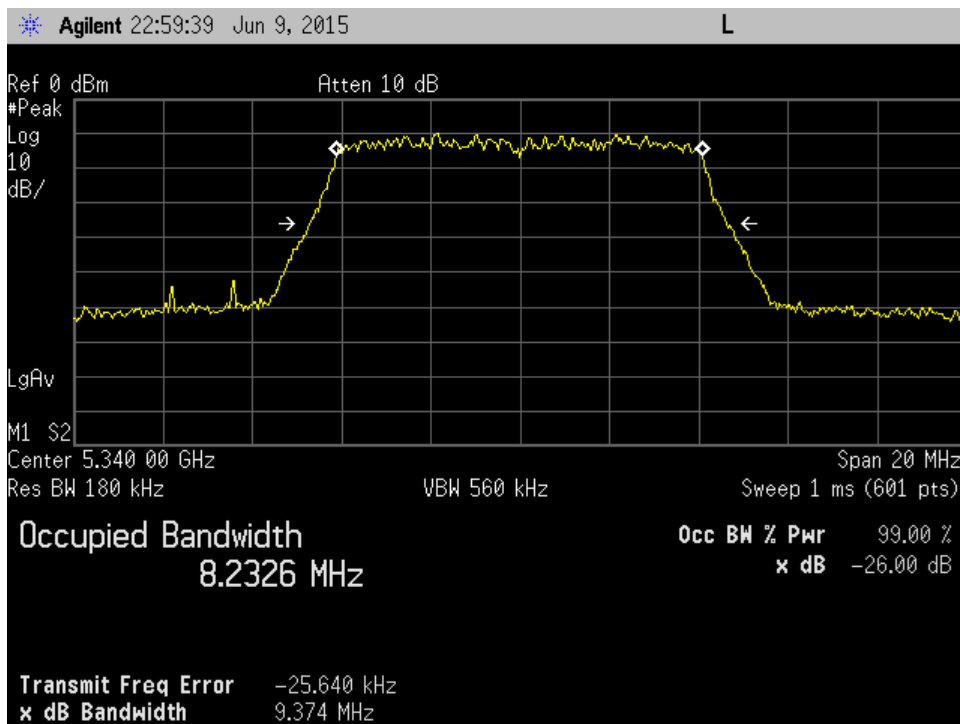
Occupied Bandwidth



10MHz high ch J1

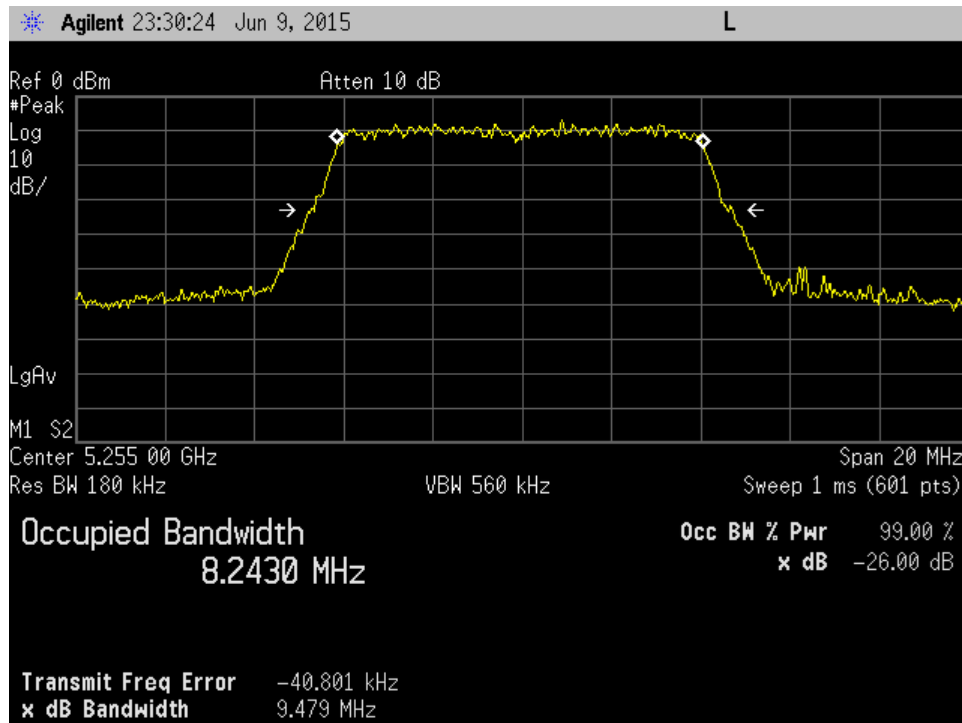


10MHz high ch J3

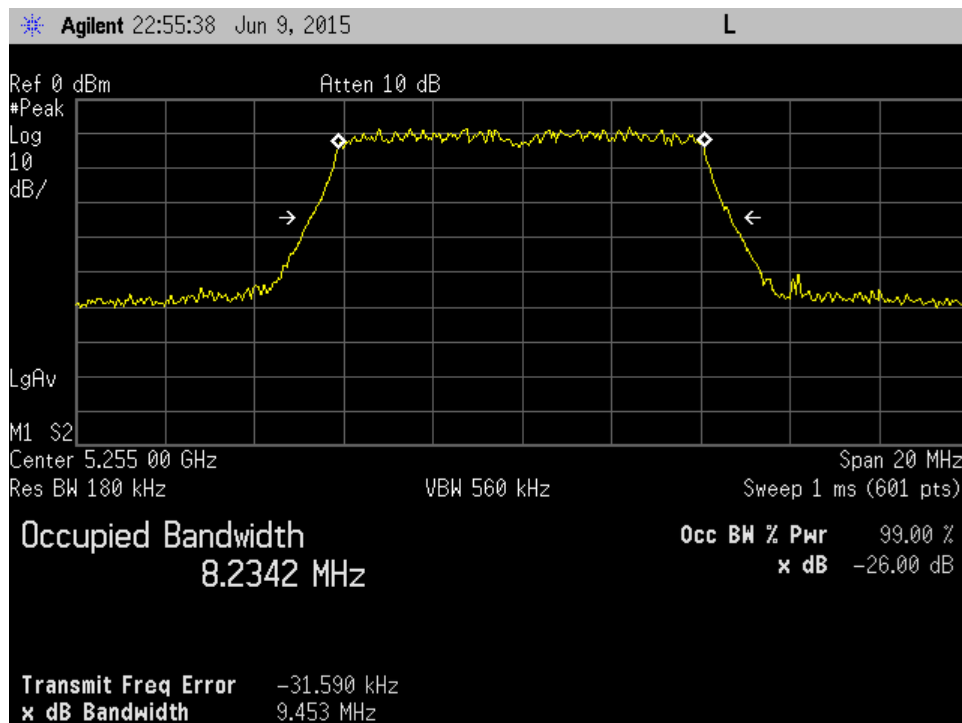




10MHz low ch J1

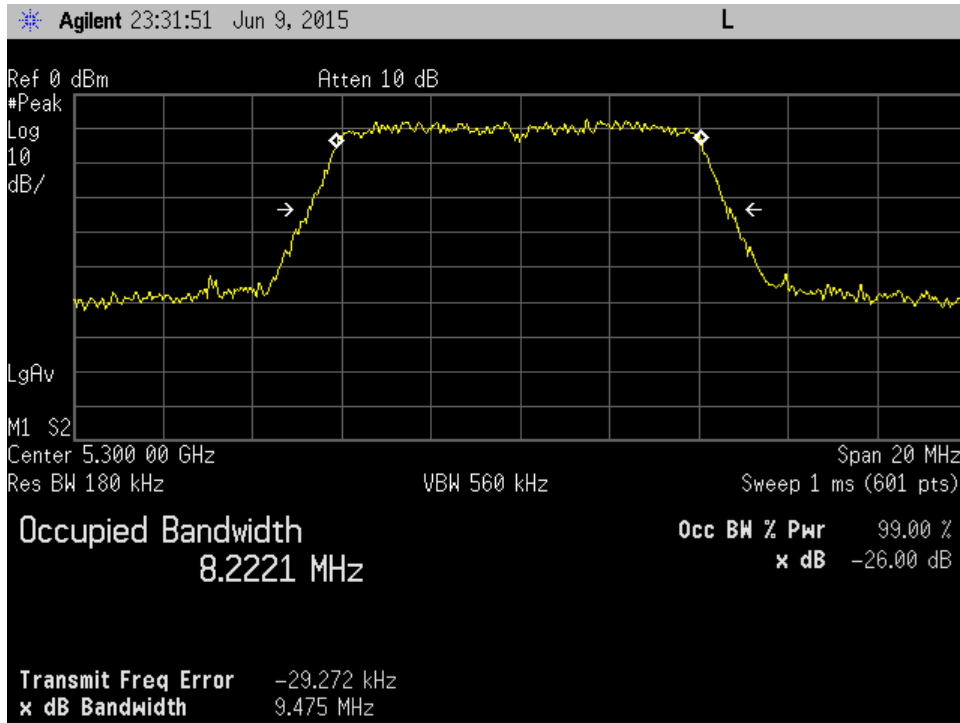


10MHz low ch J3

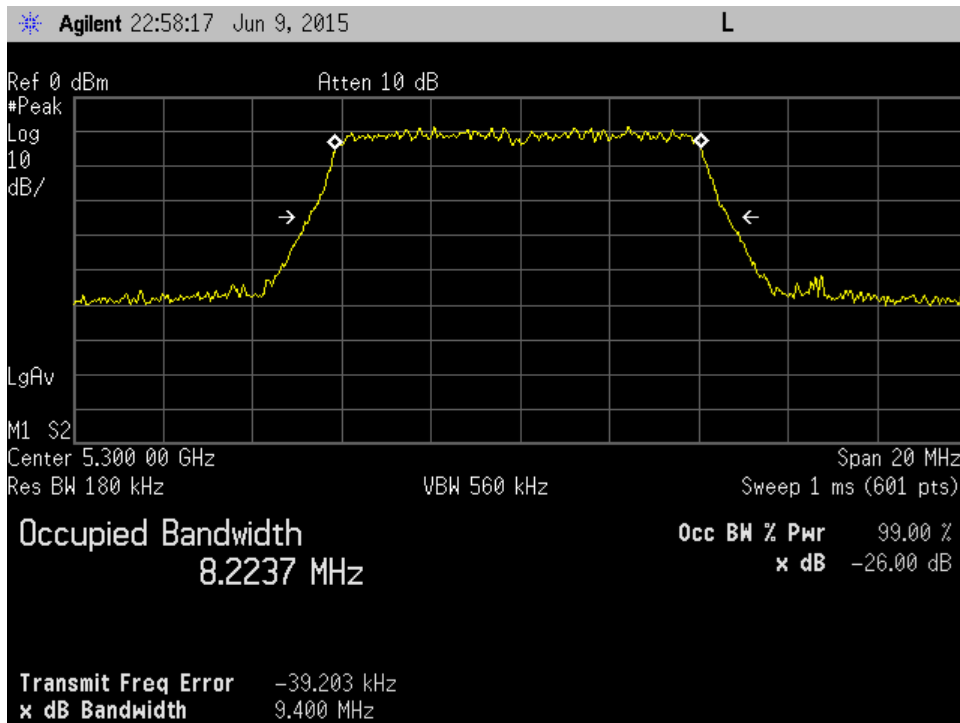




10MHz mid ch J1

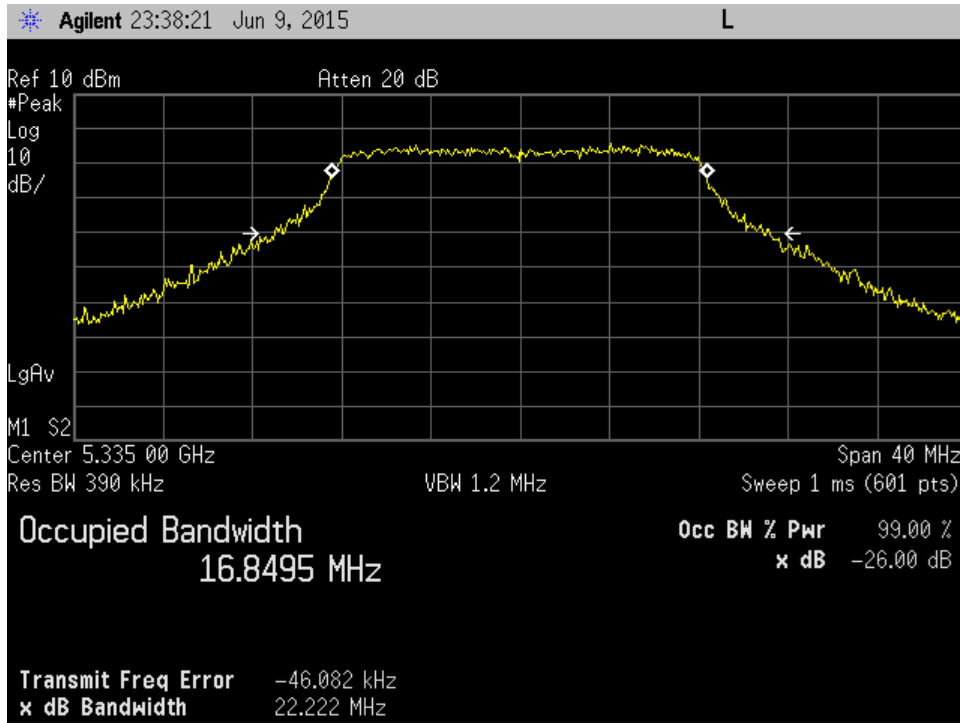


10MHz mid ch J3

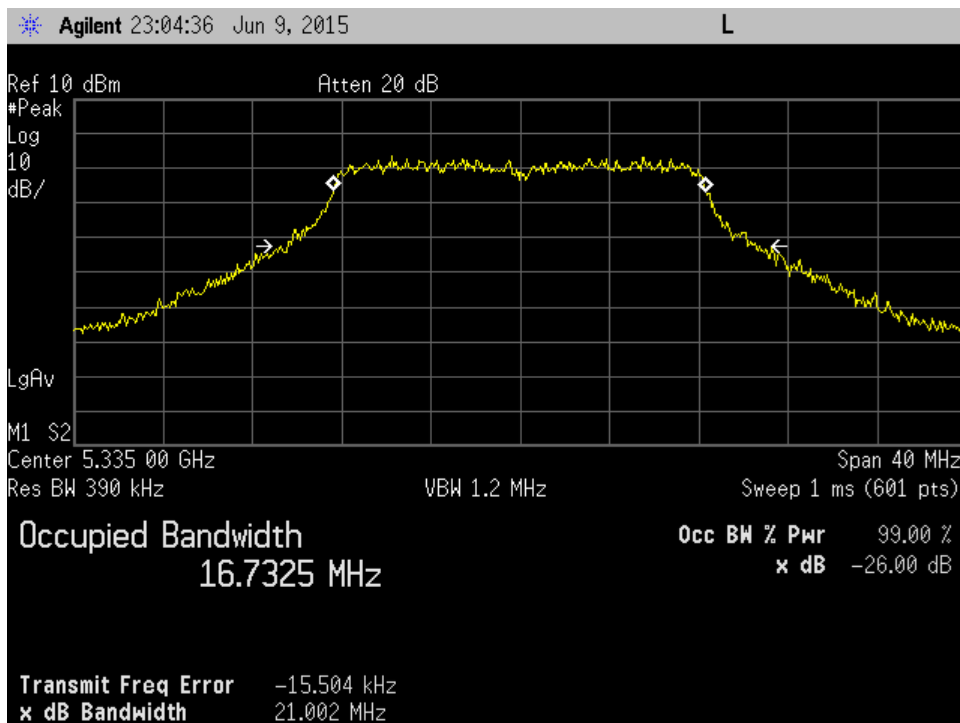




20MHz high ch J1

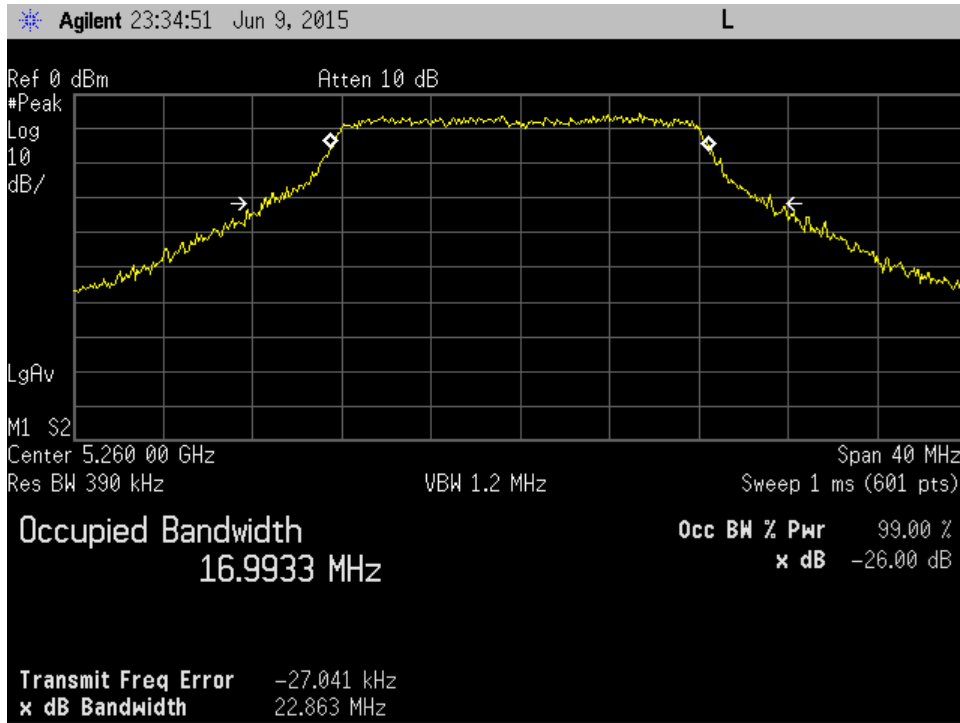


20MHz high ch J3

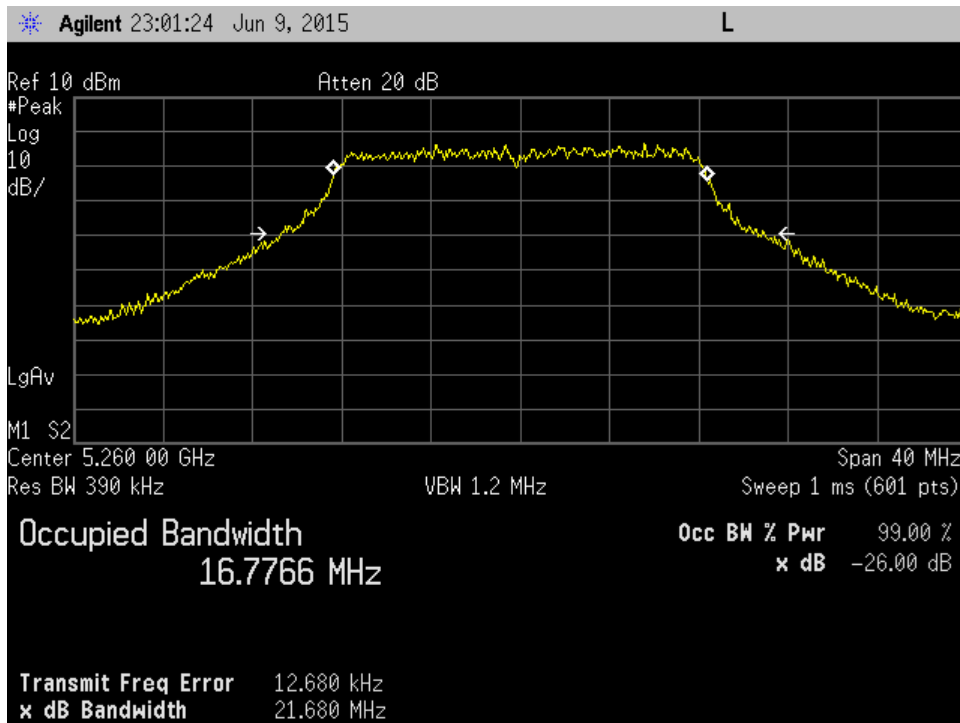




20MHz low ch J1

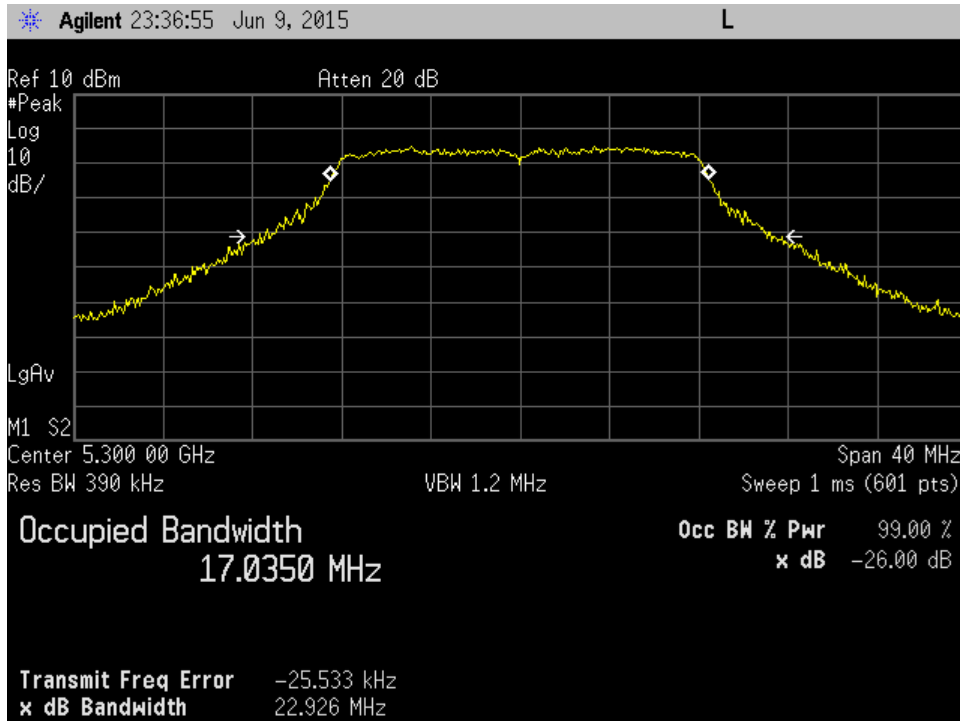


20MHz low ch J3

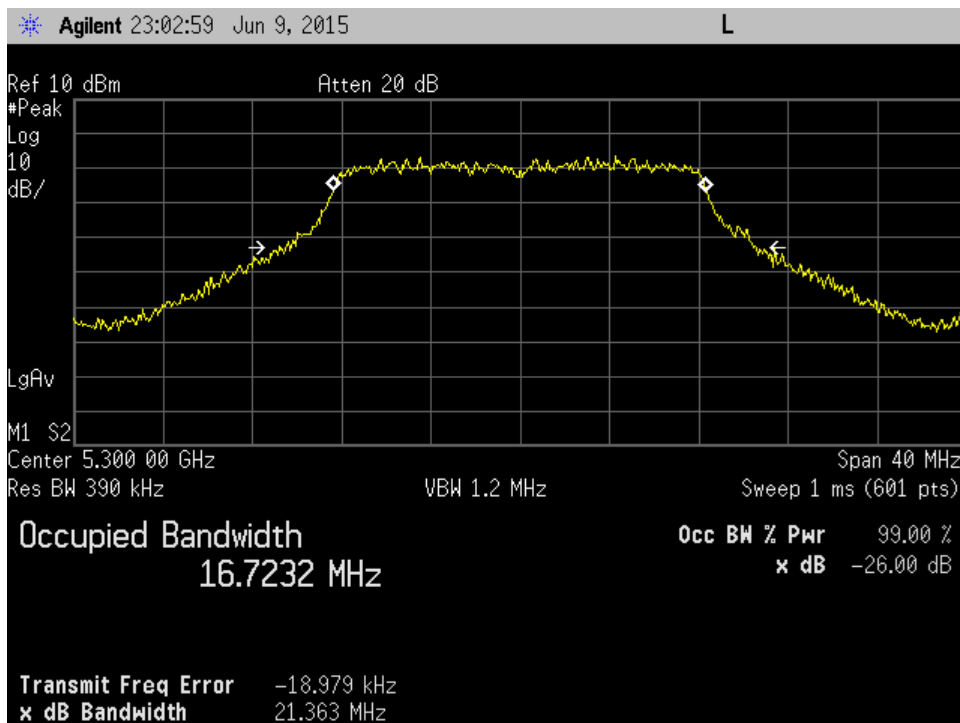




20MHz mid ch J1

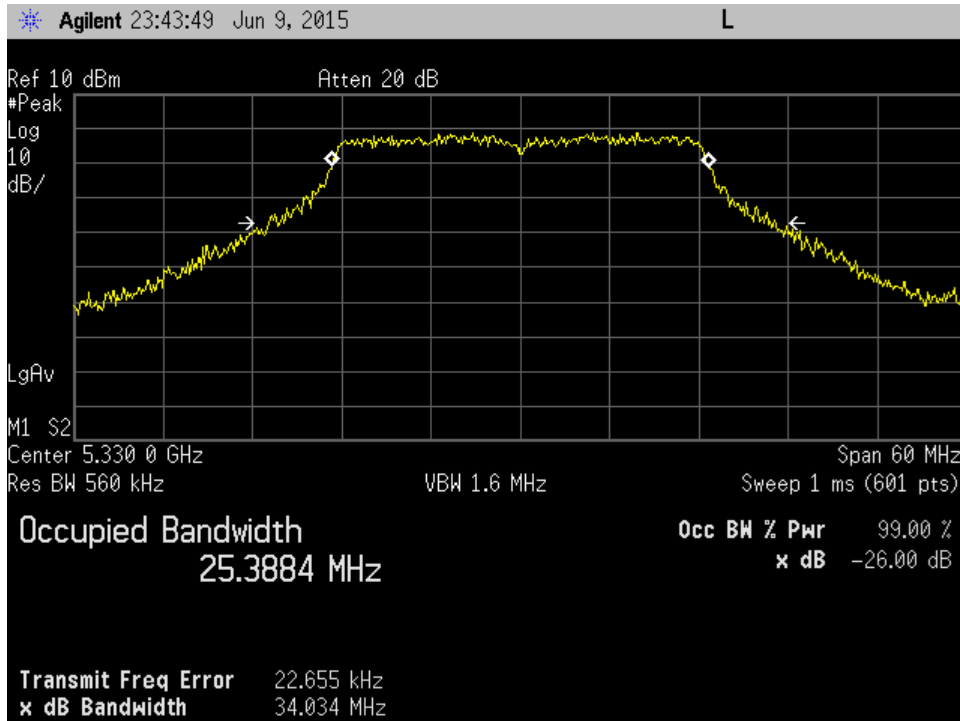


20MHz mid ch J3

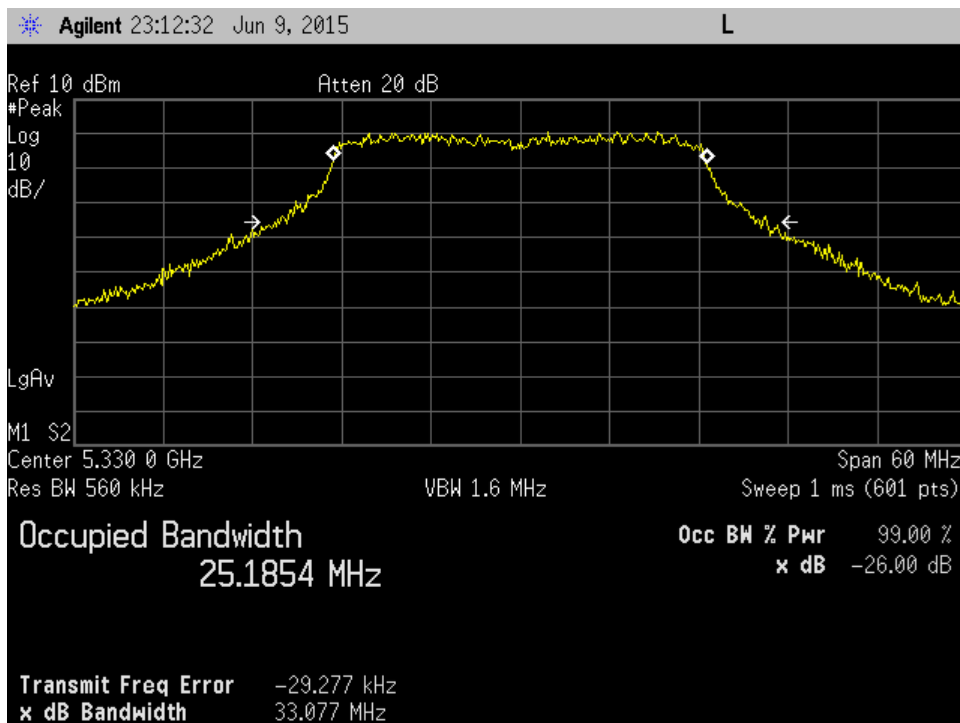




30MHz high ch J1

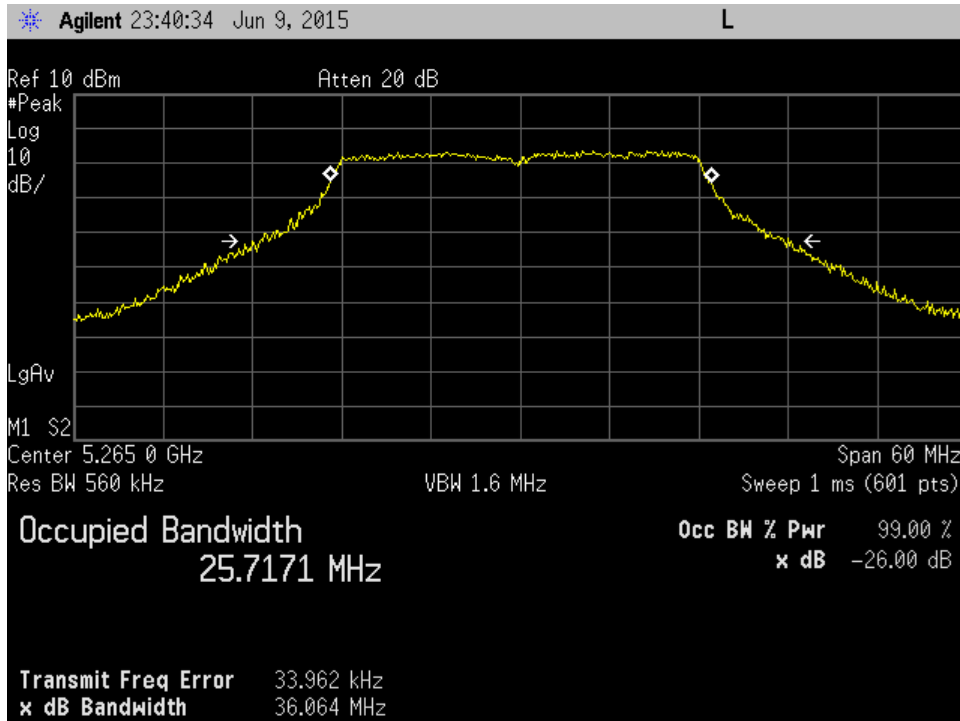


30MHz high ch J3

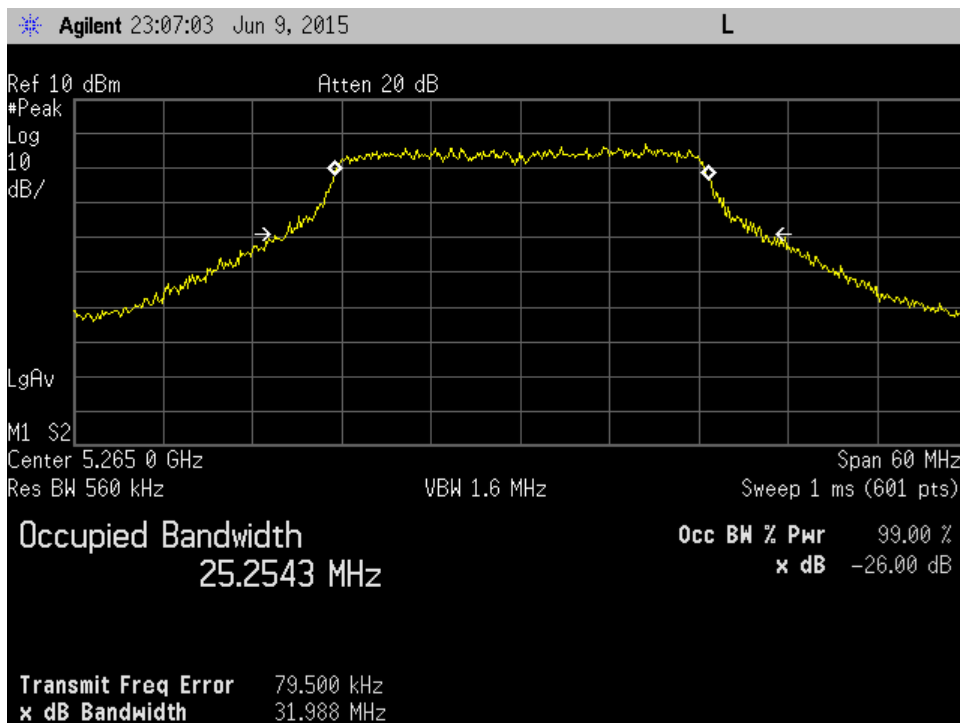




30MHz low ch J1

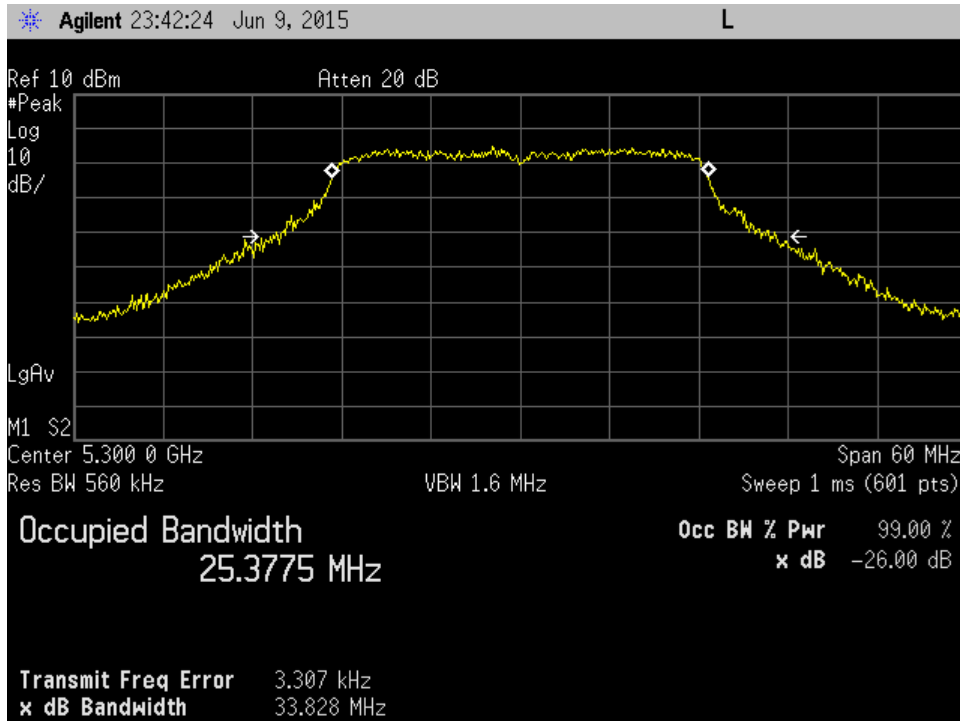


30MHz low ch J3

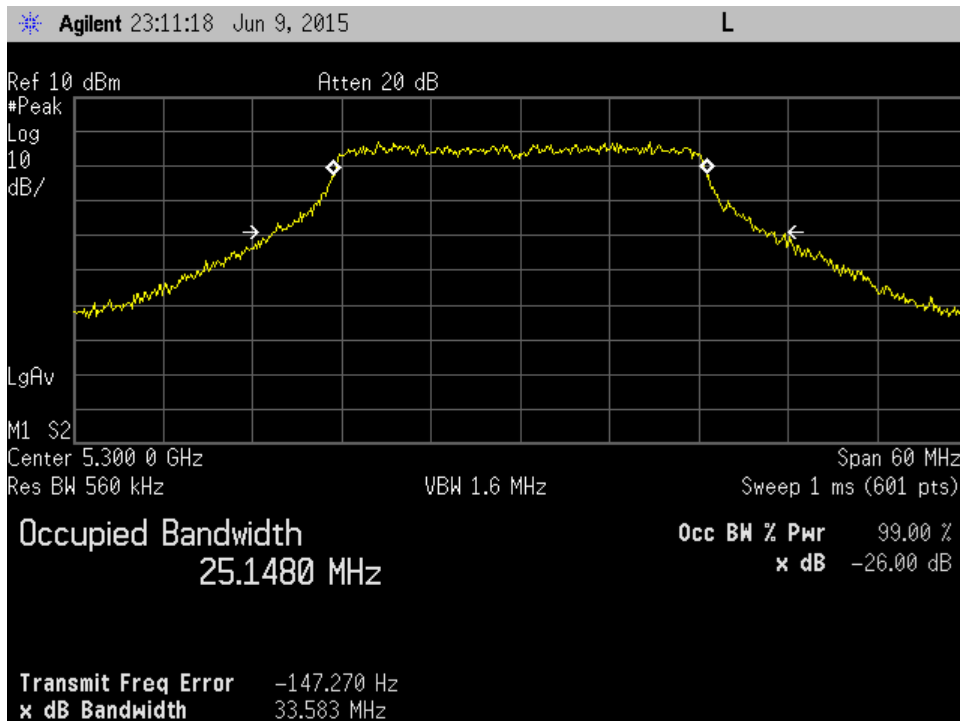




30MHz mid ch J1

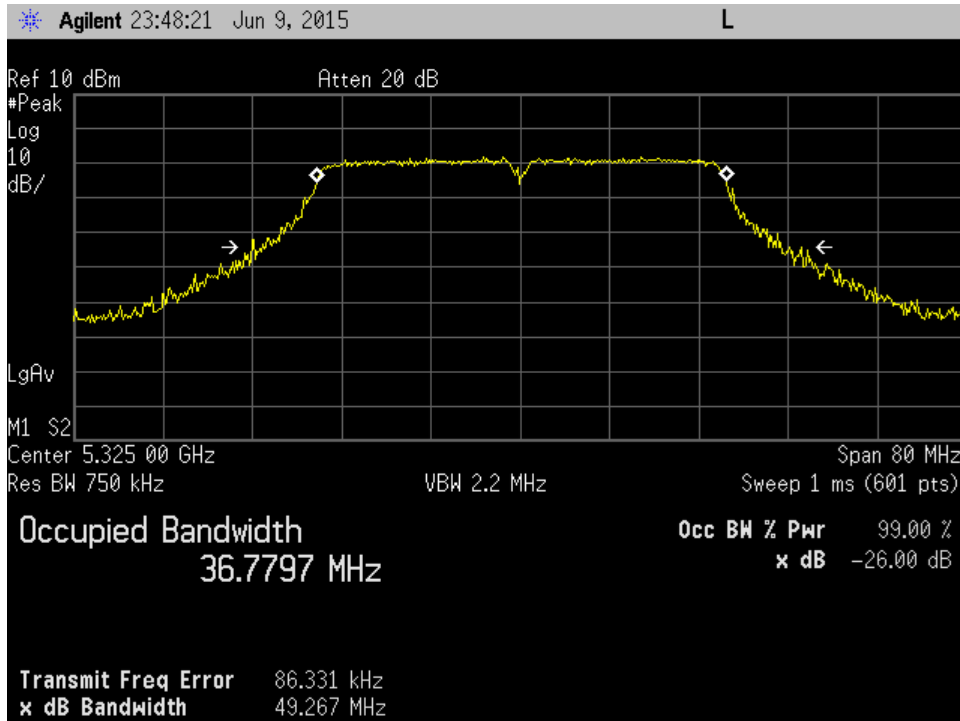


30MHz mid ch J3

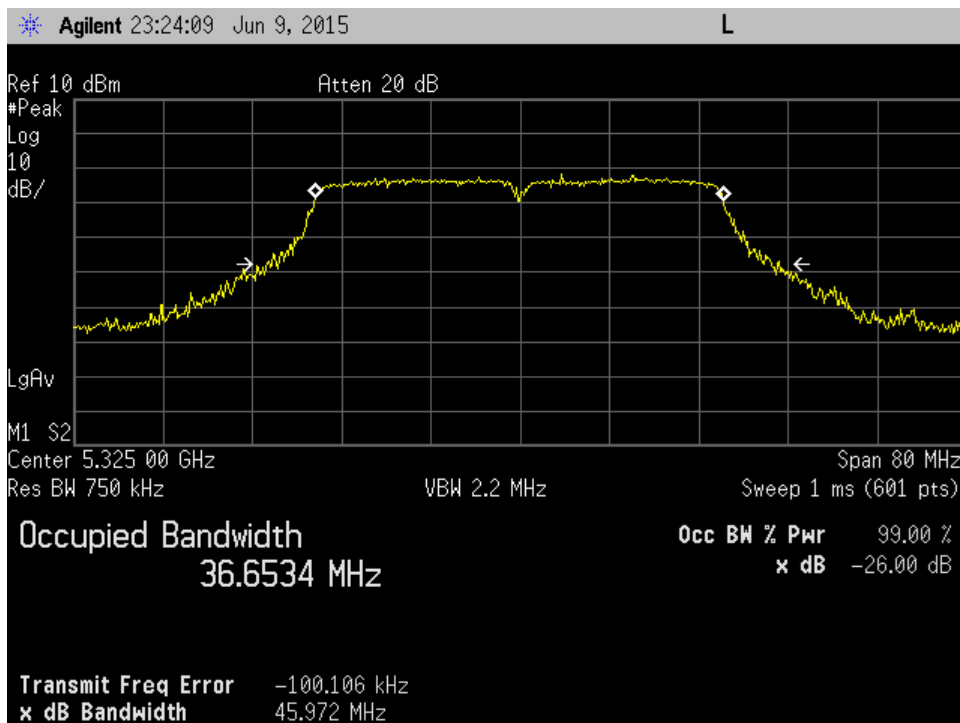




40MHz high ch J1

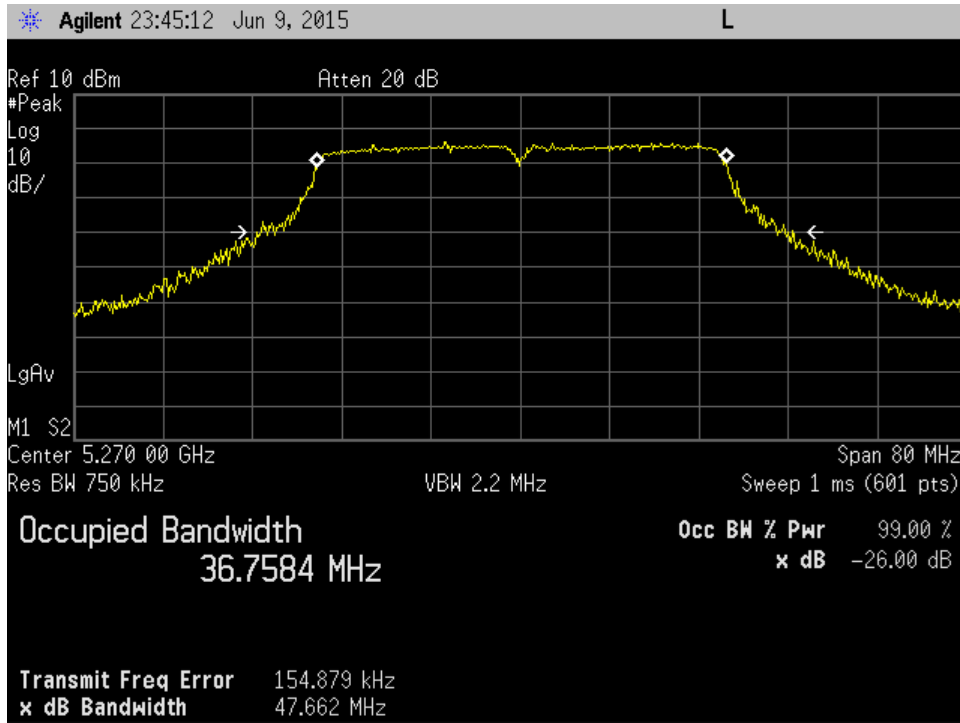


40MHz high ch J3

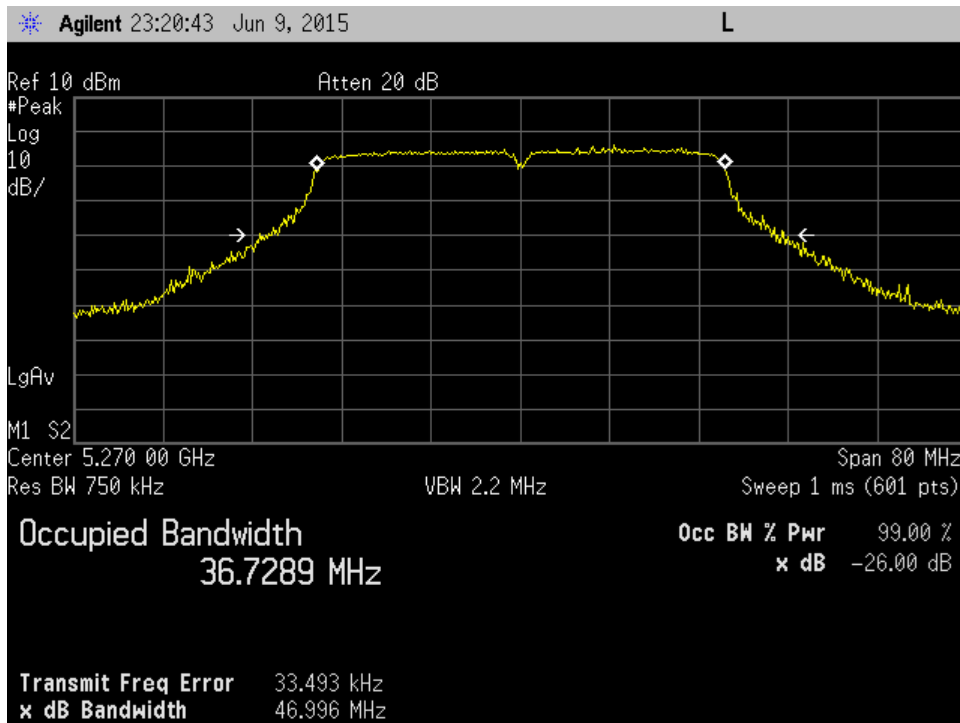




40MHz low ch J1

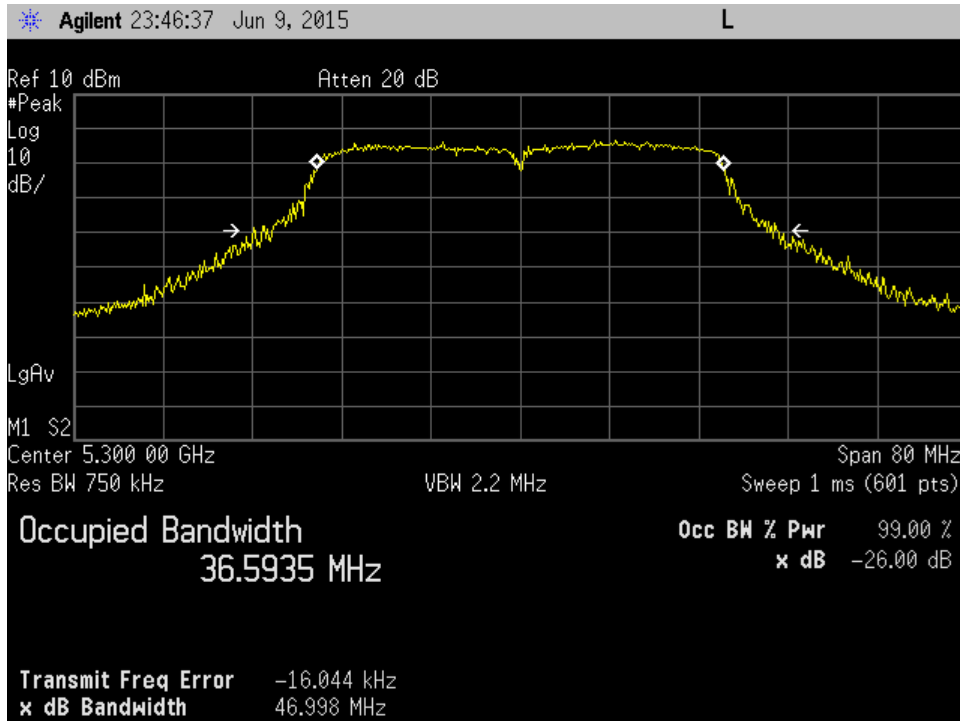


40MHz low ch J3

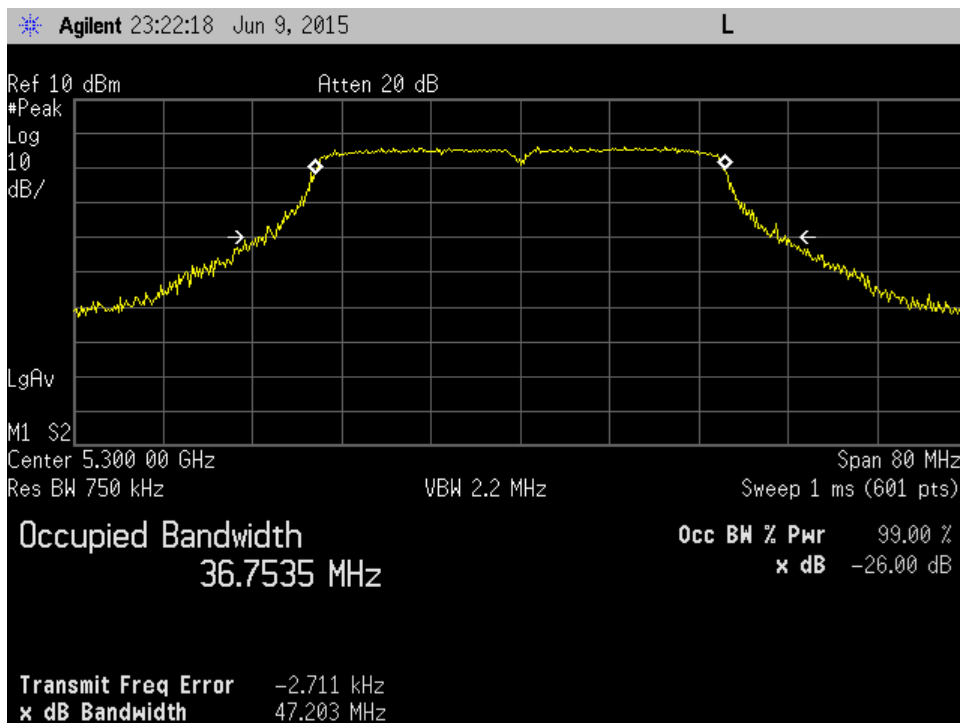




40MHz mid ch J1

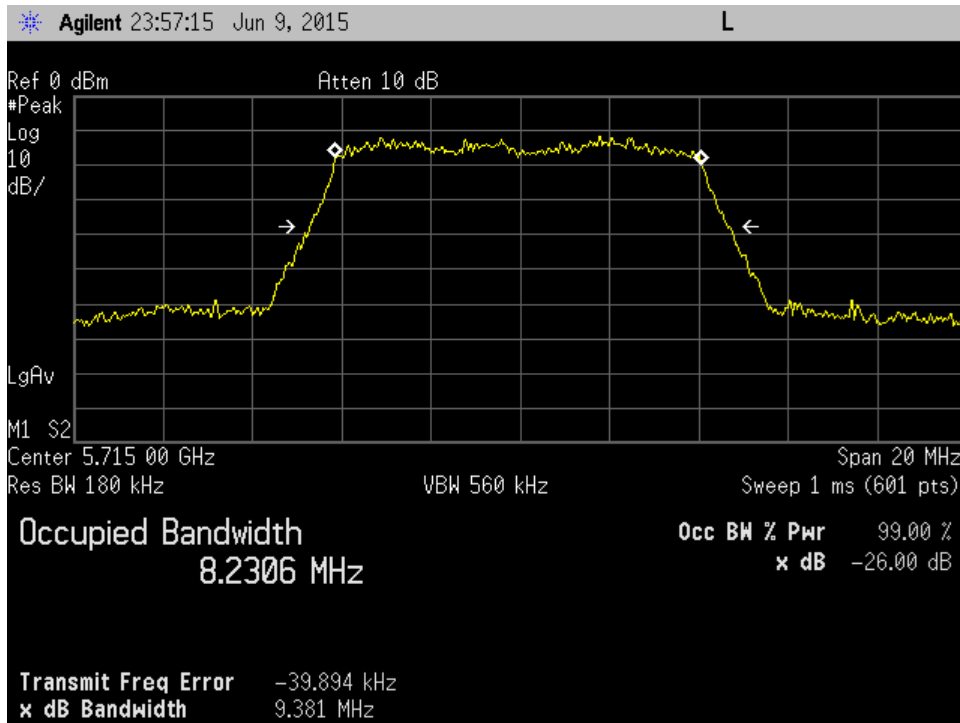


40MHz mid ch J3

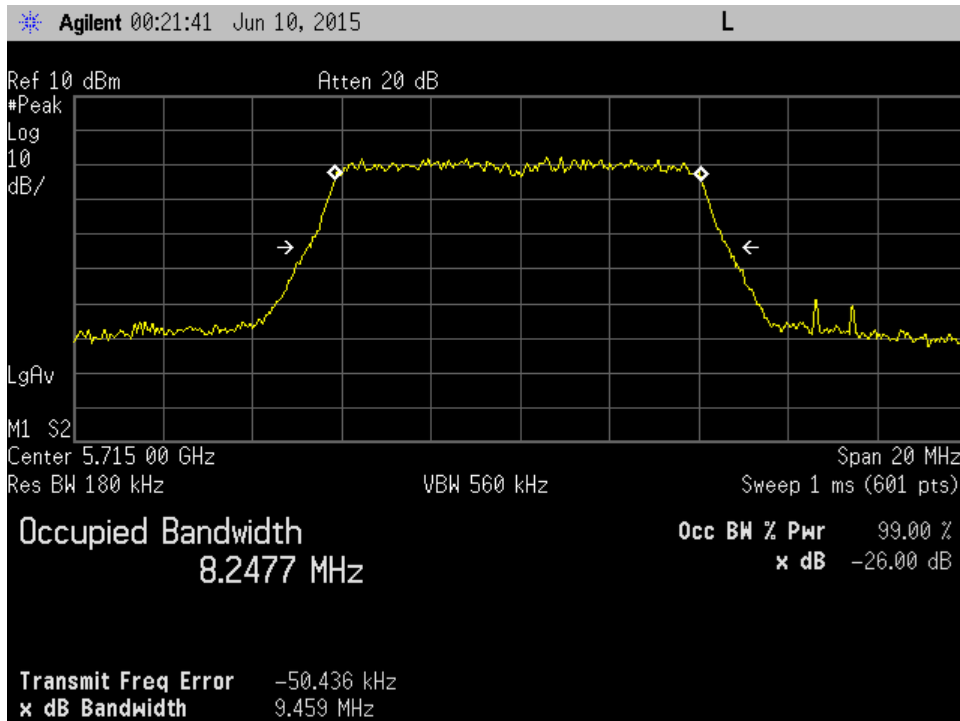




10MHz high ch J1

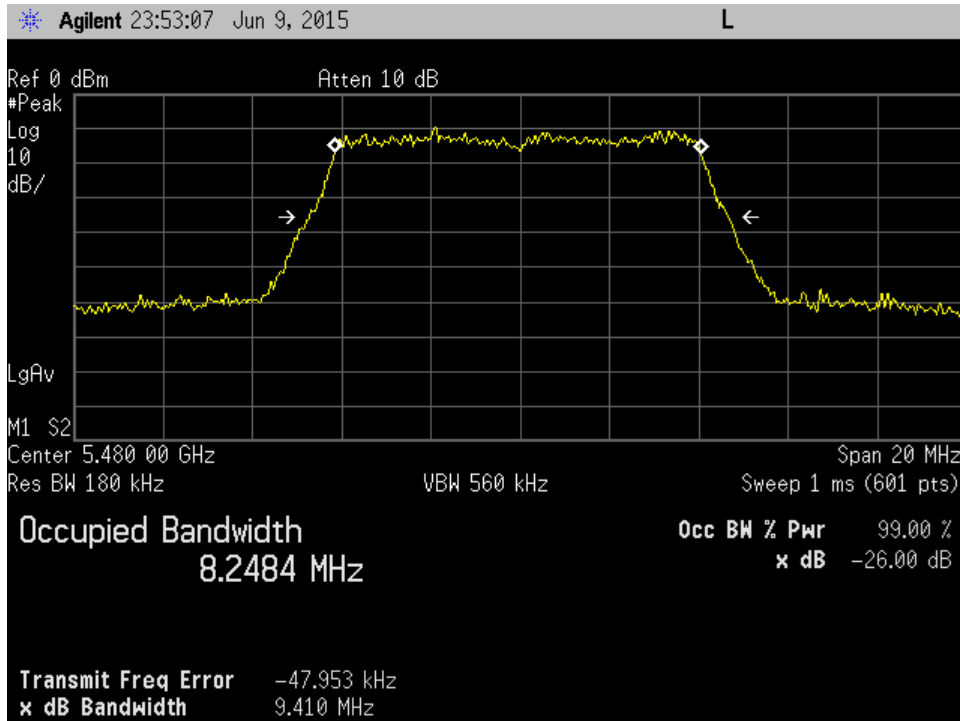


10MHz high ch J3

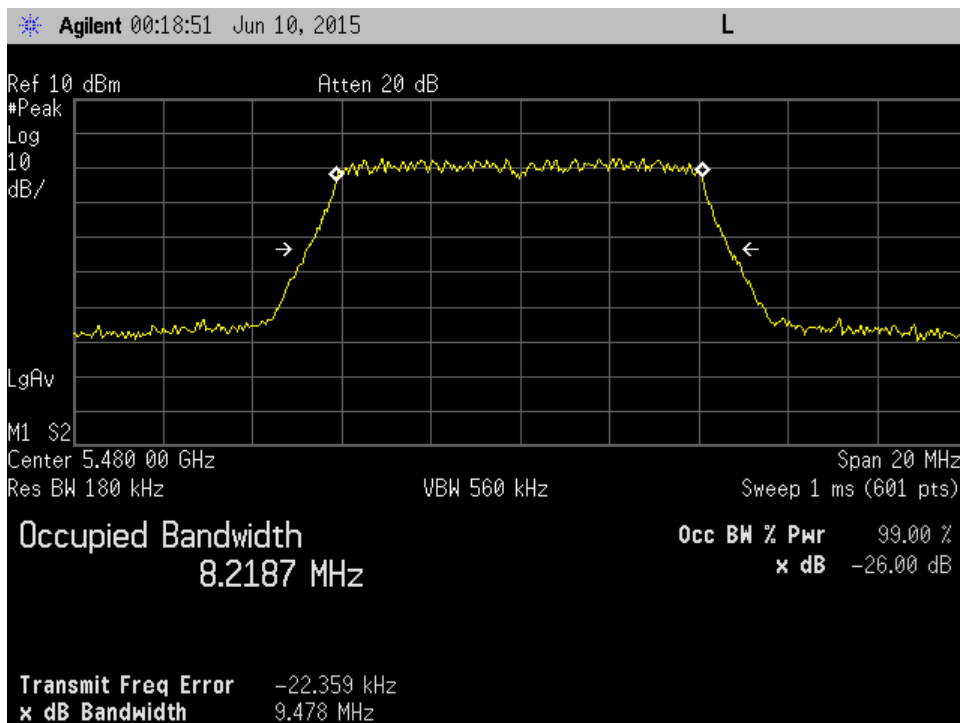




10MHz low ch J1

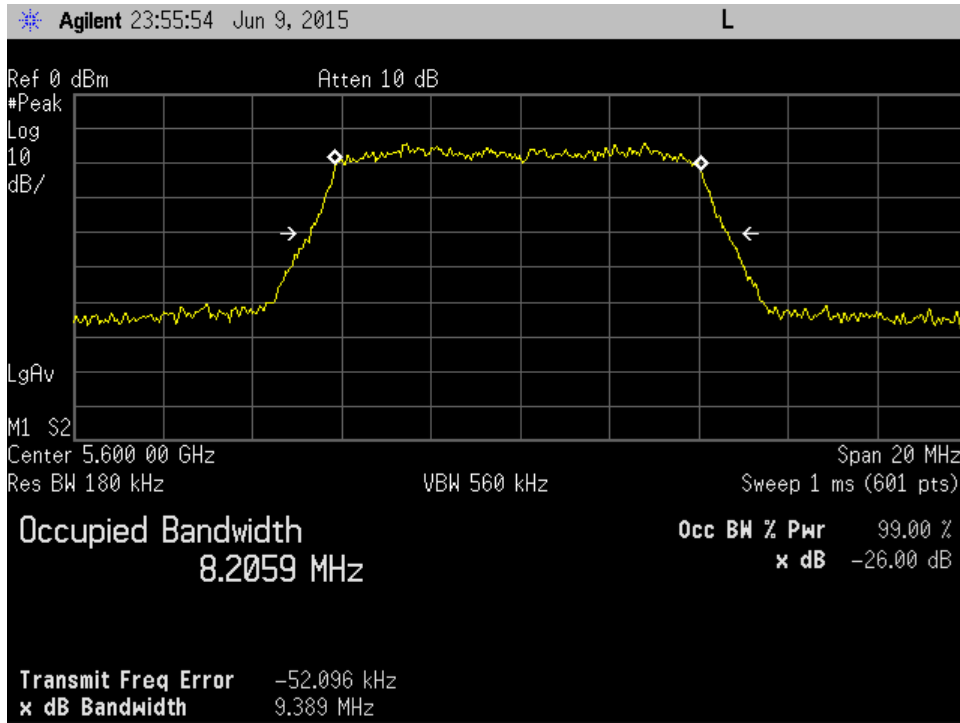


10MHz low ch J3

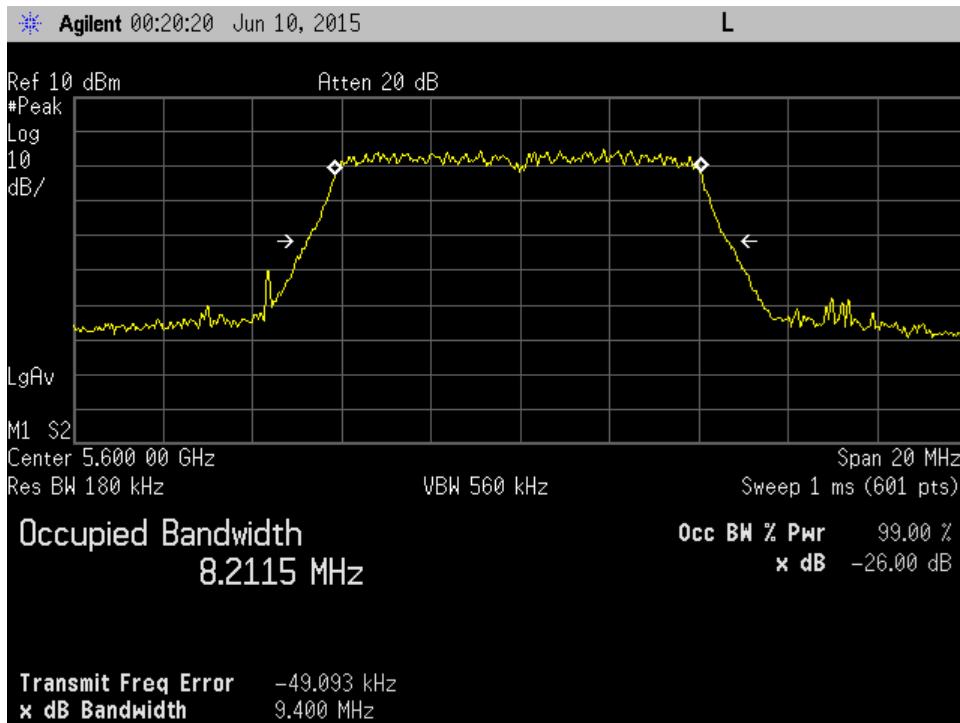




10MHz mid ch J1

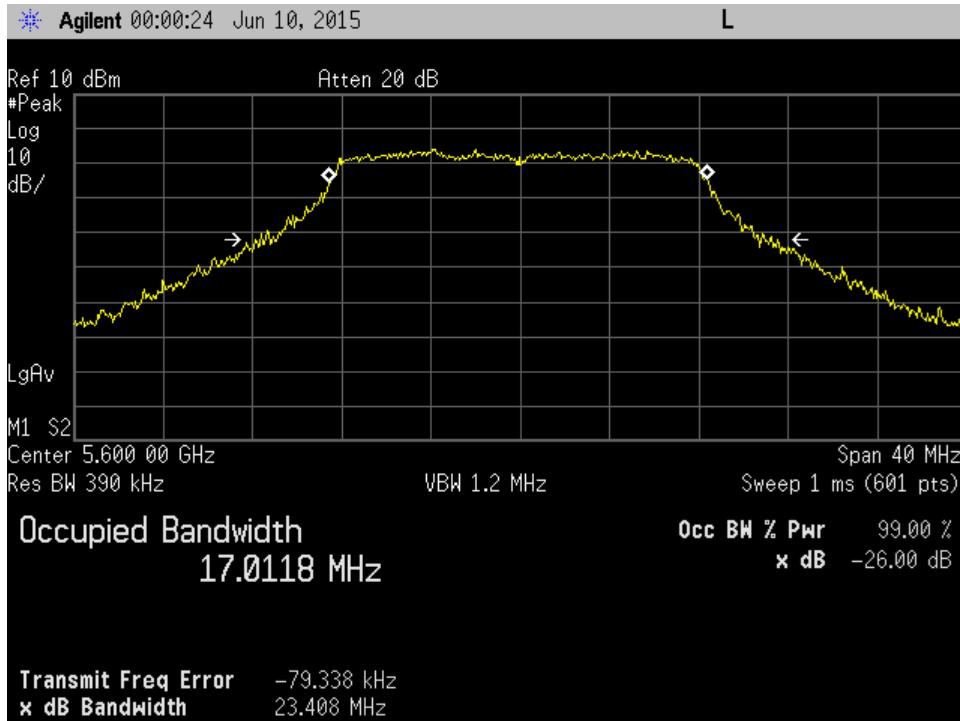


10MHz mid ch J3

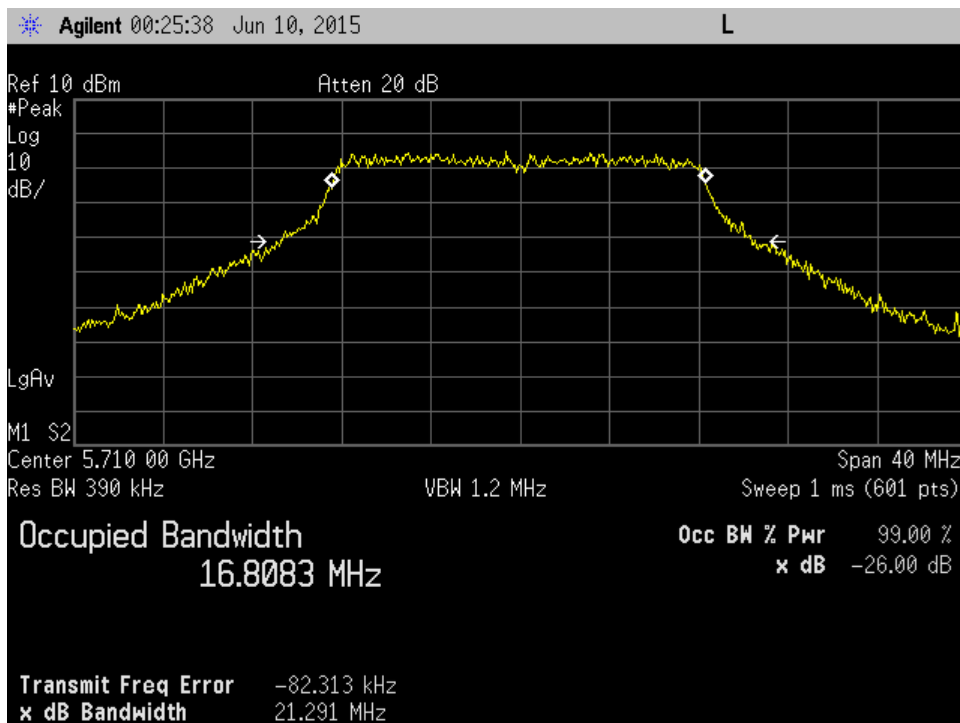




20MHz high ch J1

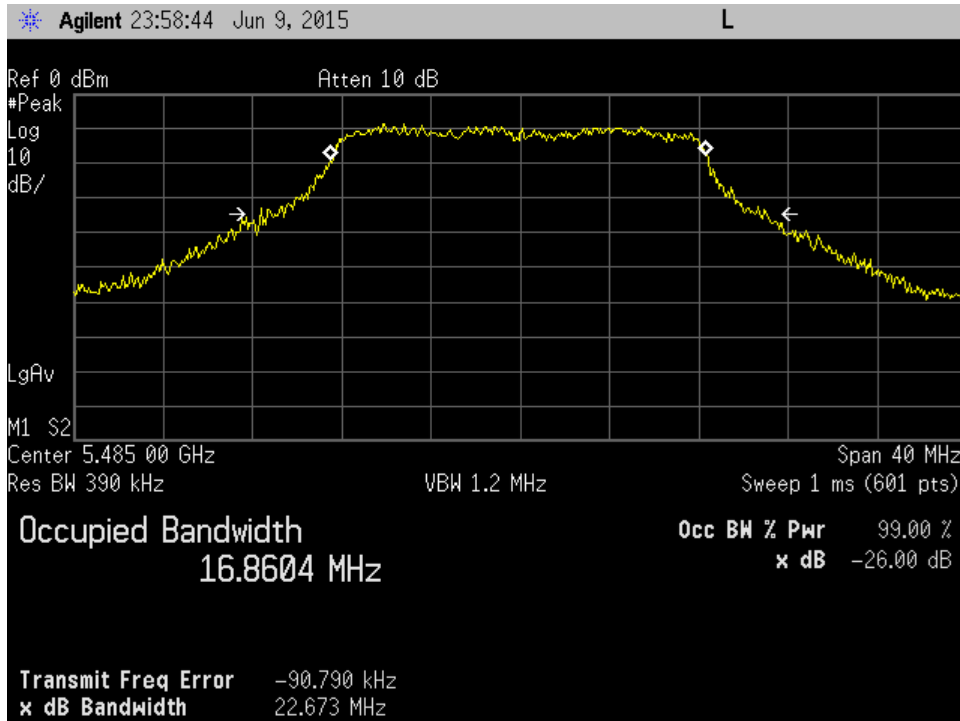


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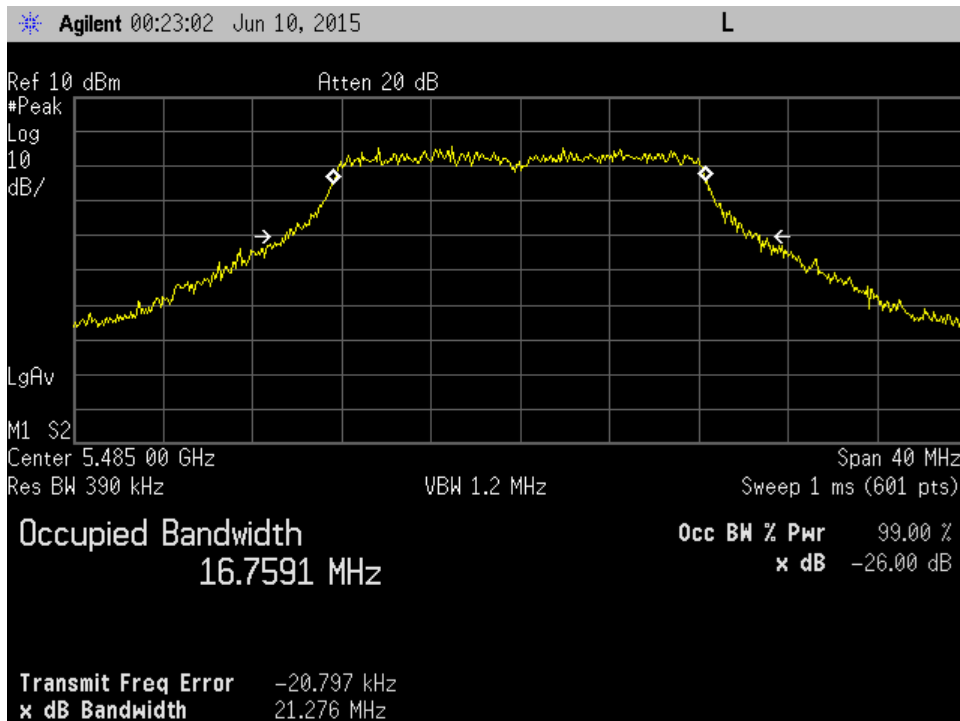




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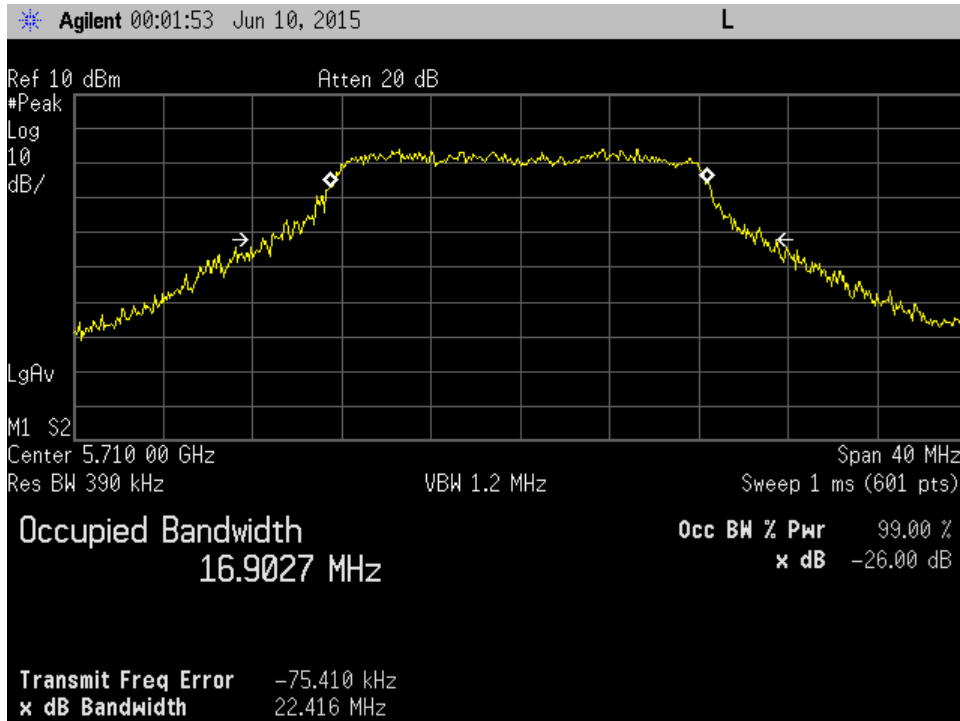


20MHz low ch J3

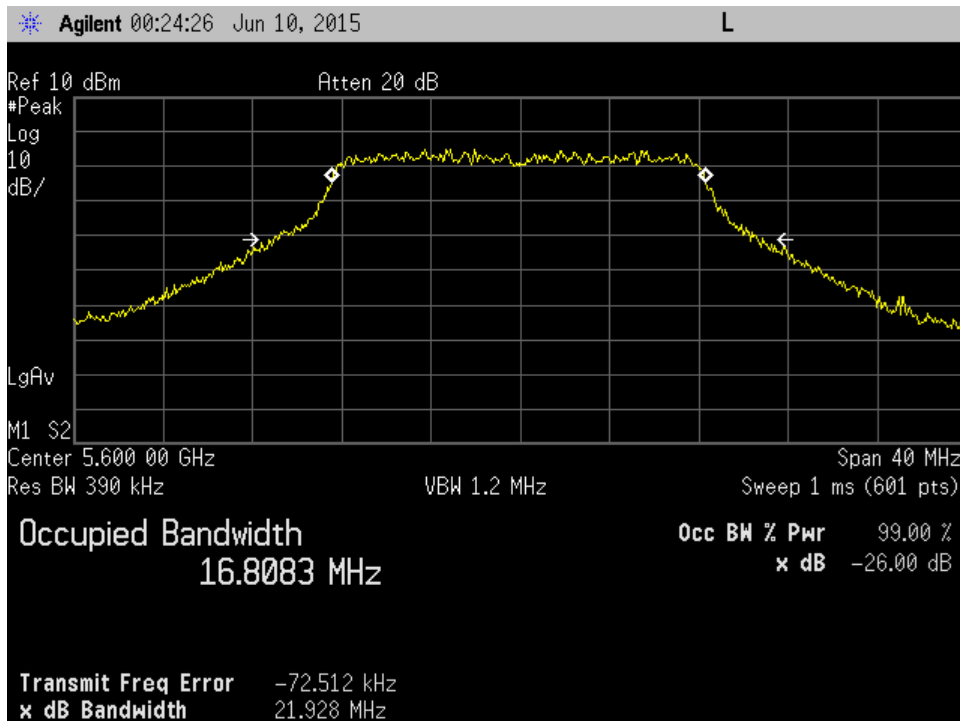




20MHz mid ch J1

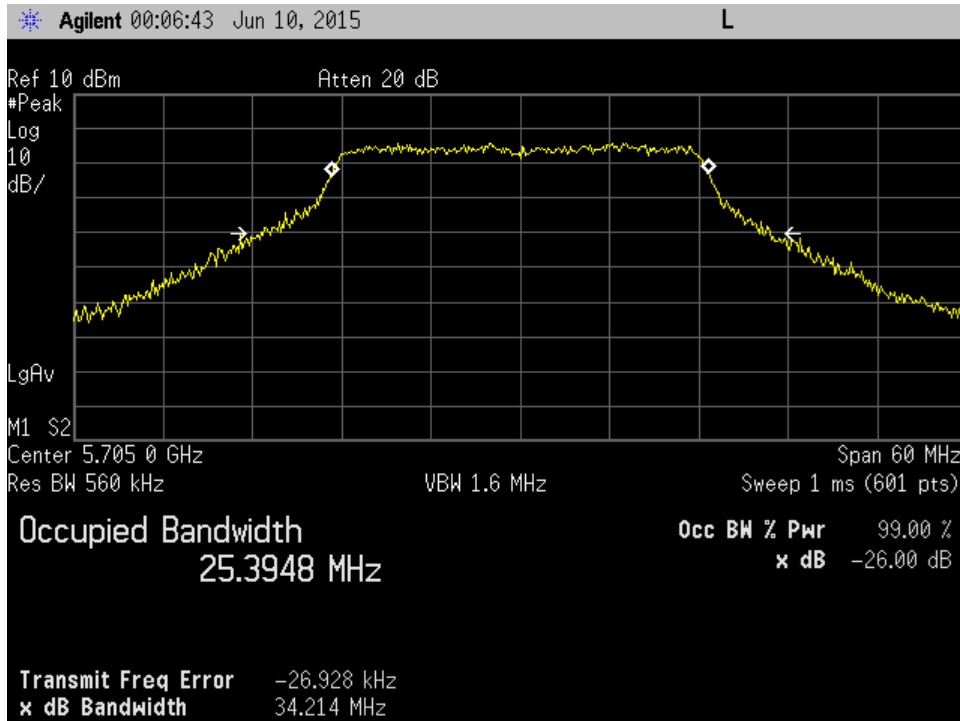


20MHz mid ch J3

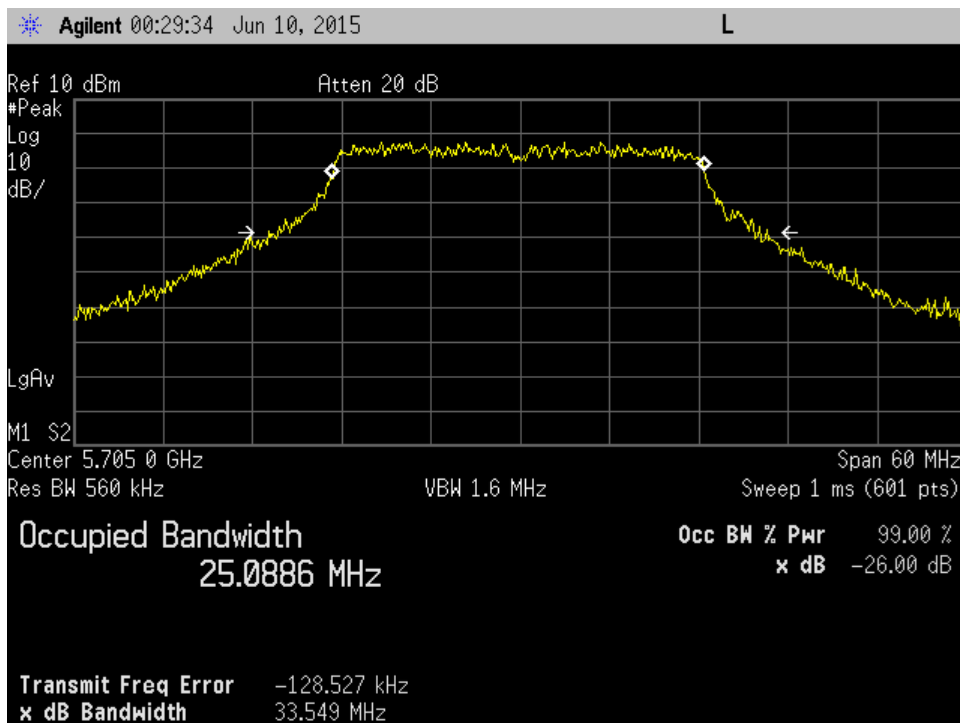




30MHz high ch J1

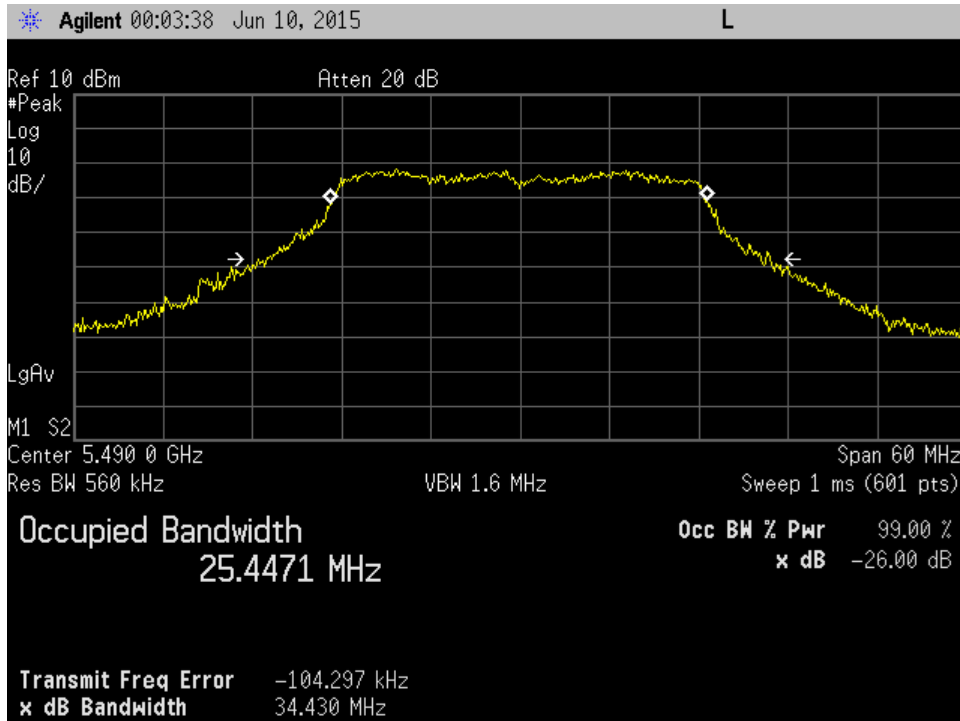


30MHz high ch J3

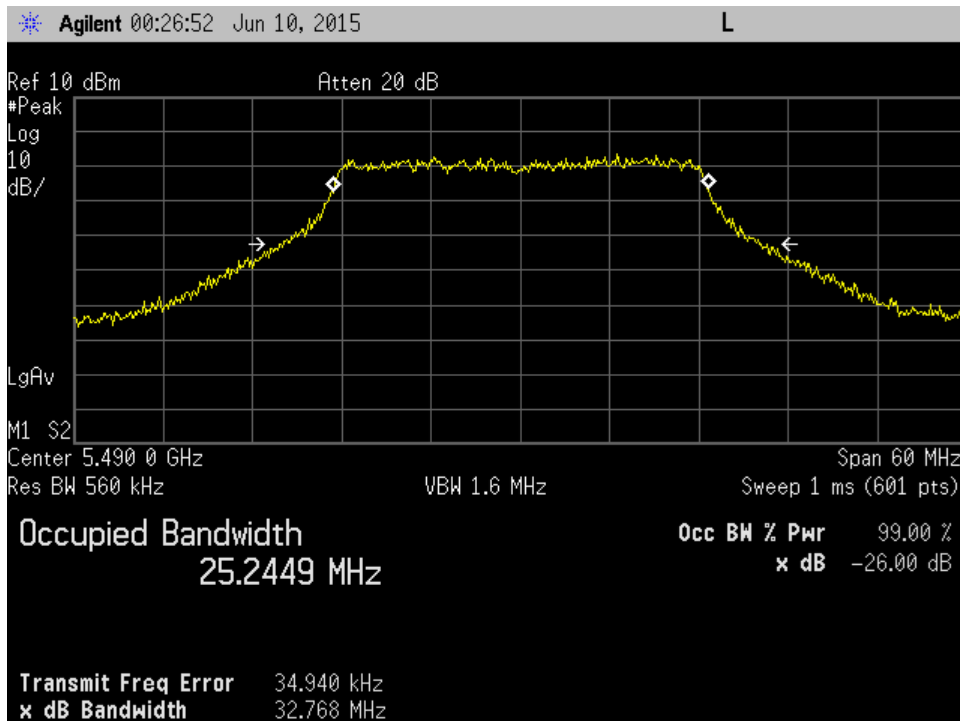




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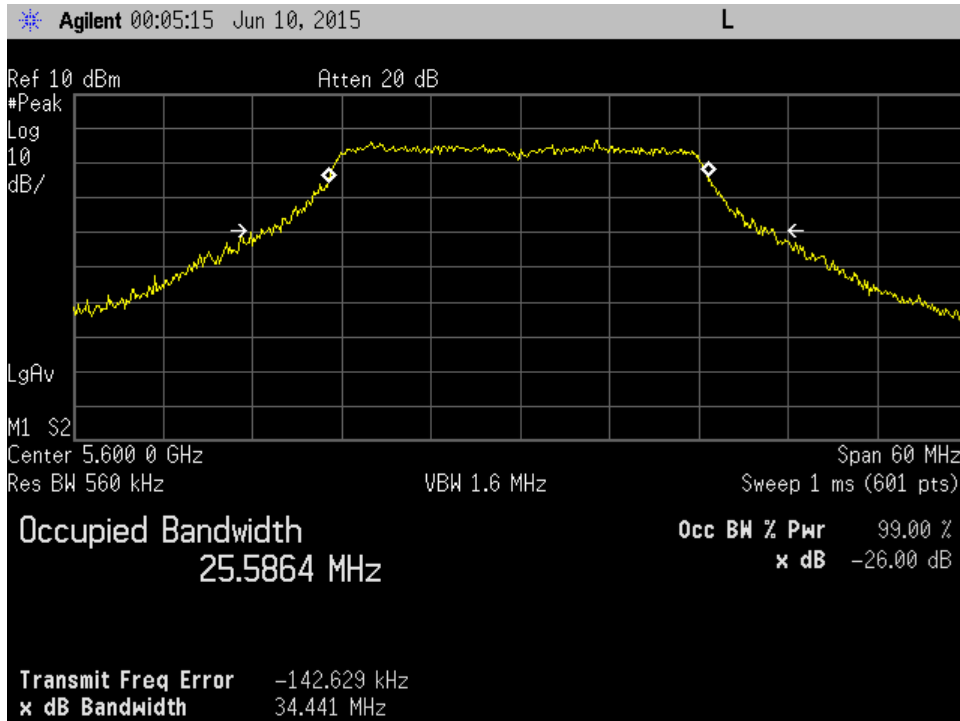


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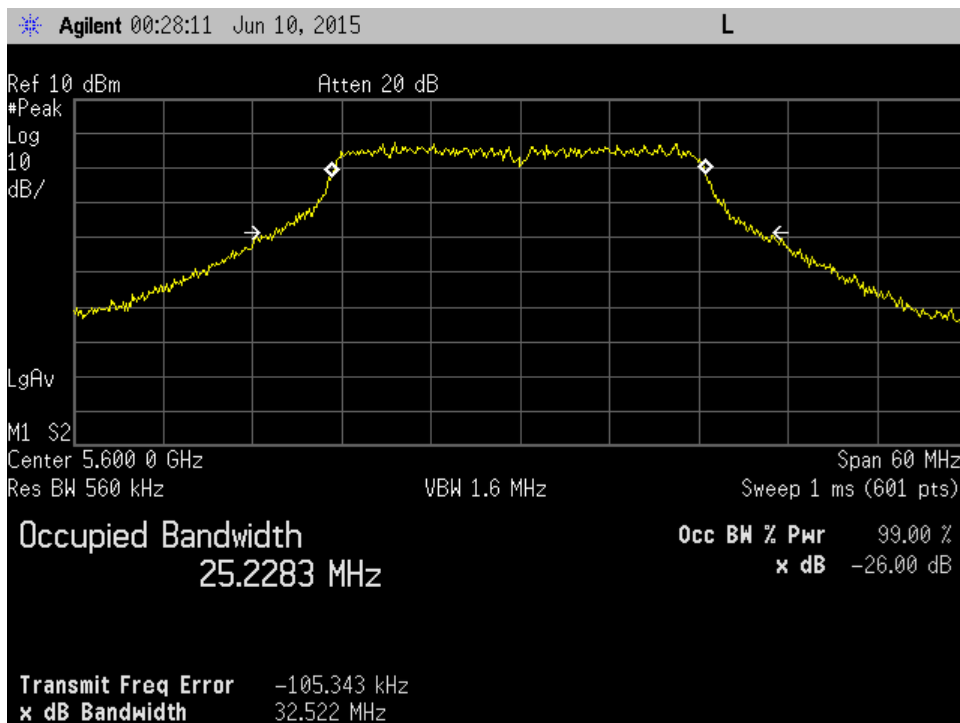




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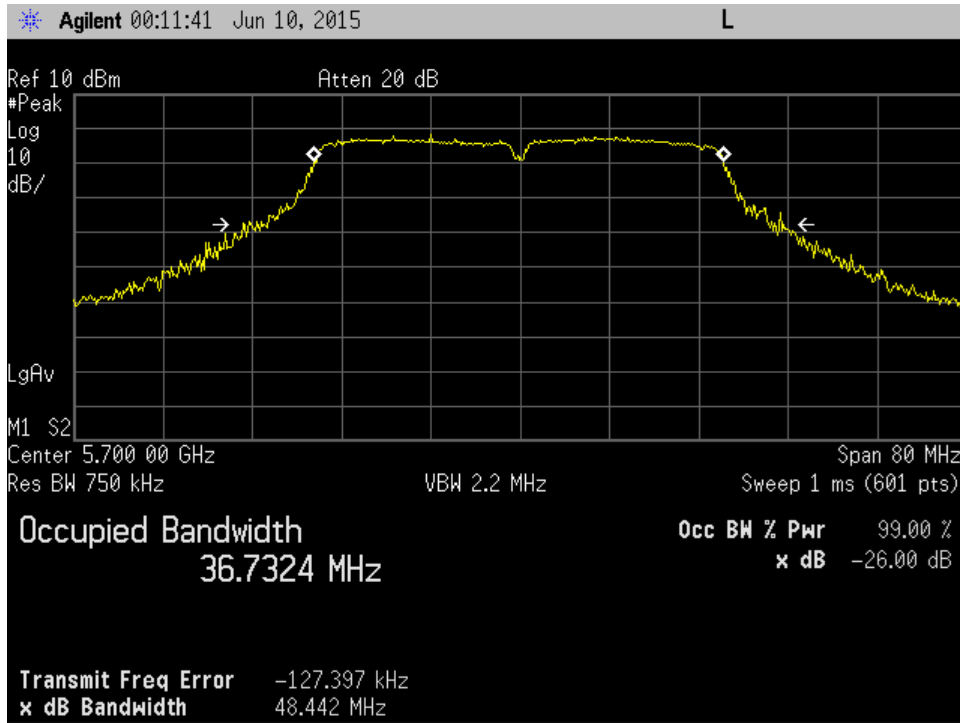


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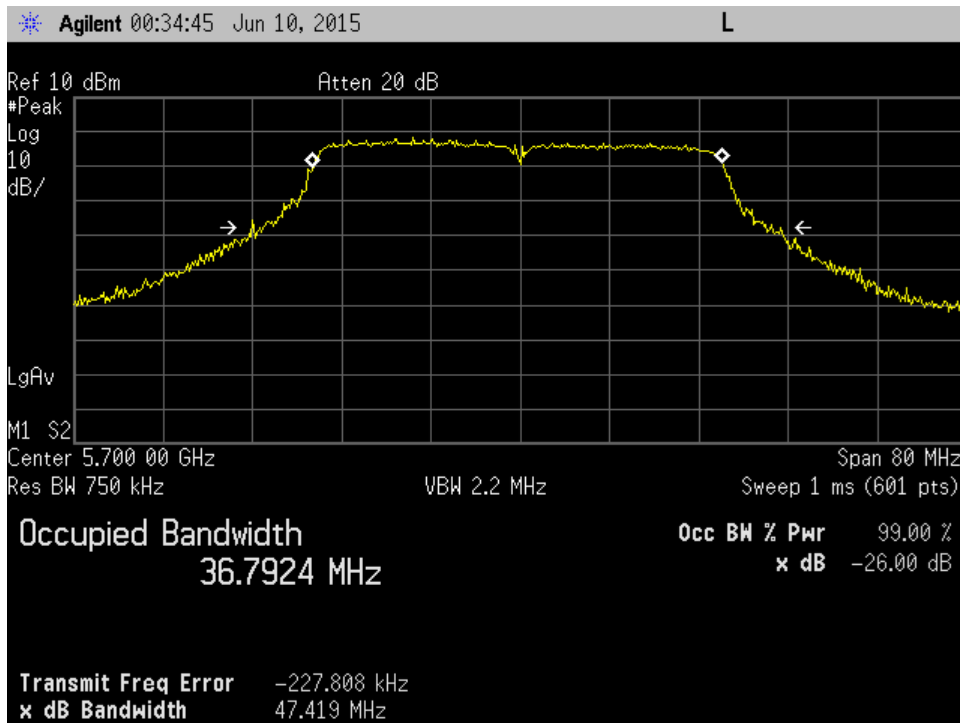




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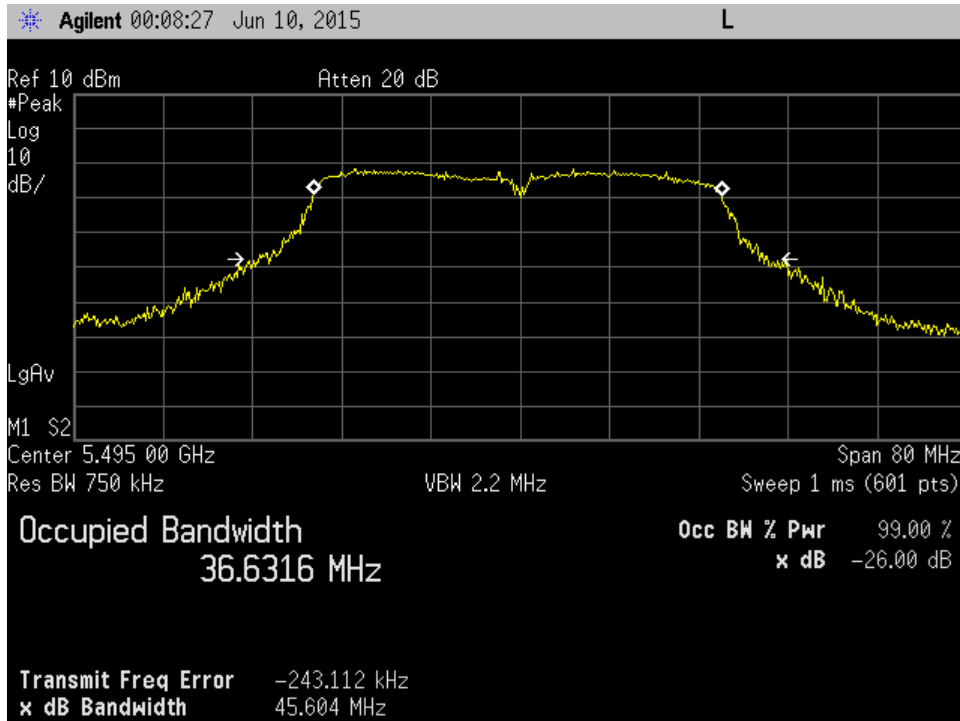


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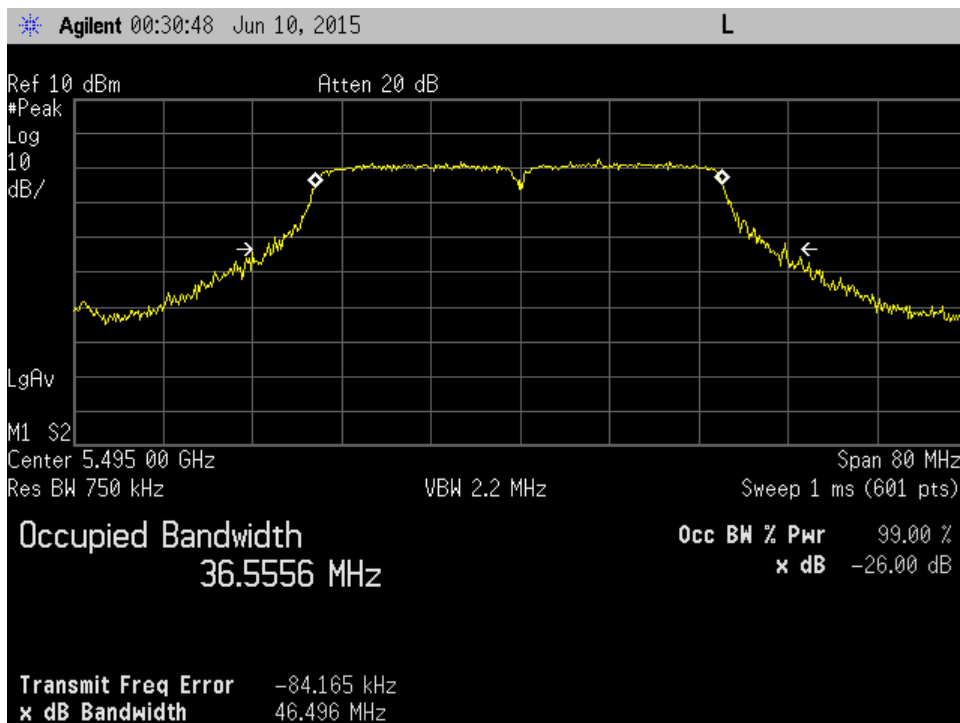




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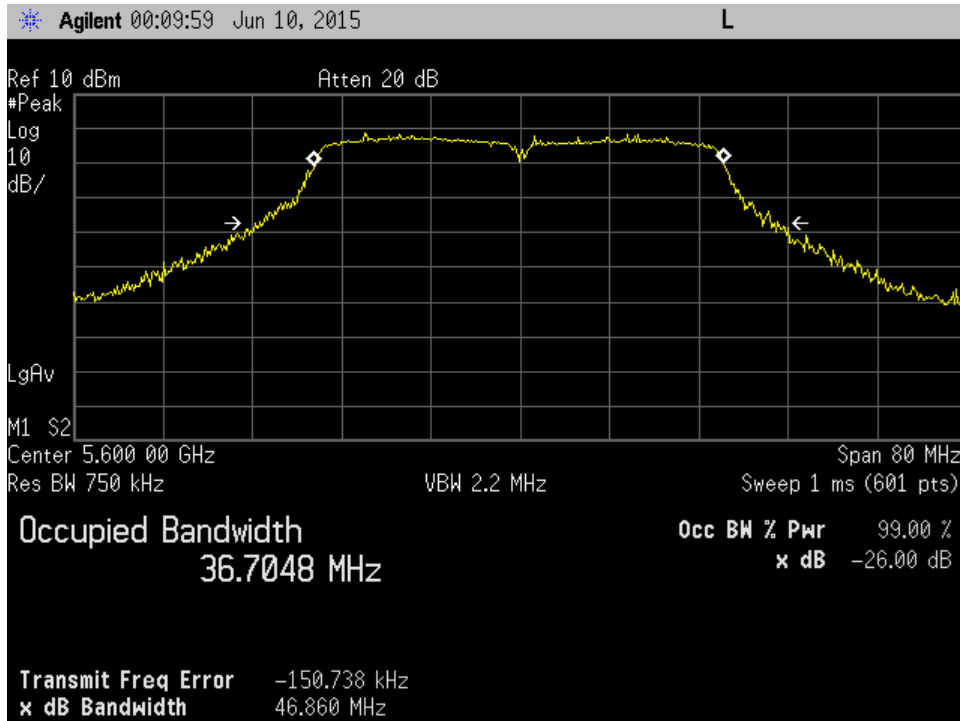


40MHz low ch J3





40MHz mid ch J1



40MHz mid ch J3

