



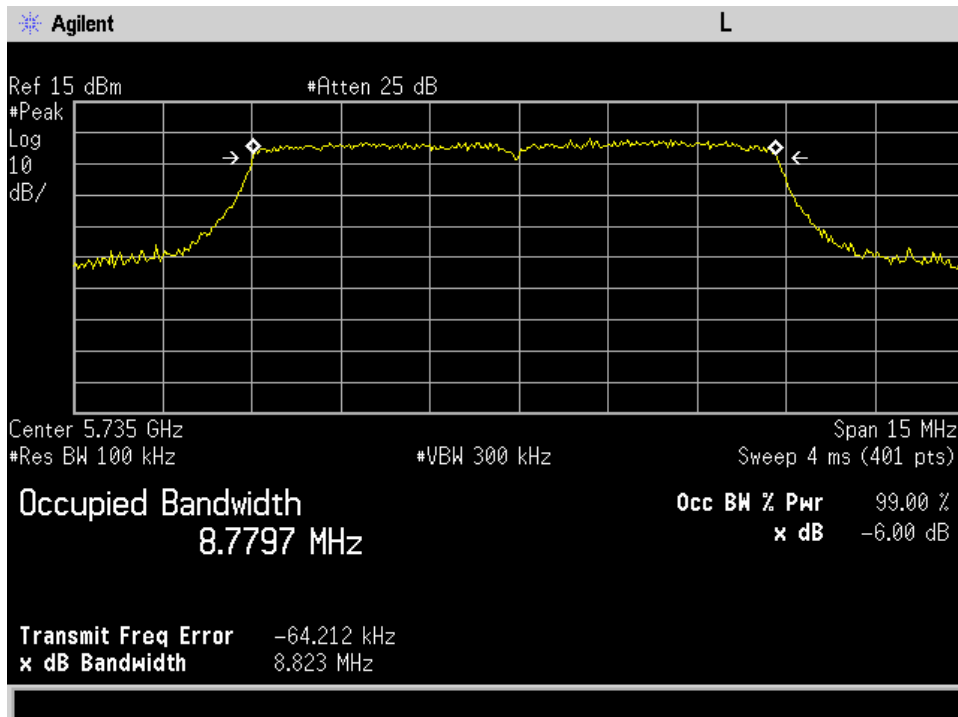
# **Annex C**

## **Occupied Bandwidth**

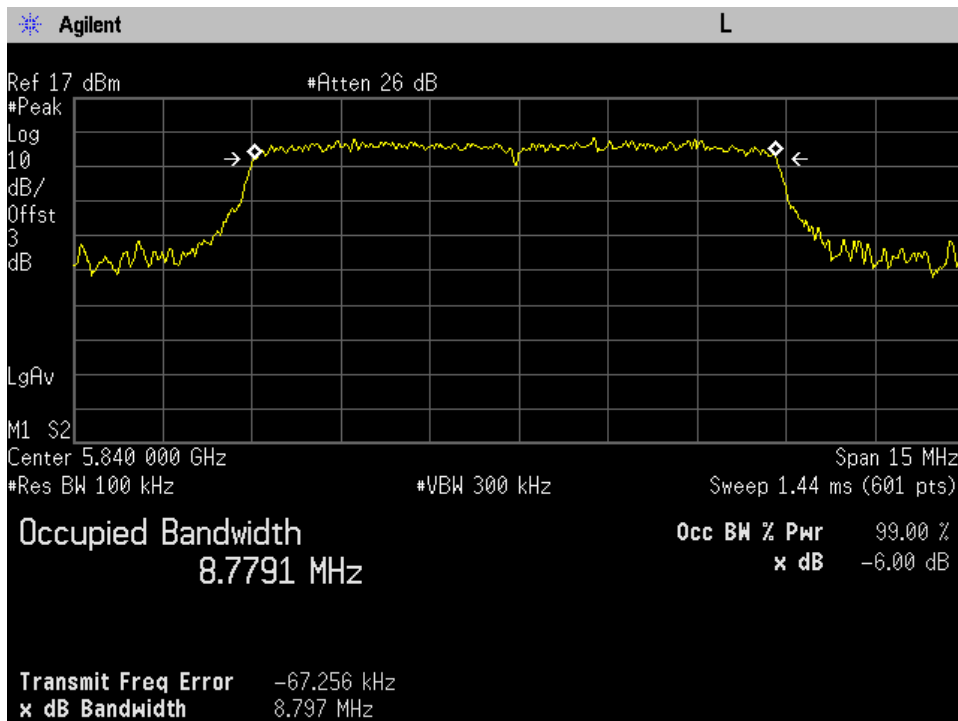
### **UNII-3**



### 10 Mhz High Ch Port 1

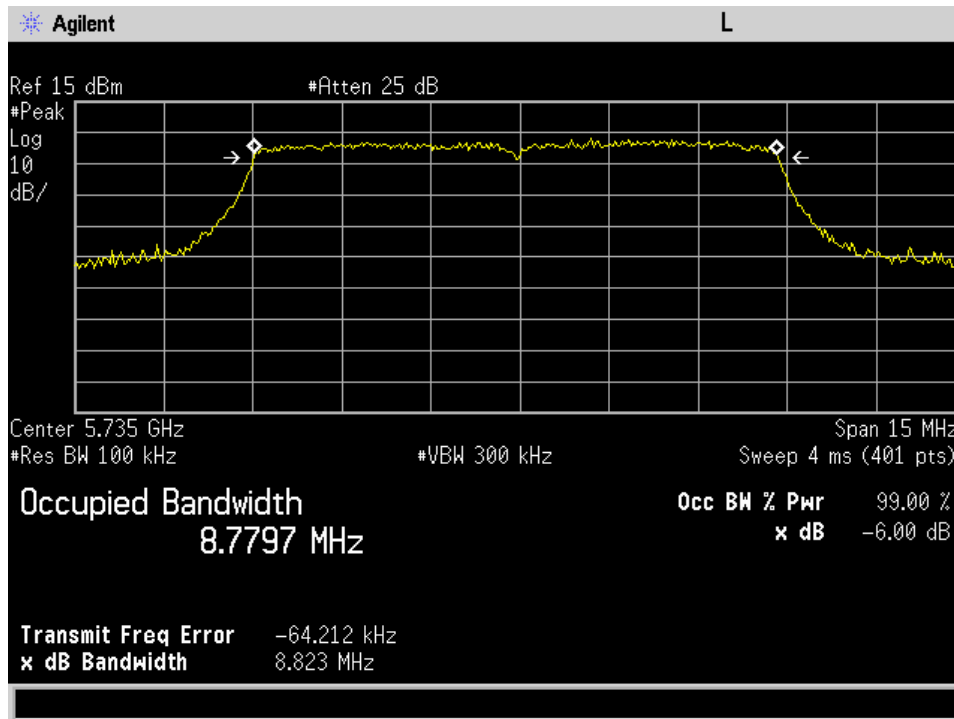


### 10 Mhz High Ch Port 2

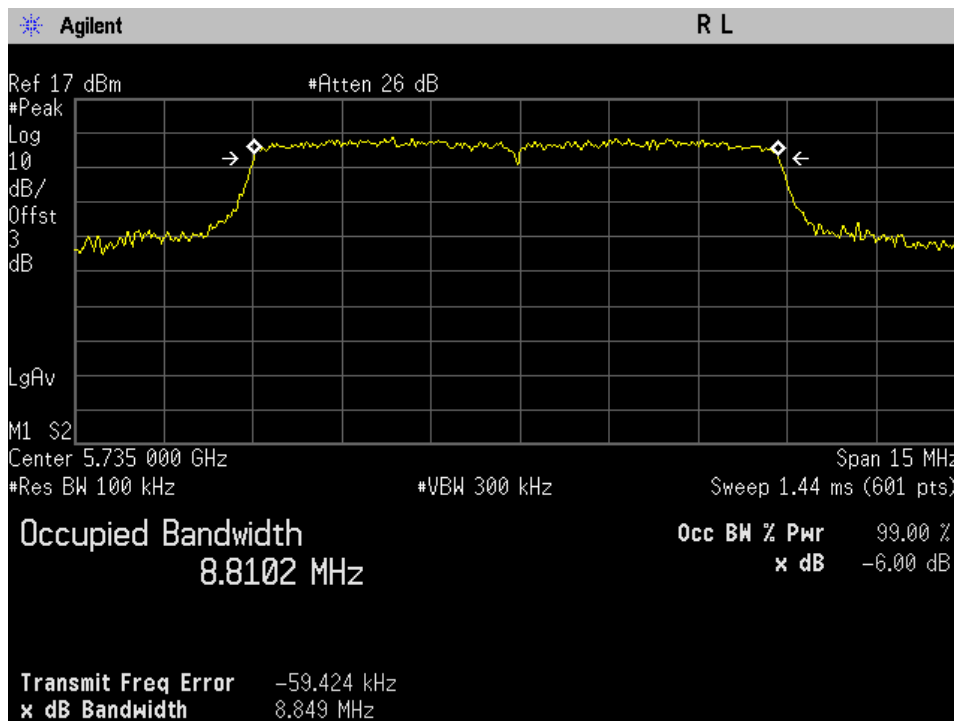




### 10 Mhz Low Ch Port 1

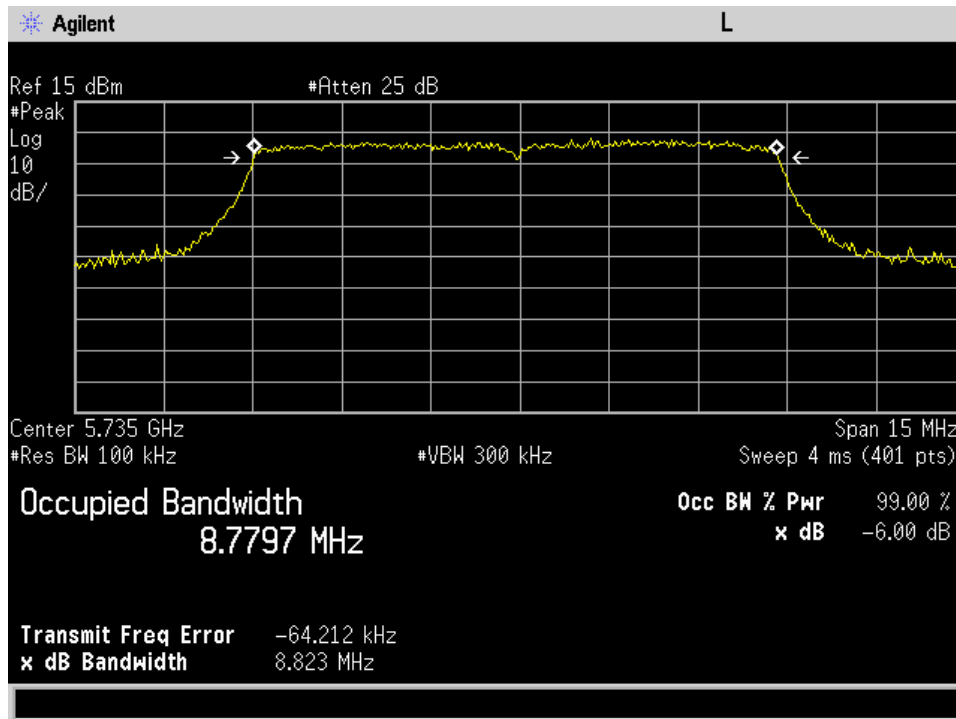


### 10 Mhz Low Ch Port 2

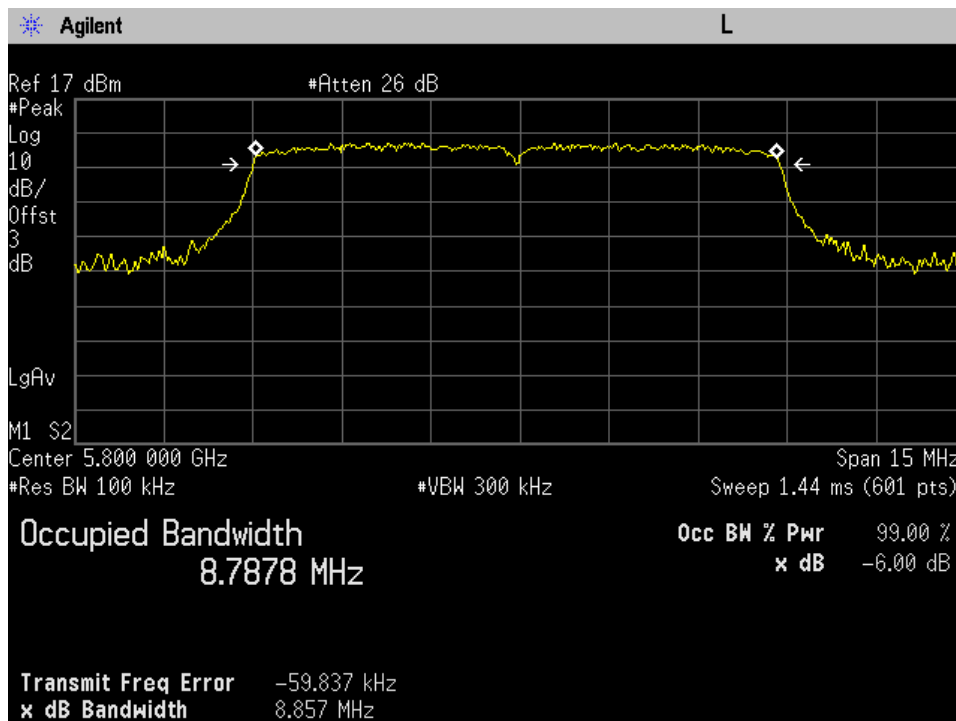




### 10 Mhz Mid Ch Port 1

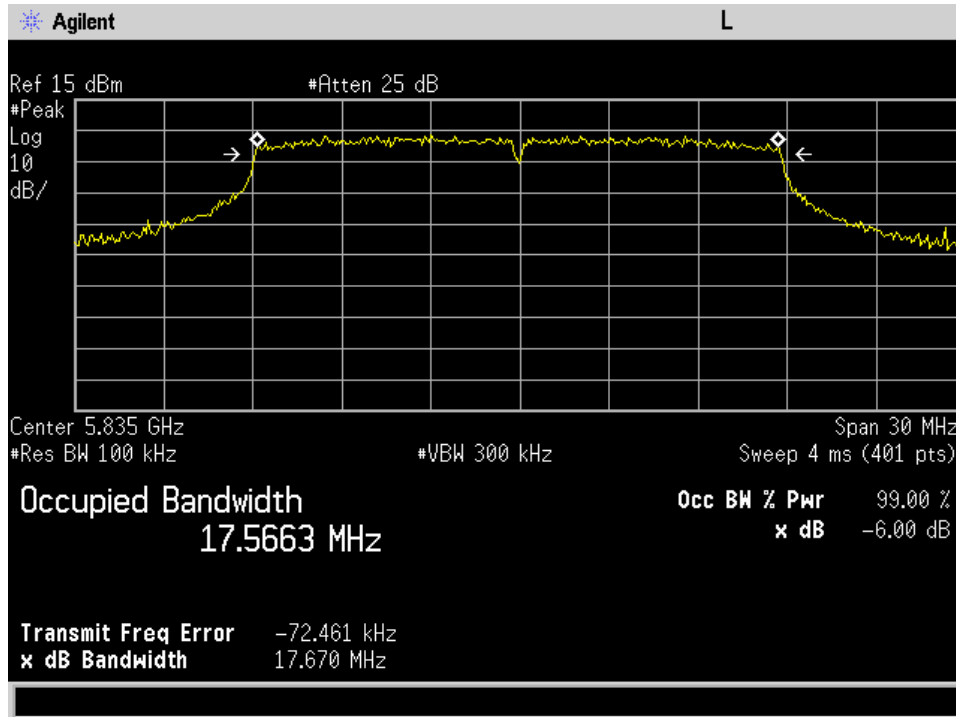


### 10 Mhz Mid Ch Port 2

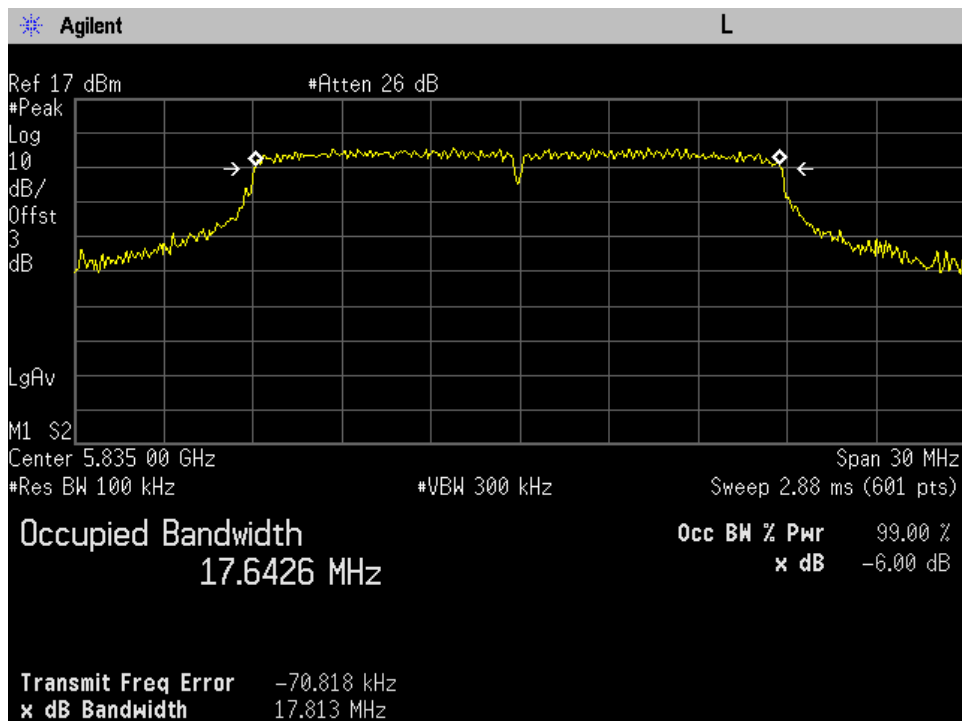




### 20 Mhz High Ch Port 1

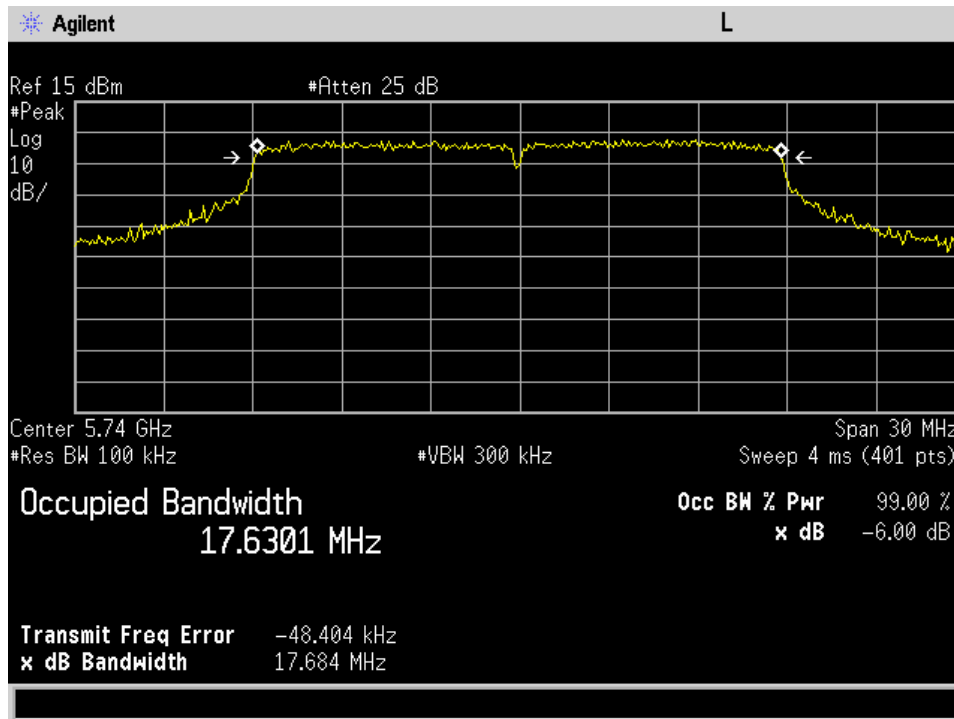


### 20 Mhz High Ch Port 2

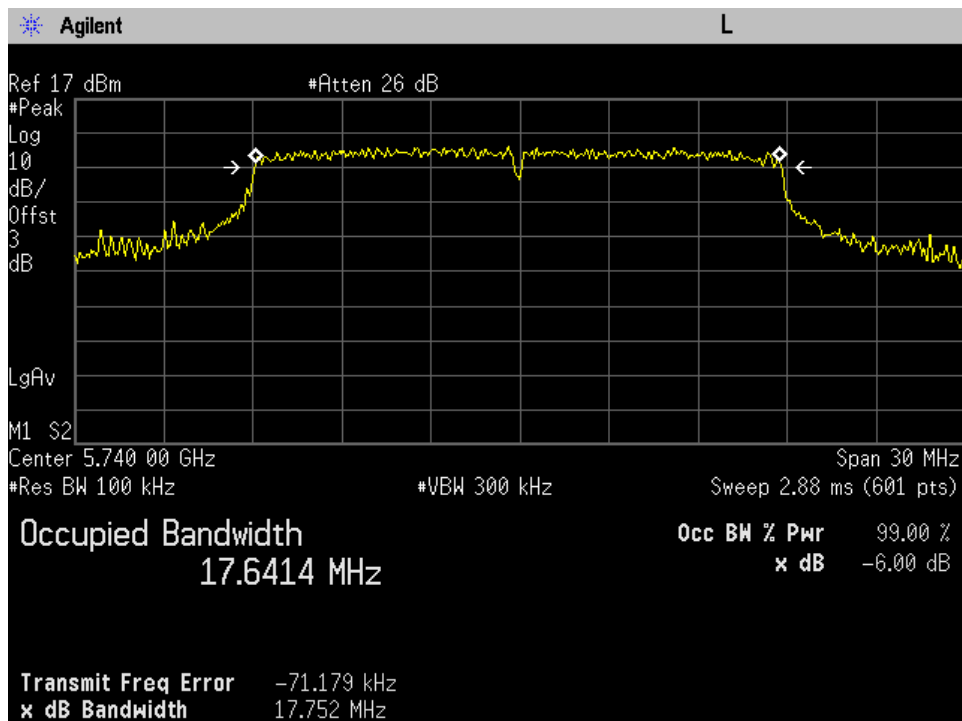




### 20 Mhz Low Ch Port 1

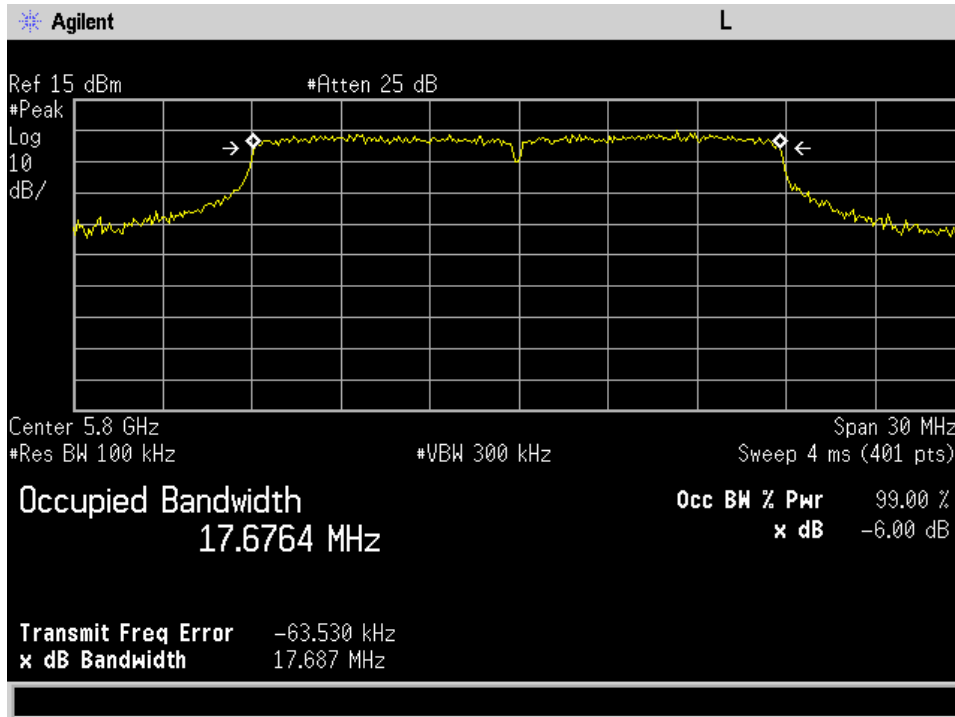


### 20 Mhz Low Ch Port 2

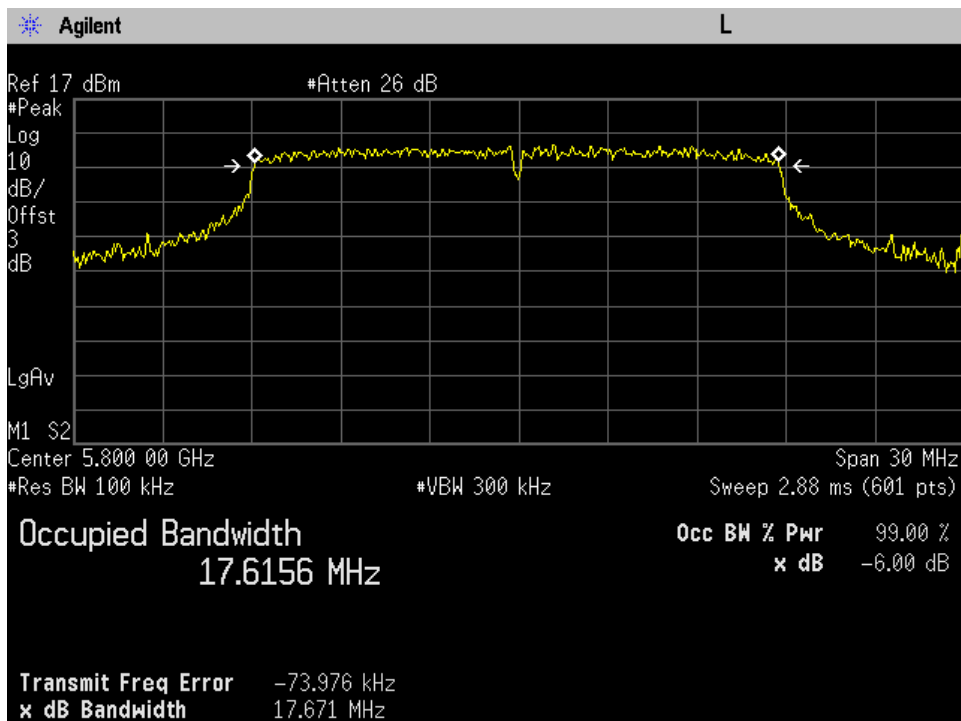




### 20 Mhz Mid Ch Port 1

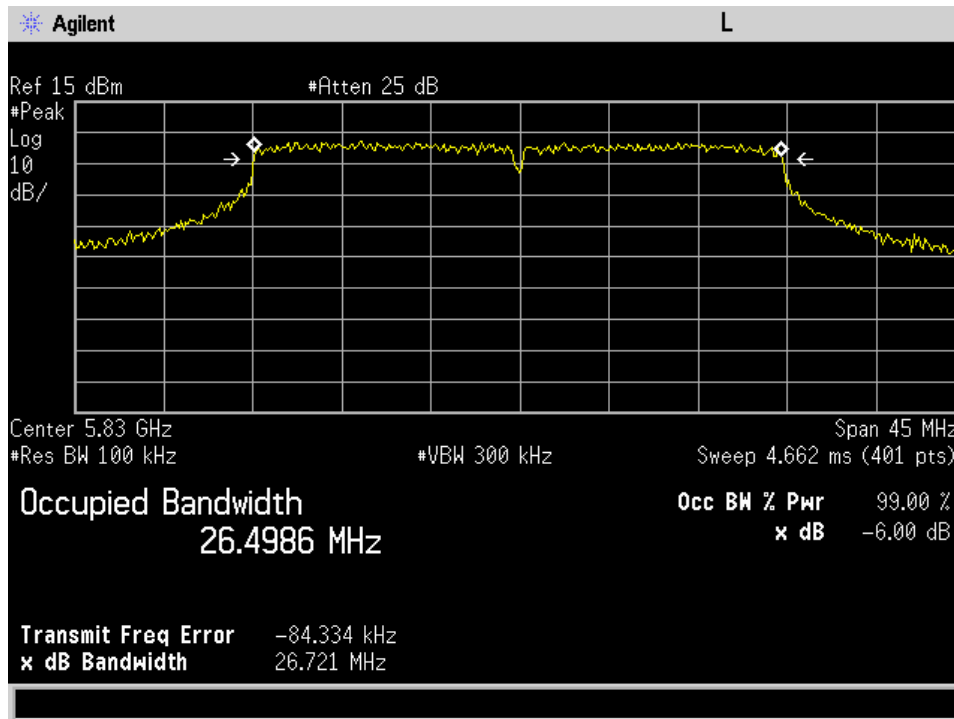


### 20 Mhz Mid Ch Port 2

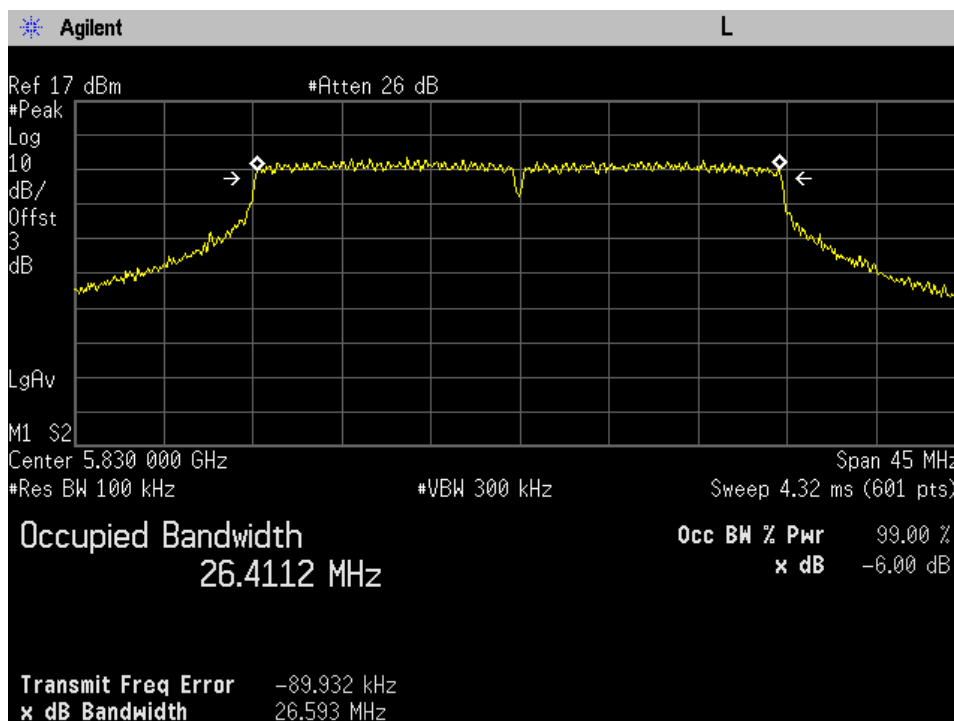




### 30 Mhz High Ch Port 1



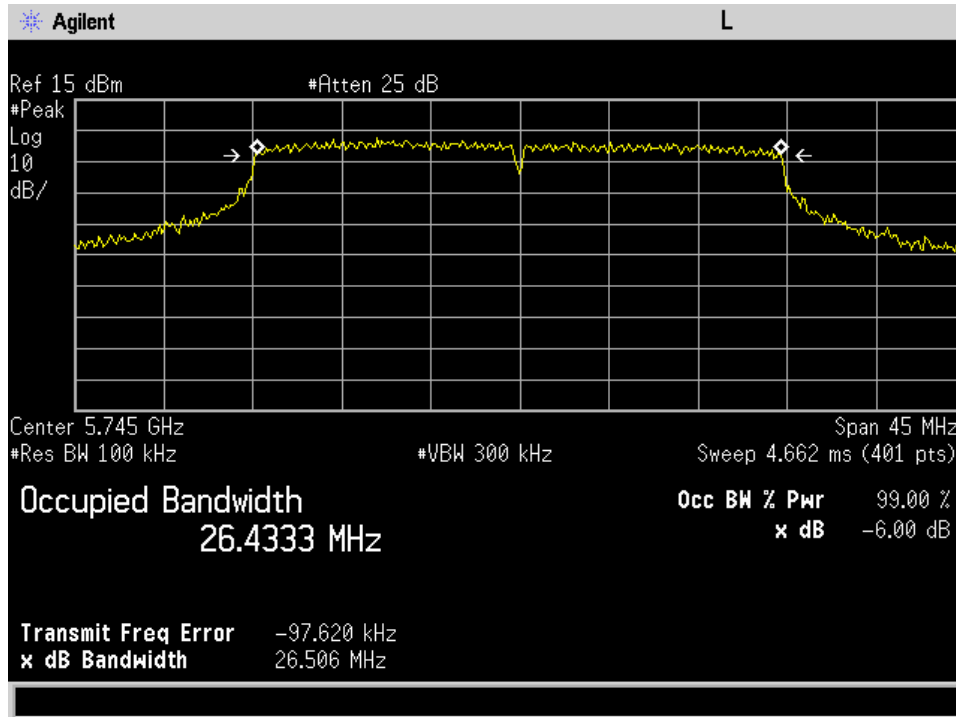
### 30 Mhz High Ch Port 2



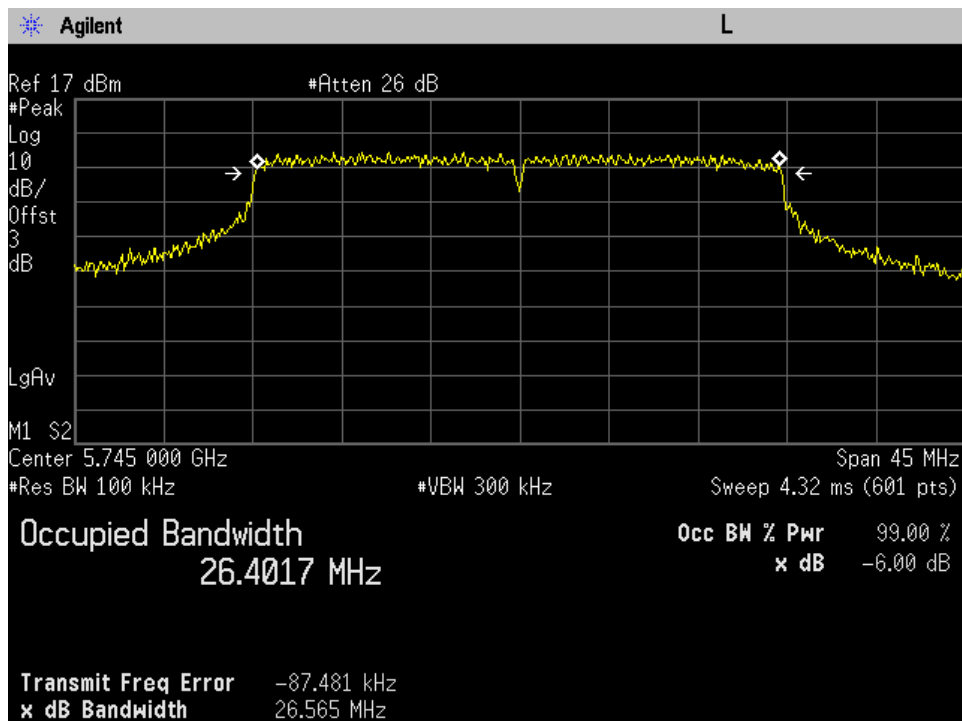




### 30 Mhz Low Ch Port 1

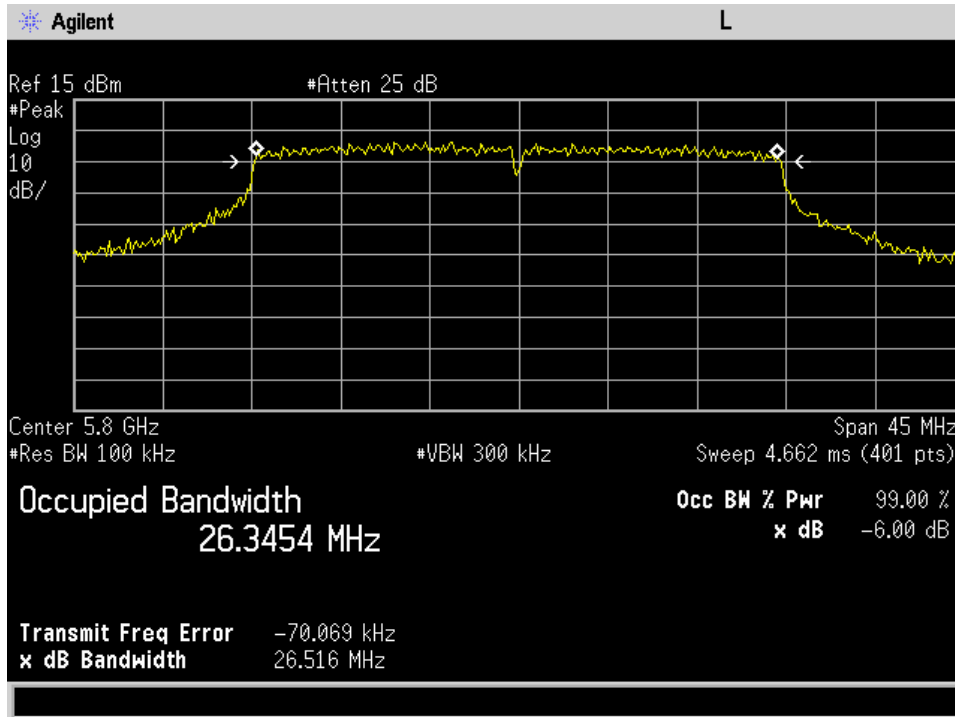


### 30 Mhz Low Ch Port 2

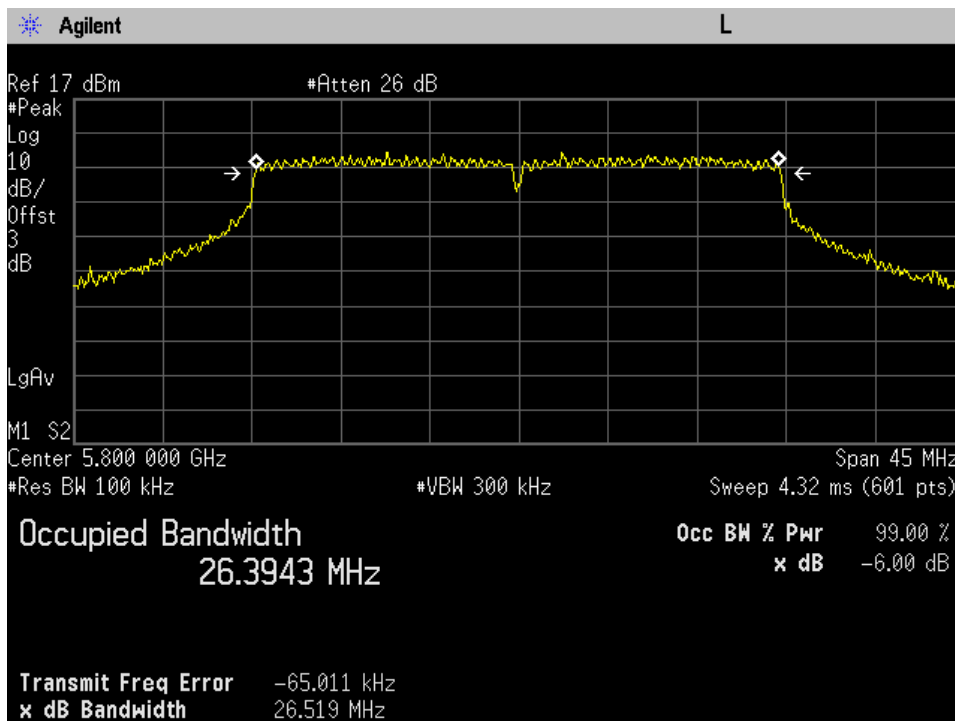




**30 Mhz Mid Ch Port 1**

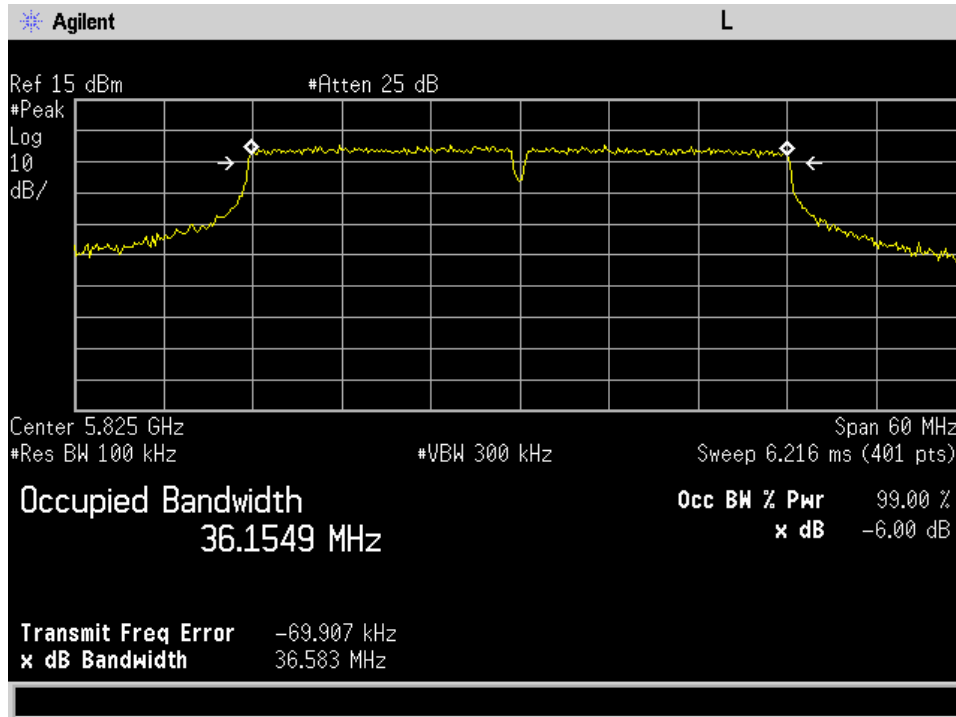


**30 Mhz Mid Ch Port 2**

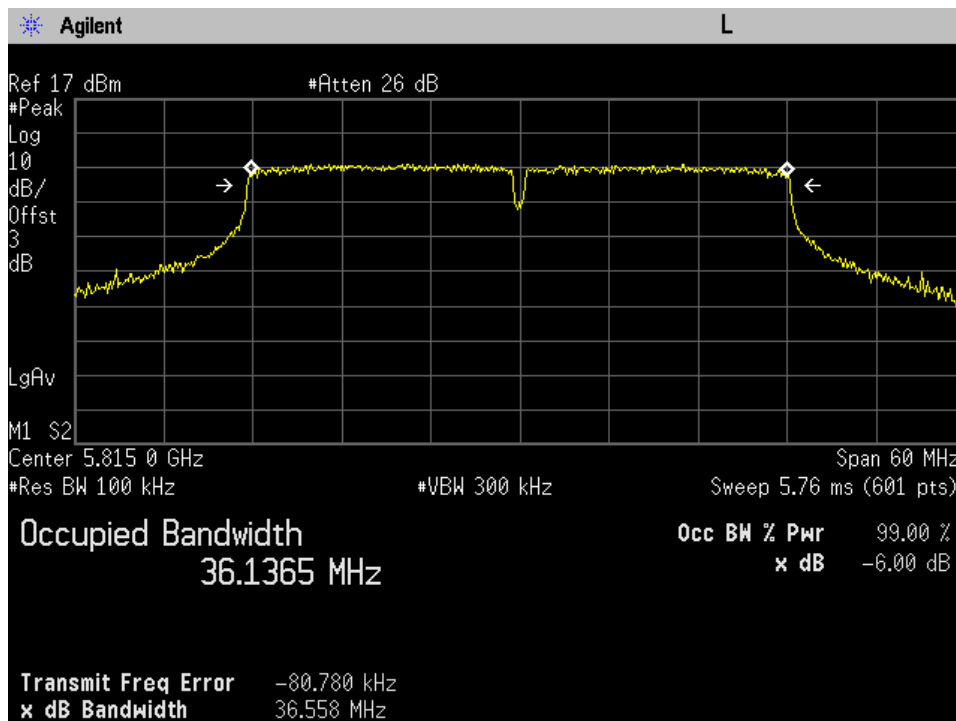




### 40 Mhz High Ch Port 1

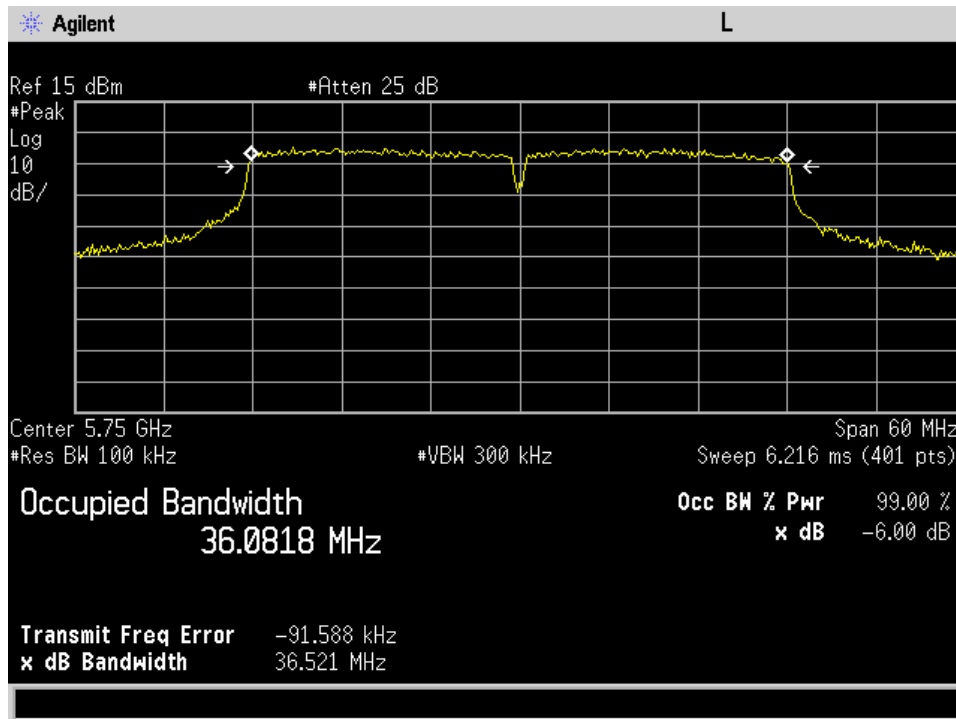


### 40 Mhz High Ch Port 2

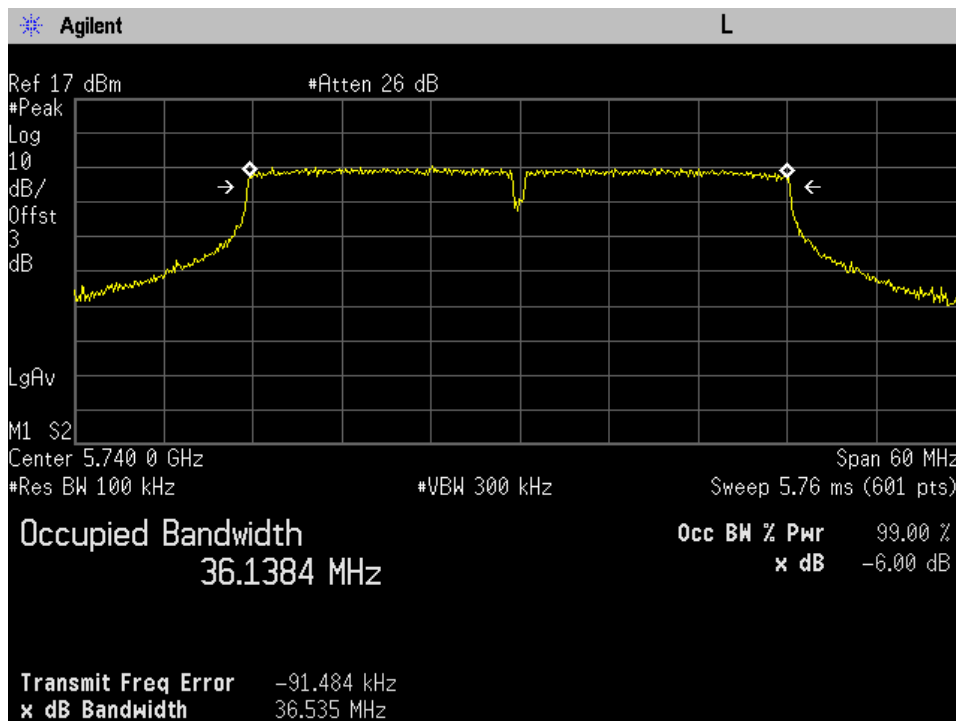




### 40 Mhz Low Ch Port 1

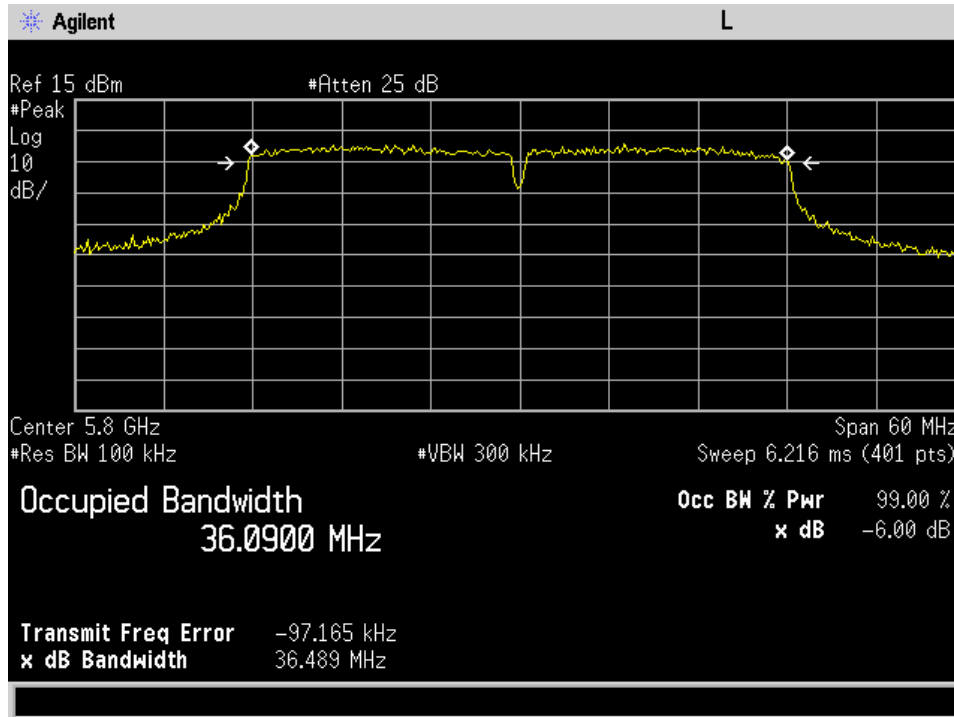


### 40 Mhz Low Ch Port 2





### 40 Mhz Mid Ch Port 1



### 40 Mhz Mid Ch Port 2

