1 Product Overview

1.1 Outline

CW6680E/CW6681E/CW6682E is an MCS-51™ Compatible high performance mixed signal microcontroller. It integrates advanced digital and analog peripherals to suit for Bluetooth Audio Player applications.

1.2 Features

- Compatible with MCS-51™ instruction set;
- Maximum 48MHz operating frequency;
- Supports MP3 decoder;
- Supports WMA decoder;
- Supports WAV decoder;
- Supports MP3 encoder;
- Keypad tone mixer;
- Two multi-function 8-bit timers, support Capture and PWM mode;
- Two multi-function 16-bit timers, support Capture and PWM mode;
- Watchdog Timer with on-chip RC oscillator;
- one full-duplex UART;
- Two SPI;
- CW6680E support Full-speed USB 2.0 Device controller;
- CW6681E support Full-speed USB 2.0 Device/Host controller;
- Independent powered RTCC;
- 48MHz PLL-based clock generator;
- Six Channels 10-bit SARADC;
- Power on Reset;
- Support Bluetooth phone.

2 Pin Definitions

2.1 CW6680E/CW6681E

2.1.1 Package

LQFP48

2.1.2 Pin Assignment

Figure 2-1 shows the pin assignments of LQFP48 package

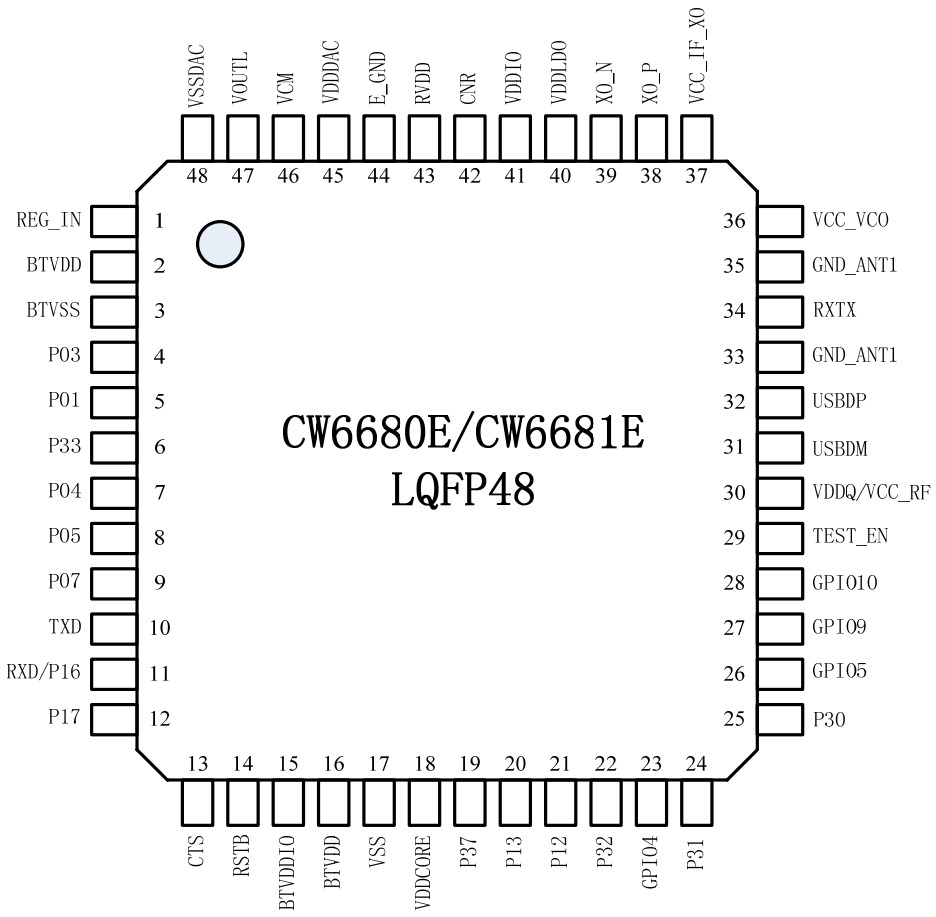

Figure 2-1 Pin Assignment for LQFP48

2.1.3 Pin Description

Table 2-1 shows the pin descriptions of LQFP48 package.

Table 2-1 LQFP48 pin description

Pin No.	Name	Type	Function
1	REG_IN	I	This pin serves as an input of the on-chip VDD and RVDD LDO regulators
2	BTVDD	PWR	Bluetooth VDD
3	BTVSS	GND	Bluetooth ground
4	P03	AI	MICIN1 VCMBUF AUXL2
5	P01	I/O	AUXR0 SDDAT2 UART0TX1 GPIO
6	P33	I/O	ADC0 PWRWKUP LVDDET CLKO GPIO
7	P04	I/O	ADC2 INT0 SPI1DO1 SPI1DODI1 PWM1 SPI0DODI1 SPI0DO1 GPIO
8	P05	I/O	ADC3 INT1 SPI1CLK1 CAP0 SPI0CLK1 GPIO
9	P07	I/O	INT3 CAP1 GPIO
10	TXD	O	UART Serial data output port for the HCI UART interface. This pin should be left unconnected if UART is not used or can be configured to GPIO
11	RXD	I	UART Serial data input port for the HCI UART interface. This pin should be left unconnected if UART is not used or can be configured to GPIO
	P16	I/O	ADC6

Pin No.	Name	Type	Function
			TMR2 PWM2 IISREFCLK AMIN CAP2 UART0TX0 GPIO
12	P17	I/O	TMR2 IISWS GPIO
13	CTS	I	UART Clear to Send-active low for HCI UART interface when the hardware flow control feature enable. This pin is used to set the system clock rate if the flow control feature is disabled
14	RSTB	I	Active low system reset. This pin contains a weak pull-up
15	BTVDDIO	I	Power supply for GPIOs
16	BTVDD	PWR	Bluetooth VDD
17	VSS	GND	Ground
18	VDDCORE	PWR	Digital 1.2V Power
19	P37	I/O	AUXL1 GPIO
20	P13	I/O	ADC5 GPIO
21	P12	I/O	GPIO
22	P32	I/O	SPI1DO0 SPI1DODI0 SDDAT01 GPIO
23	GPIO4	I/O	3.3V tolerant GPIO pin with programmable pull-up
24	P31	I/O	SPI1DI0 SDCMD1 GPIO
25	P30	I/O	ADC4 SPI1CLK0 SDCLK1 GPIO
26	GPIO5	I/O	3.3V tolerant GPIO pin with programmable pull-up
27	GPIO9	I/O	3.3V tolerant GPIO pin with

Pin No.	Name	Type	Function
			programmable pull-up
28	GPIO10	I/O	3.3V tolerant GPIO pin with programmable pull-up
29	TEST_EN	I	The test mode enable pin. This pin should be left unconnected for field application.
30	VDDQ	I	Digital block of RF circuit power supply. This pin must connect to RVDD
	VCC_RF	I	RF circuit power supply. This pin must connect to RVDD
31	USBDM	I/O	USB Negative Input/output
32	USBDP	I/O	USB Positive Input/output
33	GND_ANT1	-	Ground connection of RF I/O antenna. These pins must connect to RVSS
34	RXTX	-	RF I/O antenna pin
35	GND_ANT1	-	Ground connection of RF I/O antenna. These pins must connect to RVSS
36	VCC_VCO	I	VCO circuit power supply. This pin must connect to RVDD
37	VCC_IF_XO	I	IF and internal Crystal Oscillator circuit power supply. This pin must connect to RVDD
38	XO_P	I	Crystal or frequency reference input
39	XO_N	O	Crystal Oscillator output. Connect with XO_P if the reference clock is supplied
40	VDDLDO	PWP	LDO 5V Power
41	VDDIO	PWR	IO 3.3V Power
42	CNR	O	On-Chip RVDD LDO external decoupling capacitor pin
43	RVDD	-	On-chip 1.8V RVDD LDO output to supply internal RF circuits, this pin output typical voltage is 1.8V
44	E-GND	GND	Ground
45	VDDDAC	PWR	DAC 3.3V Power HeadPhone 3.3V Power
46	VCM	AO	DAC Bandgap voltage reference
47	DACL	AO	DAC Left Channel
48	VSSDAC	GND	DAC Ground

I: input; **O**: output; **PWR**: power; **GND**: ground; **AO**: Analog Output; **AI**: Analog Input; **NC**: not connect

2.2 CW6682E

2.2.1 Package

LQFP48

2.2.2 Pin Assignment

Figure 2-2 shows the pin assignments of LQFP48 package

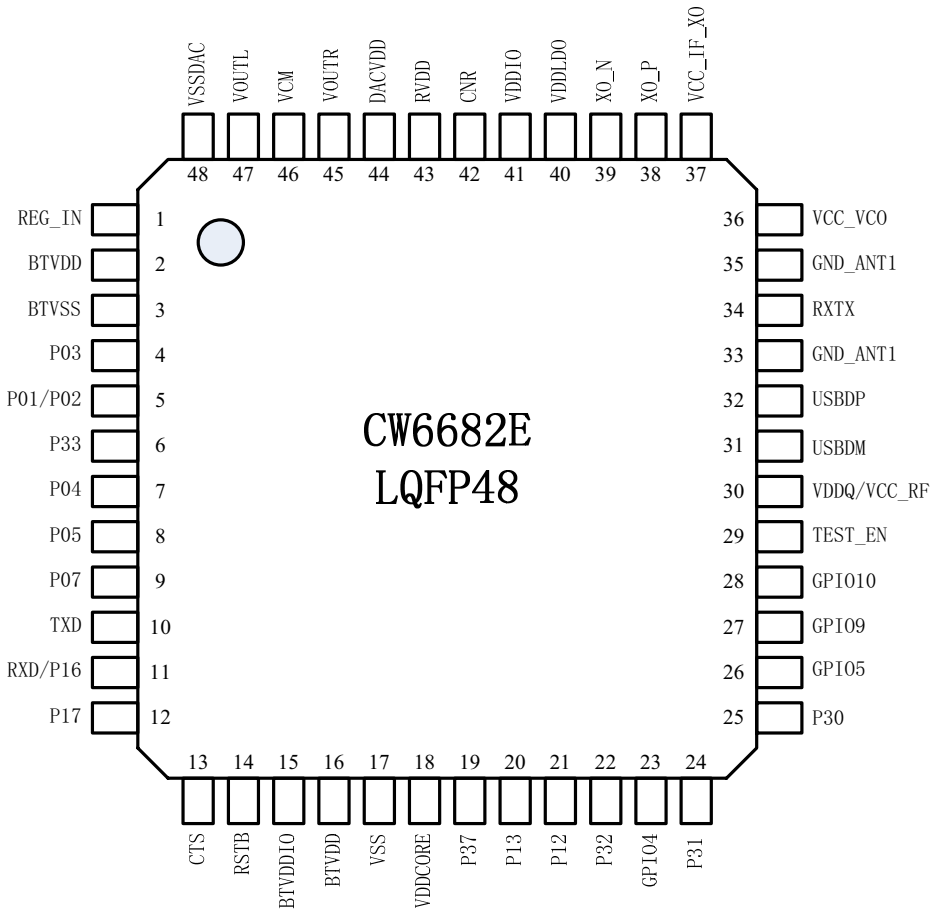

Figure 2-2 Pin Assignment for LQFP48

2.2.3 Pin Description

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23	GPIO4	I/O	3.3V tolerant GPIO pin with programmable pull-up
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44	DACVDD	PWR	DAC 3.3V Power HeadPhone 3.3V Power
45	VOUTR	AO	DAC Right Channel
46	VCM	AO	DAC Bandgap voltage reference
47	VOUTL	AO	DAC Left Channel
48	VSSDAC	GND	DAC Ground

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