T:1721M DL OUT
(To PAM)

B:1721M DL IN
(From D-Filter)

1721M DL IN
(From FPGA)

1721M DL OUT
(To FPGA)

1.1900UL PAM on/off
2.1900UL PD
3.1721UL PAM on/off
4.1721UL PD
5.6.9.10 GND
7.8 Vcc(5.6V)

Con5(1721M)

1721M UL OUT
(To FPGA)

1 2
Con6

T:1721M UL OUT
(To D-Filter)

B:1721M UL IN
(From S-Filter)

1721M UL IN
(From FPGA)

T:1900M UL OUT
(To D-Filter)

B:1900M UL IN
(From S-Filter)

1900M UL IN
(From FPGA)

1900M UL OUT
(To FPGA)

Con4(1900M)

1900M DL OUT
(To FPGA)

T:1900M DL OUT
(To PAM)

B:1900M DL IN
(From D-Filter)

<<Con1,2,4,5
1.ATT CLK; 2.ATT DATA
4.DL ATT1; 5.DL ATT2
7.UL ATT1; 8.UL ATT2
9.TEMP(for Con1)
10.DL on/off; 11.UL on/off
12.13.Vcc 3.9V; 14.GND
3.6. NC

1900M DL IN
(From FPGA)

T:800M DL OUT
(To PAM)

B:800M DL IN
(From D-Filter)

800M DL IN
(From FPGA)

800M DL OUT
(To FPGA)

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Con2(800M)

700M UL2/800M UL OUT
(To FPGA)

T:800M UL OUT
(To D-Filter)

B:800M UL IN
(From S-Filter)

700M UL2/800M UL IN
(From FPGA)

Con3

1 2

T:700M UL OUT
(To D-Filter)

B:700M UL IN
(From S-Filter)

700M UL1 IN
(From FPGA)

1.700UL PAM on/off
2.700UL PD
3.800UL PAM on/off
4.800UL PD
5.6.9.10 GND
7.8 Vcc(5.6V)

700M UL1 OUT
(To FPGA)

Con1(700M)

700M DL OUT
(To FPGA)

T:700M DL OUT
(To PAM)

B:700M DL IN
(From D-Filter)

700M DL IN
(From FPGA)