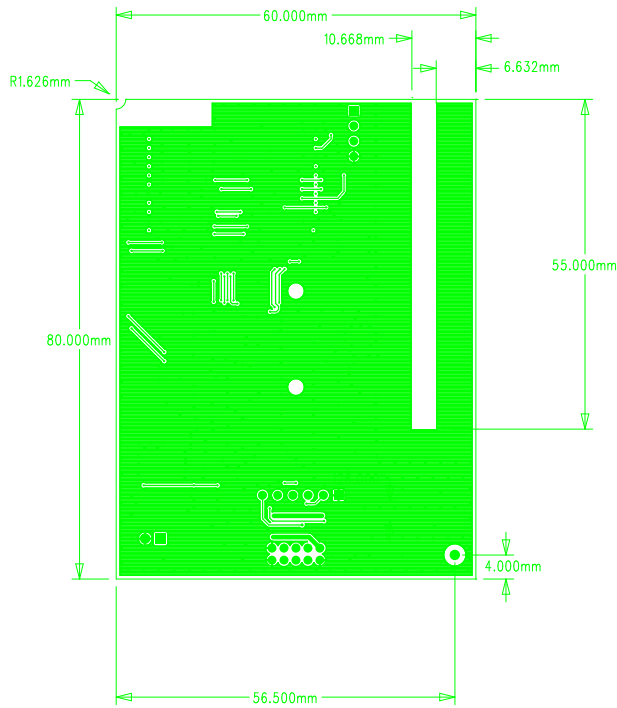


DRILL CHART



ARTWORK/FABRICATION FILES

TOP - COPPER ROUTING - COPPER1.PHO
 BOTTOM - COPPER ROUTING - COPPER2.PHO
 TOP SIDE SOLDERMASK - TOPMASK.PHO
 BOTTOM SIDE SOLDERMASK - BOTTOMMASK.PHO
 TOP SIDE SILK SCREEN - TOPSILK.PHO
 TOP SIDE SOLDER PASTE MASK - TOPPASTE.PHO
 NC DRILL FILE - NCDRILL.DRL

REVISION RECORD		
REV.	DESCRIPTION	DATE
1.0	ECN 29-2017 INITIAL RELEASE	03/23/17
2.0	ECN 48-2017	06/23/17
2.1	ECN 110-2017	07/05/17
3.0	ECN 149-2017	09/13/17

FABRICATION NOTES:

- BOARD FABRICATION AND QUALITY ACCEPTANCE PER IPC-6012B, CLASS 2. THESE DETAILED NOTES AND INSTRUCTIONS MAY SUPERSEDE IPC REQUIREMENTS.
- ALL BOARD DIMENSIONS IN INCHES. TOLERANCE = +/-0.004" UNLESS NOTED OTHERWISE.
- MATERIAL - FR-4 GRADE GLASS EPOXY, LEAD-FREE COMPLIANT PER IPC-4101B/126 OR /129. CTE Z-AXIS EXPANSION <=3.5%, Tg >320 DEG C, Tg >140 DEG C. MINIMUM FLAMMABILITY RATING UL 94V-0
- HOLE WALL PLATING OF 0.5 MILS MINIMUM FOR BURIED OR BLIND VIAS AND 0.7 MILS MINIMUM FOR THROUGH VIAS.
- FINISH-2-10uIN IMMERSION GOLD PLATING OVER 50-200uIN ELECTROLESS NICKEL (ENIG).
- SOLDER MASK OVER BARE COPPER, LPI, PER IPC-SM-840, REGISTRATION +/-0.003", BLUE. NO COVERAGE ON SOLDER PADS PERMITTED. ALL VIAS TO BE TENTED
- SILK SCREEN BOTH SIDES WITH WHITE EPOXY NON-CONDUCTIVE INK. SILKSCREEN SHOULD BE TRIMMED OFF ANY SOLDERED ENTITY.
- HOLE SIZE TOLERANCE = +/- 0.003" UNLESS NOTED OTHERWISE.
- HOLE CENTERS AND PAD CENTERS TO BE CONCENTRIC WITHIN 0.003"
- COPPER ADDITION (THEIVING, CROSSHATCH, ETC) IS NOT PERMITTED ON ANY LAYERS UNLESS OTHERWISE SPECIFIED. COPPER ADDITION IN BREAKAWAY AREAS FOR PANEL FORMS IS ACCEPTABLE.
- LAMINATION, STACKUP, COPPER PLATING, AND ETCHING TO BE CLOSELY MONITORED TO ENSURE PRODUCT MEETS DESIGN INTENT. NO CHANGES TO MATERIALS AND/OR GERBER FILES ARE PERMITTED WITHOUT WRITTEN APPROVAL.
- UL DATE/LOGO AND/OR VENDOR INFORMATION CAN BE IN SILKSCREEN NOMENCLATURE WHERE SPACE PERMITS, UNLESS OTHERWISE SPECIFIED. NO ADDITIONAL COPPER, LOGOS, OR TEXT OF ANY KIND IN COPPER LAYERS.
- CONTROLLED IMPEDANCE 20 mil WIDE MICROSTRIP TRACES ON SIGNAL LAYER 1 TO BE 107 OHMS +/- 10% REFERENCED TO LAYER 2 GROUND PLANE, WHEN MEASURED BY A TDR (TIME DOMAIN REFLECTOMETER) IN ACCORDANCE WITH IPC-2221 AND IPC-TM-650, METHOD 2.5.5.7. IMPEDANCE TESTING MAY BE PERFORMED AS PER A C=0 SAMPLING PLAN IN ACCORDANCE WITH IPC 6012B CLASS 2. DIELECTRIC THICKNESS AND/OR TRACE WIDTH MAY BE ADJUSTED TO MEET IMPEDANCE REQUIREMENTS.

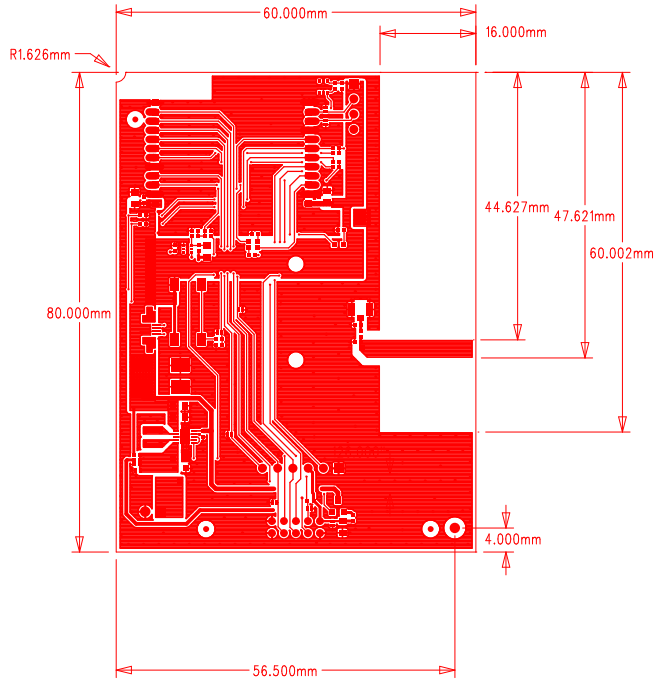


Note: Material dielectric thickness may need to be adjusted to meet total thickness requirement.



DRAWN BY: PGS	DATE: 03/23/17	TITLE: LoRa Sensor Controller
CHECKED BY: CMH	DATE: 03/23/17	PROJECT: LoRa Sensor Controller - CBBRCA10W10V10M10D10M
APPROVED BY: JMB	DATE: 03/23/17	SIZE: A
		DRAWING NO: 750-01040
		REV: 3.0
FILENAME:	SCALE: 1 TO 1	SHEET: OF

DRILL CHART



ARTWORK/FABRICATION FILES

TOP - COPPER ROUTING - COPPER1.PHO
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REVISION RECORD		
REV.	DESCRIPTION	DATE
1.0	ECN 28-2017 INITIAL RELEASE	03/23/17
2.0	ECN 40-2017	06/23/17
2.1	ECN 110-2017	07/05/17
3.0	ECN 149-2017	09/13/17

FABRICATION NOTES:

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DRAWN BY: PGS	DATE: 03/23/17	TITLE: LoRa Sensor Controller
CHECKED BY: CMH	DATE: 03/23/17	PROJECT: LoRa Sensor Controller - CBBRDATION/ER/4100P
APPROVED BY: JMB	DATE: 03/23/17	SIZE: A
		DRAWING NO: 750-01040
		REV: 3.0
FILENAME:	SCALE: 1 TO 1	SHEETS: OF