FCC ID: SQ9XKT1294
IC: 5768A-XKT1294
Model: XKT1294

Technical Description:

The function of main ICs are mentioned as below.

1) U1(EM9201) acts as 2.4GHz RF Module .
2) U1(SNC82340) acts as MCU .
3) U4(LC1463CB5ATR33)acts as Voltage Regulator .
4) U2(eSW4506A)acts as motor driver IC and associated circuit act as motion control of model.
5) Oscillator of Y1 (16.384MHz) and Y2 (32.768kHz) are used for MCU.
6) Oscillator of X1 (26MHz) is used for RF IC.

Antenna Used: PCB trace antenna has been used.

Frequency Range: 2422MHz – 2460MHz (3 channels)

Channel Table: 2422MHz, 2446MHz, 2460MHz

Modulation Type: GFSK

Transmitting Power Tolerance
1) Nominal Field Strength at 3m (91dBuV)
2) Nominal Conducted Power at antenna output (-3dBm)
3) Production tolerance (+/-3dB)
4) Antenna gain(0dB)

CMM-9201/9202-V7.1
Mini 2.4GHz Transceiver Module

C-MAX

Description

The CMM-9201-V7.1 module is a miniaturised 2.4GHz transceiver module based on EM Microelectronic's low energy RF transceiver EM9201/02. The module is highly optimized for proprietary link application requiring ultra low power consumption and short time-to-market. It offers a plug and play solution for any EM9201 application without any additional hardware nor RF layout. Built in with a folded-dipole PCB antenna, this small sized, low cost module provides an ideal solution to wireless 2.4GHz license-free application worldwide.

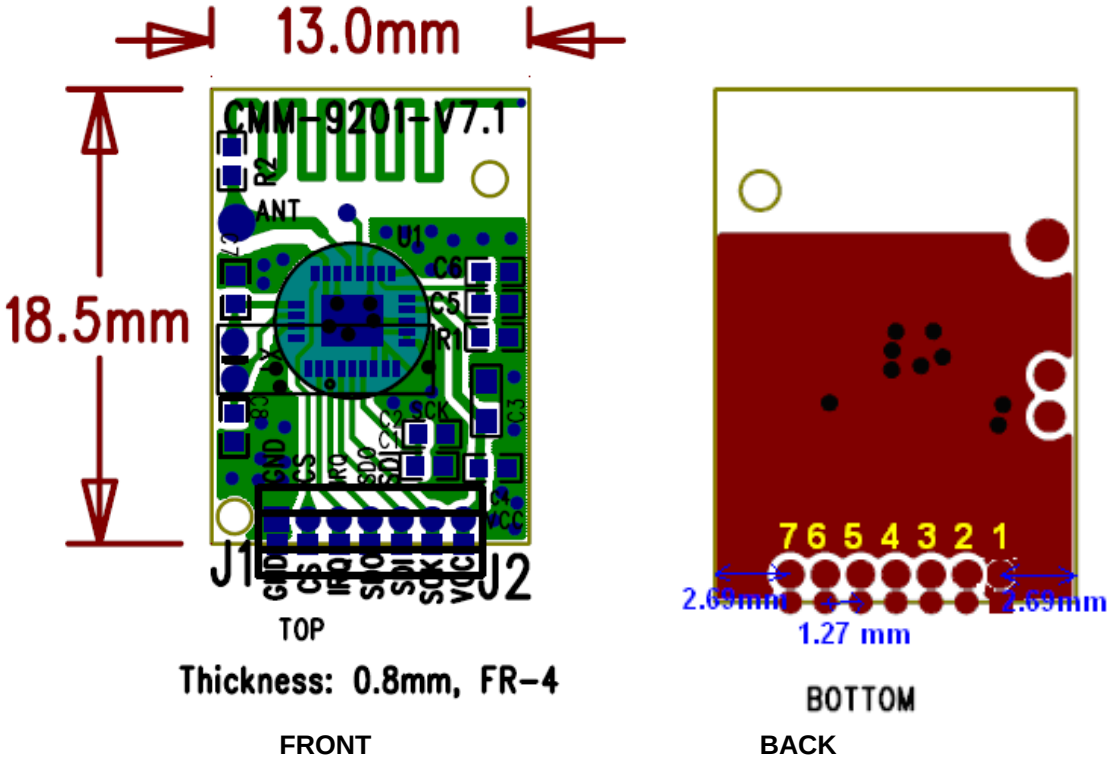
The EM9201/02 is a low-voltage 2.4GHz transceiver IC with built-in link-layer logic permitting proprietary wireless links in the 2.400 … 2.4835 GHz ISM band. It has a radio core with a low-IF architecture and GFSK modulation scheme being compliant with the emerging Bluetooth low energy technology standard..

1.1 Features

- Fully integrated 2.4 GHz transceiver (Die form)
- Operating voltage 1.9V ~ 3.6V
- Mini-sized (18.5mm x 13mm)
- Integrated Battery Low Detection
- Programmable RF output level (-20 to +2 dBm) via software control
- Low current consumption
  (0.8uA at standby, 14.2mA (@2.5V) in RX, 12.9 mA (@2.5V) in TX (0dBm))
- 1Mb/s (CMM-9201), 2Mb/s (CMM-9202) data rate
- No Tuning necessary
- Reaches 60m (CMM-9201) at open space line of sight
- GFSK modulation
- SPI interface to host controller

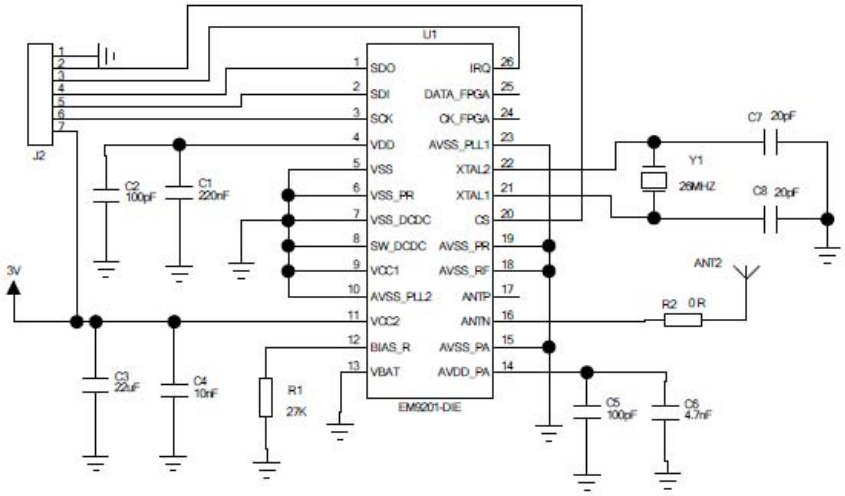
1.2 Module Dimension & Pin Assignement

Pin Number	Pin Name	Pin Description
1	GND	Ground Connection
2	CS	Chip Select (Active LO)
3	IRQ	Interrupt Output for external host Controller
4	SDO	SPI Data Output
5	SDI	SPI Data Input
6	SCK	SPI Clock Input
7	VCC	Power Supply



Module thickness: 5.5mm max.

1.3 Module Reference Circuit diagram



1.4 Module Electrical Specifications

Specification	CMM-9201	CMM-9202
Voltage Range	1.9V to 3.6V	1.9V to 3.6V
Battery-low detection (adjustable)	2.1V to 2.45V	2.1V to 2.45V
Frequency Range	2.4 to 2.484 GHz	2.4 to 2.484 GHz
Modulation	GFSK	GFSK
On-air data rate	1Mbps	2Mbps
RF channels	40	40
Current Consumption (Vcc = 2.5V)		
- RX mode	14.2mA	14.5mA
- TX mode (0dBm output power)	12.9mA	12.5mA
- Standby Low Power mode	85 uA (typ.)	85 uA (typ.)
- Power-down mode	0.8uA	0.8uA
Programmable output power	-20dBm to +2dBm	-20dBm to +2dBm
RF setup time (Standby <-> TX/RX)	Max 180 us	Max 180 us

2. Ordering information

C-MAX Module Part Number	Max Data Rate	Typical Operating Voltage
CMM-9201-V7.1	1 Mbps	1.9 ~ 3.6V
CMM-9202-V7.1	2 Mbps	1.9 ~ 3.6V

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Tel.: +852-2798-5182
Fax: +852-2798-5379
e-mail: enquiry@c-max.com.hk

C-MAX Technology Ltd (Shenzhen)
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Luohu District, Shenzhen, PR China,
Tel：+86-755-25181858
Fax：+86-755-25181859

Fully integrated, low power 2.4 GHz Transceiver

Description

EM9201 is a low-voltage 2.4GHz transceiver IC with built-in link-layer logic suitable for proprietary wireless links in the 2.400 … 2.4835 GHz ISM band.

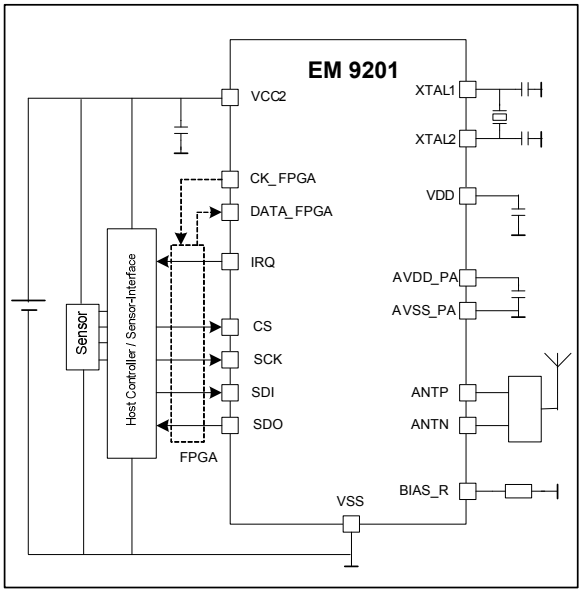
EM9201 features a radio core with a low-IF architecture and GFSK modulation scheme being compliant with the emerging Bluetooth low energy technology standard.

Control of the link-layer logic is possible though a standard SPI interface. To achieve this, an external host-controller MCU is required.

EM9201 includes a special mode called bridge, which allows direct control of the RF interface and which can be used to emulated any proprietary protocol, employing an external FPGA,

EM9201 can operate from a 3 V battery or any other source of power such as any external LDO regulator.

Typical Application Schematic



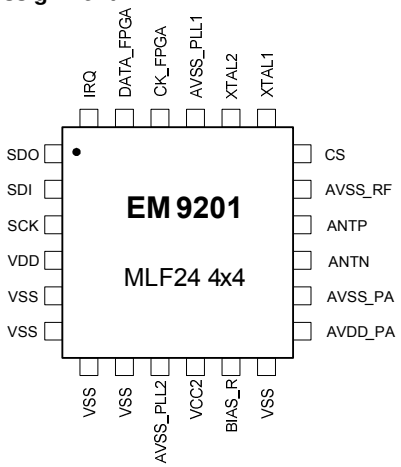
Features

- Wide operating voltage range from 1.9V to 3.6V.
- Suitable for Lithium battery.
- Bluetooth Low Energy-compliant GFSK modulation
- Low drift of PLL frequency by design
- 1Mb/s On air data rate
- Programmable RF output level:
  -20 dBm … + 2dBm in 8 steps
- No antenna matching elements needed through appropriate PCB antenna design :
- 200 Ω differential impedance of antenna port
- Low-cost 26MHz Xtal, frequency tolerance +/-30ppm
- BLD function: battery level detection in accordance with selected battery
- Current consumption (V_{CC2} = 2.5V)
  14.2 mA in RX
  12.9 mA in TX (0dBm output power)
  0.8 µA in power-down mode
- MLF24 4x4 package

Applications

- Remote sensing in general
- Wireless mouse, keyboard etc.
- Wireless sensors in watches
- Wireless sports equipment
- Alarm and security systems

Pin Assignment



Contents

1. Introduction

The EM9201 is a highly integrated multi-channel RF transceiver designed for low-power and low-voltage wireless applications in the world wide ISM frequency band at 2.400 - 2.4835GHz.

EM9201's TX-chain features a completely on-chip GFSK transmitter based on direct synthesis of the RF-signal directly applied to the 2.4GHz power amplifier. The output power can be digitally tuned in a wide range (-20 dBm …+2 dBm) in order to optimize the current consumption for a wide set of applications. The on-air transmission rate is 1Mb/s.

Thanks to the very robust low-IF architecture employed in the RX-chain, the EM9201 can operate without the need of expensive external filters for the blocking of undesired RF-signals. EM9201 features a fully on-chip low noise, high sensitivity 2.4 GHz front-end. The fast configurability of the integrated frequency synthesizer makes the EM9201 also suitable for frequency hopping systems.

Employing a properly designed antenna with a differential real impedance of 200 Ohm, there is not need of further external components to achieve the on-air communication with the EM9201. Adaptation to any other antenna type is anyway ensured through a properly designed matching network.

These features make the EM9201 an attractive choice for a broad range of wireless applications, where power-efficient battery operation is a needed. Thanks to the cheap bill-of-material and the few of-the-shelf components required, EM9201 can make the difference in terms of system cost.

1.1 Block diagram

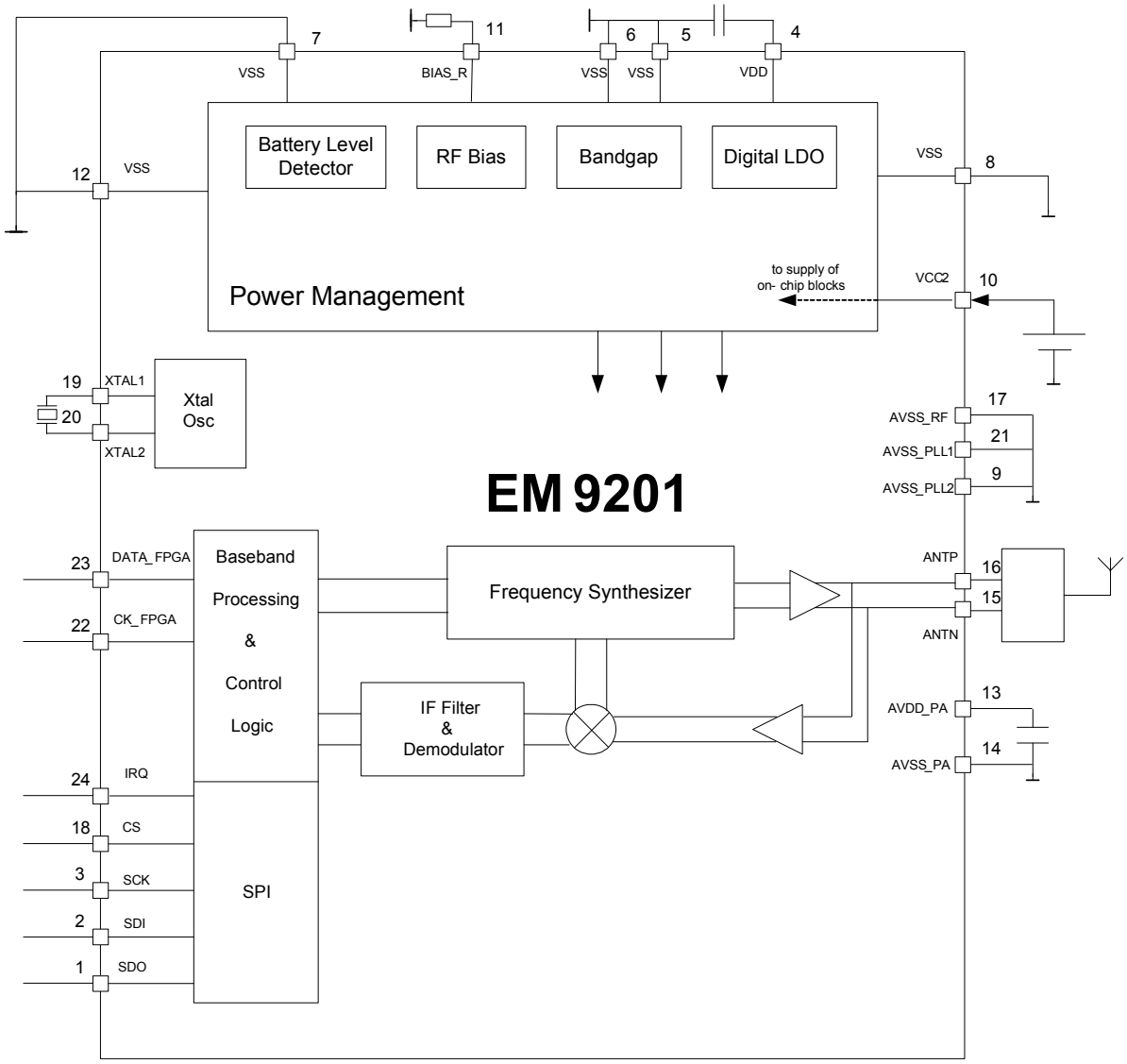


Figure 1.1: Simplified block diagram. Not all external components shown

1.2 Pin description

This section describes how the power supply shall be connected to the EM9201. In Figure 1.2, a configuration schematic for the power lines is depicted. Table 1.1 summarizes a list of recommended external components. For a proper operation of the chip, all pins with labels VSS or AVSS shall be connected to the common PCB ground.

Pin Nr	Name	Pin type	Description
1	SDO	Digital Output	SPI data output
2	SDI	Digital Input	SPI data input
3	SCK	Digital Input	SPI clock input
4	VDD	Power	Positive supply of digital part. This terminal shall not to be loaded by any external circuitry
5	VSS	Ground	Negative supply of digital part [1]
6	VSS	Ground	Negative supply [1]
7	VSS	Ground	Negative supply [1]
8	VSS	Ground	Negative supply [1]
9	AVSS_PLL2	Ground	Negative supply of PLL [1]
10	VCC2	Power	Main chip supply.
11	BIAS_R	Analog	Terminal for bias-setting resistor.
12	VSS	Ground	Negative supply [1]
13	AVDD_PA	Power	Regulated output voltage of the PA. This terminal shall not to be loaded by any external circuitry
14	AVSS_PA	Ground	Negative supply of PA [1]
15	ANTN	RF	Negative antenna terminal
16	ANTP	RF	Positive antenna terminal
17	AVSS_RF	Ground	Negative supply of RF part [1]
18	CSN	Digital Input	SPI Chip Select
19	XTAL1	Analog In	Xtal oscillator input
20	XTAL2	Analog Out	Xtal oscillator output
21	AVSS_PLL1	Ground	Negative supply of PLL [1]
22	CK_FPGA	Digital Output	Clock out for optional FPGA
23	DATA_FPGA	Digital I/O	Data terminal for optional FPGA
24	IRQ	Digital Output	Interrupt output for external host controller

[1] For a proper operation of the chip, this terminal shall be connected to a common ground plane.

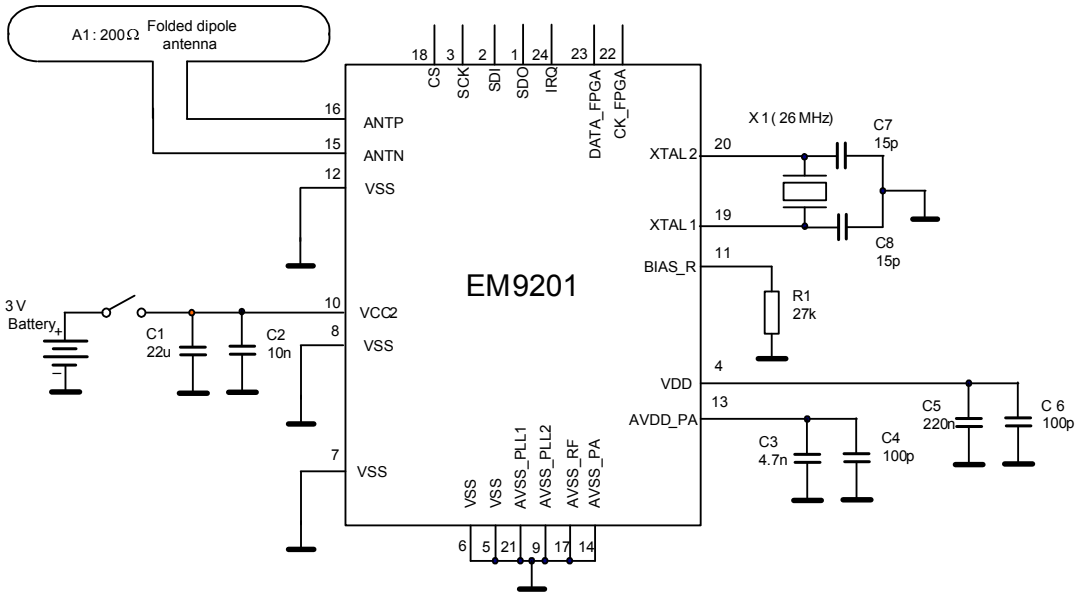


Figure 1.2: EM9201 power configurations

Component	Value	Footprint	Description
A1	200Ω	-	Printed PCB antenna or matching network
C1	22uF	0805	Storage capacitor, X5R +/- 10% ESR <100 mΩ
C2	10nF	0402	VCC2 decoupling, +/- 10%
C3	4.7nF	0402	LDO-PA decoupling capacitor, +/- 10%
C4	100pF	0402	LDO-PA decoupling capacitor, +/- 10%
C5	220nF	0805	LDO-Digital decoupling capacitor, +/- 10% ESR < 4 Ω
C6	100pF	0402	LDO-Digital decoupling capacitor, +/- 10%
C7 [2]	15pF	0402	XTAL Load Capacitor, +/- 5%
C8 [2]	15pF	0402	XTAL Load Capacitor, +/- 5%
R1	27kΩ	0402	RF-biasing resistor, +/- 2%
X1	26MHz	-	Crystal. Example: NX3225SA

Table 1.1: Recommended component list for the power section of the EM9201

[2] C5 and C6 shall be adjusted accordingly to the Crystal load capacitance. Described values are referred to a crystal load capacitance of 10pF.

2. Electrical specifications

2.1 Absolute Maximum Ratings

Table 2.1 summarizes the absolute maximum rating for the EM9201. Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified electrical characteristics may affect device reliability or cause malfunction. EM9201 is available in a green-mold and lead free MLF 4x4 package. The maximum soldering conditions are specified as in Jedec J-STD-020C standard.

Parameter	Symbol	Min.	Max.	Unit
System Ground	GND	-0.2	0.2	V
Supply Voltage	V_{SUP}	GND - 0.2	3.6	V
Voltage at remaining pin	V_{PIN}	GND - 0.2	V_{SUP} + 0.2	V
Storage temperature	T_{st}	-50	150	°C
Electrostatic discharge referred to GND according to Mil-Std-883C, method 3015.7	V_{ESD}	-2000	+2000	V

Table 2.1: Absolute maximum ratings

2.2 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level unless otherwise specified.

2.3 General Operating Conditions

General operating conditions for EM9201 are summarized in Table 2.2. These parameters are specified based on the component list defined in Table 1.1 and on application schematic of Figure 1.2.

Parameter	Min	Typ	Max	Unit
Supply voltage	1.9	3.0	3.3	V
Temperature range	-20		+70	°C

Table 2.2: EM9201 General operating conditions

2.4 Electrical Characteristics

2.4.1 Current consumption

This section summarizes the estimated current consumption of the EM9201 from the pin VCC2. The parameters defined in Table 2.3 are specified based on the component list defined in Table 1.1 and on application schematic of Figure 1.2. Functional modes used in the table are defined in section 3.2. Unless otherwise specified, the voltage VCC2 is set to 2.5V. Typical values are stated at room temperature (T=25 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power-Down	Icc_pd	No oscillators running, register values kept		0.8		µA
Standby mode [3]	Icc_stdby	26MHz Xtal oscillator active		140		µA
Standby low power mode [3]	Icc_stdby_lp	Xtal low power mode activated		85		uA

[3] Typical value based on NX3225SA Xtal type with 15pF load capacitors.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transmit Mode Current	Icc_tx	Pout = 0 dBm, channel 19		12.9		mA
Receive Mode Current	Icc_rx			14.2		mA

Table 2.3: Typical current consumption

2.4.2 Vcc2 Supply monitor

Parameter	Conditions	Min	Typ	Max	Unit
Battery-Low Detection Threshold levels	Battery Protection Battery Low Early warning	2.1	2.23 2.49	2.45	V

2.5 RF Characteristics

This section summarizes the RF performances of the EM9201. The parameters defined in this paragraph are specified based on the component list defined in Table 1.1 and on application schematic of Figure 1.2 from the power management point of view and all considerations described in section 5.1. Unless otherwise specified, the voltage VCC2 is set to 2.5V, typical values are stated at room temperature (T=25°C) and measured RF channel is 19 (2.44 GHz).

2.5.1 General Characteristic

Parameter	Notes	Min	Typ	Max	Unit
Operating frequencies		2400		2484	MHz
Differential antenna impedance			200		Ω
Data Rate			1000		kbps
Channel spacing			2		MHz
Frequency deviation			±250		kHz
Crystal frequency			26		MHz
Crystal frequency tolerance [4]			±30		ppm
Spurious emission in stand-by mode for $f \leq 1$GHz	[5]		-57		dBm
Spurious emission in stand-by mode for $f > 1$GHz	[5]		-47		dBm

2.5.2 Transmitter Operation

This section describes the RX performances of EM9201. All Measures are based on packet error rate (PER) with a wanted signal packet of 128bit on channel 19 (2.440 MHz). All spurious and adjacent power are measured for the output power 0 dBm.

Parameter	Notes	Min	Typ	Max	Unit
Output Power		-20	0	+2	dBm
Number of output power steps			8		
RF power accuracy			±3		dB
Transmit power @ 2 MHz offset				-20	dBm
Transmit power @ 3 MHz offset				-30	dBm
Spurious emission in operating mode for f in the ranges 47MHz – 74MHz 87.5MHz – 118 MHz 174MHz – 230MHz 470MHz – 862MHz	[5]		-54		dBm
Spurious emission in TX mode for other $f \leq 1$GHz	[5] [6]		-36		dBm
Spurious emission in TX mode for other $f > 1$GHz	[5] [6]		-30		dBm

2.5.3 Receiver Operation

This section describes the RX performances of EM9201. All Measures are based on packet error rate (PER) with a wanted signal packet of 128bit on channel 19 (2.440 MHz). In case of in band blocking, interferer signal is a PRBS9 signal. In case of out of Band blocking the interferer signal is a CW. In both cases the wanted signal power is defined as -77dBm.

---

[4] The specified frequency drift includes initial frequency tolerance of the crystal, temperature stability, aging effects and tolerance of external components.

[5] Measuring conditions and signals specifications are described on ETSI EN 300 440-1 V1.3.1 (2001-09) TX and RX section

[6] This parameter is highly dependent on the quality of components building up the antenna and antenna matching network. In order to achieve the best performances, high quality RF components are advised.

Parameter	Notes	Min	Typ	Max	Unit
Sensitivity for 0.1% BER			-83		dBm
Spurious emission in RX mode for 30MHz < *f* < 1GHz	5 6		-57		dBm
Spurious emission in RX mode for *f* > 1GHz	5 6		-47		dBm
Out of band blocking for 30MHz < *f* < 1999MHz	5 6		-30		dBm
Out of band blocking for 2000MHz < *f* < 2399MHz	5 6		-35		dBm
Out of band blocking for 2484MHz < *f* < 2999MHz	5 6		-35		dBm
Out of band blocking for 2999MHz < *f* < 12750MHz	5 6		-30		dBm
C/I ratio for the co-channel interferer			21		dB
C/I ratio for ±1 MHz offset interferer			15		dB
C/I ratio for ±2 MHz offset interferer			-17		dB
C/I ratio for f ≥ +3 MHz offset interferer			-27		dB
C/I ratio for -3 MHz offset interferer			-12		dB
C/I ratio for -4 MHz offset interferer			-5		dB
C/I ratio for -5 MHz offset interferer			-12		dB
C/I ratio for f ≤ -6 MHz offset interferer			-27		dB

2.6 Timing Characteristics

This section summarizes the timing characteristics of the EM9201. The parameters defined in this paragraph are specified based on the component list defined in Table 1.1 and on application schematic of Figure 1.2 from the power management point of view and all considerations described in section 5.2. Unless otherwise specified, the voltage VCC2 is set to 2.5V, typical values are stated at room temperature (T=25°C) and typical characteristic of xtal TSS-3225A.

Parameter	Symbol	Min	Typ	Max	Unit
RX↔TX in same channel	Trx_tx		150		µs
Stand-by Mode → TX/RX Mode(transmission)	Tstdb_rf		150		µs
PLL lock time	Tpll_lock			100	µs
Start up [7]	Tpd_std		10	25	ms
Power down to standby mode [7]	Txt_std		1	10	ms

[7] This parameter is highly dominated by the Xtal oscillator start-up time, which strongly depends on Quartz Q-factor. Typical values are for NX3225SA with typical load capacitors. Maximum are stated for NX3225SA with significant margin for Q-factor and capacitors spreading.

3. Functional description

3.1 EM9201 Start-up

This section describes the start-up phase of the EM9201. This description is intended to be informational only as it is independent of any external actions.
When a battery is connected to the pin VCC2, the regulated digital supply ramps up quickly and an internal RC oscillator is turned-on, providing a clock to the power-check circuit. If the latter indicates enough supply, the Xtal oscillator is enabled and, after a certain time dependent on the crystal, an interrupt on the IRQ pin is released, indicating that the start-up procedure has finished. The RC oscillator, used to allow a reliable Xtal start-up, is stopped once this is completed started.

3.2 Functional Modes

This paragraph describes the modes EM9201 can operate in and the procedure needed to change from a mode to another. Figure 3.1 shows a EM9201 state diagram. As described in §3.1, EM9202 becomes functional at the end of the start-up procedure. The default state is stand-by. An SPI transaction allows the host to change the state. Some of the transitions are also automatic, e.g. for a one-shot transmission.

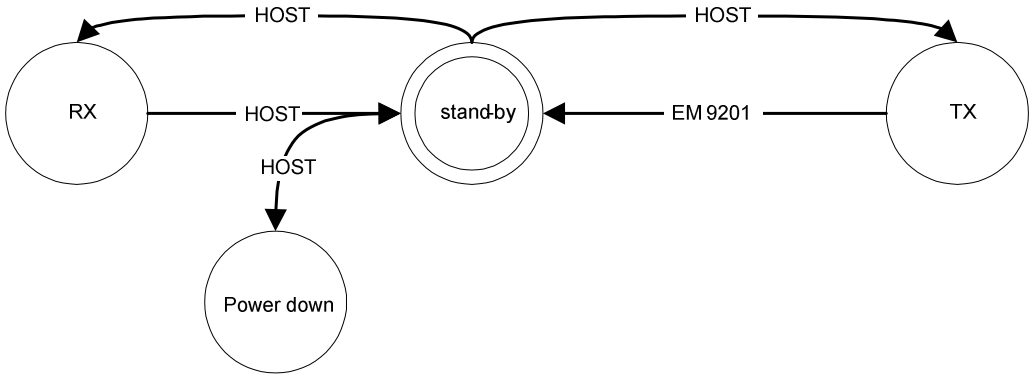


Figure 3.1: Simplified system state diagram.

3.2.1 Standby mode

This is the default mode into which the EM9201 goes after reset, and the starting point for any RF operation (transmission / reception) or activation of special power-management modes (power down mode). In this case, only the Xtal oscillator is running.

3.2.2 Power down mode

In order to minimize the power in idle case, the EM9201 can be set into a very low consumption mode. In Power done mode, all on-chip clocks are disabled and the power consumption of the regulated digital supply is minimized. While in normal operation the voltage level seen on the VDD-pin is around 1.8V, it's now reduced to around 1.2V such that off-state leakage is reduced. All register values in the SPI interface are kept. This mode is enabled by an SPI command (`PowerMgt.Xtreme` = 1) .

3.2.3 Standby low power

EM9201 also provides a second standby mode, where the current consumption of the only active Xtal-oscillator is reduced and the main system clock is set to around 400 kHz. This mode is complementary to the Power down mode since here the accurate time-base due to the Xtal oscillator is kept. However, the Standby low power mode is much less effective in terms of current savings. This mode is enabled by an SPI command (`PowerMgt.LowPwrStdBy = 1`) .

3.2.4 TX Mode

When in TX mode, EM9201 can send a packet over the air. To achieve this, EM9201 first sets all parameters of the radio core in TX State and then it modulates the digital signal to be transmitted. After a complete packet transmission, EM9201 can enter the following configurations (refer to § 3.3 for a detailed description):

- EM9201 goes in standby mode, if auto acknowledge mode is not selected
- EM9201 switches in RX mode to receive an acknowledgement, if the auto acknowledgement mode is selected.

TX mode can be only accessed from the standby mode. The timing required to achieve correct RF-operation at the antenna port is not longer than the time specified in `RFTiming.RFStUpTim` register. This timing is mainly determined by the settling time of the PLL in the frequency synthesizer.

3.2.5 RX Mode

When in RX-mode, EM9201 can receive GFSK-modulated signals. In this mode the radio core is set in RX state until no request of the host to exit RX mode is received. If auto acknowledge mode is selected, upon each reception of a correct packet, EM9201 switches to TX mode to send an acknowledgment.
This mode can only be activated from the standby mode. The timing required to achieve correct reception of a packet is not longer than the time defined in `RFTiming.RFStUpTim` register.

3.3 Radio core

EM9201 features a highly integrated, multi-channel RF transceiver for wireless applications in the 2.4GHz worldwide ISM frequency band. The robust low-IF architecture and the direct GFSK modulation scheme are not only designed for proprietary communication protocols, but also to be compatible with the emerging Bluetooth Low Energy Wireless standard. A raw on air date rate of 1Mbps is supported for up to 40 channels. The digital GFSK-modulation and -demodulation is performed using a bit-bandwidth product (BT) of 0.5 and a modulation index of 0.5
The radio core can be programmed to be in two main states:

- TX state: the whole transmit-chain is active and the digital baseband data can be up-converted to a 2.4GHz GFSK modulated signal
- RX state: the frequency synthesizer and the whole RX-chain are active and ready to receive a packet.

3.3.1 Frequency synthesizer (PLL)

The frequency synthesizer provides accurate and low jitter 2.45 GHz RF signal used both for the up-conversion process in TX state and for the down-conversion of an on-air RF signal in RX state. Both in TX and RX, 40 different channels can be used. In order to support direct GFSK- modulation in transmit-operation with low frequency drift, a closed loop modulation approach is implemented. To avoid drift due to temperature variations, an auto-calibration mechanism is included in the PLL to proper center the VCO control voltage.

3.3.2 RX chain

The EM9201 Rx chain is based on a typical low-IF architecture implying a low noise resonant RF-amplifier (LNA), followed by a down-conversion mixer and a poly-phase IF-filter. The output of the IF-filter is converted into a square wave using a high gain limiting amplifier. The digitalized I/Q signals stimulate a digital GFSK-demodulator which provides the received packet data and status information. This information is finally processed by the digital baseband.
The RX-chain also features a receive-signal-strength indicator (RSSI), which can measure the power of the down-converted RF signal after the IF-filter. The averaged value of this power can be read through the SPI after the single-shot RSSI measurement has been completed (see §4.10).
The relationship between the applied RF-power Pin and the value given by the RSSI can be expressed as follows:

$$Pin\ [dB] = -50dBm - (10 - RFRSSIOut[3:0]) * 5dB$$

where is RFRSSIOut[3:0] is the 4-bit value of the RFRSSI register. The measured input power has a tolerance ±3dB.

3.3.3 TX-chain

The TX chain features a GFSK modulator implemented by direct modulation of the frequency synthesizer. A high efficiency Power Amplifier (PA) guarantees the required power at the output stage.
The PA output power can be adjusted in 8 levels as reported in Table 3.1. all values are Measured with vcc2 = 2.5V, T=25°, load impedance = 200 Ohm. These levels can be set by the `RFPwr[2:0]` bits of the `RFSetup` register.

RF Power (RFPwr[2:0])	Output power	DC Current consumption
111	+2 dBm	17.9 mA
110	0 dBm	12.9 mA
101	-3 dBm	11.4 mA
100	-6 dBm	10.4 mA
011	-9 dBm	9.6 mA
010	-12 dBm	9.2 mA
001	-16 dBm	8.8 mA
000	-20 dBm	8.6 mA

Table 3.1: RF power setting of the EM9201.

3.3.4 Air data rate

The EM9201 has a fixed data rate of 1Mbit per second (Mbps).

3.3.5 Channel frequency

EM9201 can send/receive data in up to 40 channels. The wanted channel can be set using the `RFChannel` register. `RFChannel` shall be a value in between 0 and 39. If a value greater than 39 is set the channel will be coerced to 39. The center frequency of each channel is defined as:

$$F_c = 2402 + \texttt{RFChannel} * 2$$

To be able to establish a communication both devices of a link shall be set on the same channel.

3.4 Baseband

The Baseband processor is the EM9201 central digital control system. It handles all states of the chip including SPI transactions and radio operations. Furthermore, it configures digital data for transmission as well as it processes packets received from the demodulator – generally all what is referred to 'Link layer'. EM9201 is able to send and receive each packet according to the host command. When EM9201 is configure in TX mode, it will send a packet in a burst, wait for an acknowledge packet from the other part (acknowledge system is active per default. To deactivate it refer to Register ACKSetup (0x0B)). After that EM9201 goes in stand-by mode and the host controller will be able to set the EM9201 for other operations. In case auto the acknowledgment system is active, EM9201 will also deal automatically with any re-transmission in case of bad acknowledge or absence of acknowledge. The acknowledge concept is described in Figure 3.2.

In RX mode the EM9201 will wait for any packet on the given frequency, and verify the address, flag and CRC, then send a acknowledgement (if acknowledgement system is active), and go back in reception until the host controller change the EM9201 mode to stand-by.

In the following paragraphs, some c code is used to describe the basic functions of the EM9201. In particular it is assumed that the user implements a function `EM920xWrite` which writes an EM9201 register using SPI interface as described in 3.7.

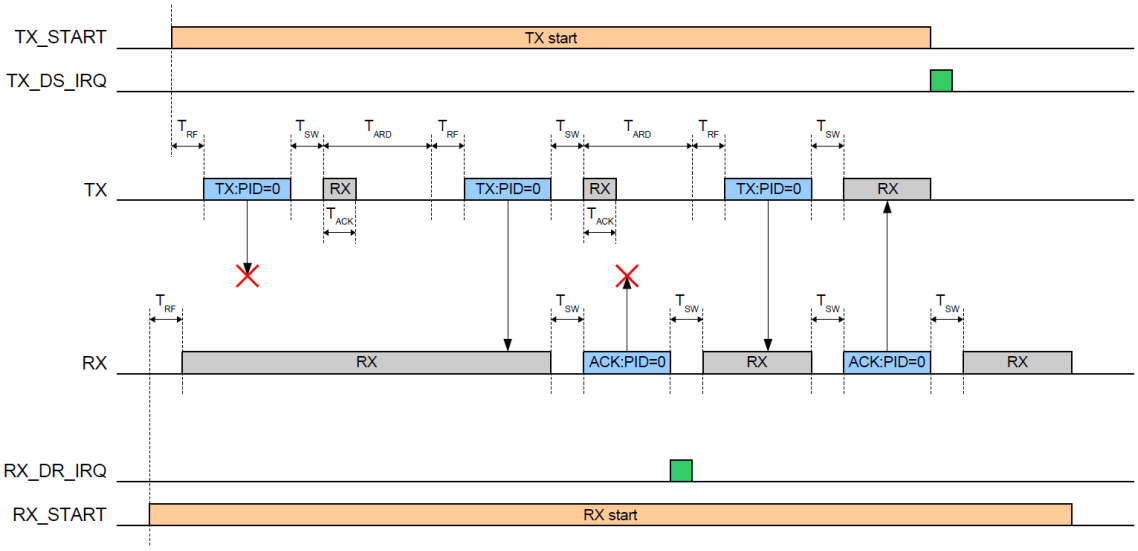


Figure 3.2: Auto-Acknowledge procedure

3.4.1 Auto-calibration flow

For a correct transmission and reception, the PLL shall be calibrated before any data transmission attempt. It is mandatory to execute the auto-calibration procedure only on channel 19. To request an auto-calibration the `RFSetup.AutoCalib` bit shall be set to 1. This bit goes back to 0 at the end of the auto-calibration. The calibration procedure is then automatically controlled by the PLL. The auto-calibration procedure can be considered finished when `Int2Sts.IntStsAutoCalEnd` bit is set to 1. This bit can be optionally transferred to the IRQ pin by masking the auto-calibration interrupt by writing 1 to the register `Int2Msk.IntMskAutoCalEnd`. Note that the last interrupt also appears during a normal transmit or receive operation, as it indicates that the PLL has completed its set-up procedure. In these two cases, it can be safely ignored.

The characteristic of the PLL can slightly differ depending on the temperature, thus it is advised to request the start of an auto-calibration procedure from time to time.

3.4.2 Transmission flow

To send a packet using the EM9201, host shall follow the following procedure:

- Select the channel to be used by writing in register `RFChannel`. The value shall be a number in the range 0..39. Any bigger value will be coerced to 39.
- Configure the output power by writing in register `RFSetup` the desired value as described in 4.7.
- Configure the RF startup timings by writing the desired value as described in 4.9. This step is optional
- Define the own and peer address as described in 4.13 and 4.15.
- Clear all interrupts by writing 0xFF in register `Int1Sts` and `Int2Sts`
- Configure the interrupt mask to transfer interrupt TXDS to IRQ by writing in registers `Int1Msk` and `Int2Msk` the appropriate value defined in 4.3 and 4.4.
- Configure the acknowledgment system as described 4.12. This step is optional.
- Configure the number of allowed retransmissions. This step is needed only ack system is active.
- Set packet length by writing a value in register `TxPayloadLength`
- Write up to `TxPayloadLength` byte into the TX FIFO registers as described in 4.23
- Increment TX FIFO pointer by writing 0x80 in Register `FIFOCtrl`.
- Set the `Config.Start` and `Config.TxRxn` bits to 1.

The following procedure can be used as example of host code:

```
void start_tx()
{
        //set communication Channel. Eg channel 19
        EM920xWrite(RFChannel, 19);

        //set ouput power. Eg 0dBm
        EM920xWrite(RFSetup, 0x16);

        //set RF startup time. Eg 150us
        EM920xWrite(0x08, 0xAD);

        //set own address Eg 0x12005F
        EM920xWrite(0x0E, 5F); // the four least significant bits shall be set to b1111
        EM920xWrite(0x0F, 00);
        EM920xWrite(0x10, 12);
        //Set peer address. Eg 0x12345F
        EM920xWrite(0x11, 5F); // the four least significant bits shall be set to b1111
        EM920xWrite(0x12, 34);
        EM920xWrite(0x13, 12);

        //Clear all interrupts
        EM920xWrite(0x00,0xFF);
        EM920xWrite(0x01,0xFF);

        // Configure IRQ on txDS and MaxRT
        EM920xWrite(Int1Msk, 0x60);
        EM920xWrite(Int2Msk, 0x00);

        // Configure ACK. Eg set ACK timing to 110us
        EM920xWrite(0x0B, 0x08);

        // configure maximum retransmissions
        EM920xWrite(0x0C, 0x7F);

        // set payload length. Eg 8 bytes
        uint8_t Payload_Len = 7; // this is always want payload len - 1
        EM920xWrite(0x14, Payload_Len);

        for (int I = 0; I < Payload_Len; I++)
        {
            EM920xWrite(I + 0x40, data_to_be_sent[I]);
        }

        // increment TX FIFO
        EM920xWrite(0x16, 0x80);

        // Send Data
        EM920xWrite(0x04, 0x03);
        WaitIRQ()
}
```

The last procedure will:

- Power up the radio system and set it up to transmit at the given frequency
- Send the packet in one burst at the given data rate
- If ack system is active it will enter in receiver state and wait for the acknowledge packet

- Signalize to host using IRQ pin whether the packet was or not sent correctly. In case ack system is active the interrupt will be released only if the ack was also received correctly.
- If the ack system is active, and a NACK was received, EM9201 will increments the auto retransmission counter. When the number of retransmission set in `MaxRT` register have been reached, EM9201 goes on stand-by setting the MAX_RT interruption.

3.4.3 Reception flow

To receive a packet using the EM9201, host shall follow the following procedure:

- Select the channel to be used by writing in register `RFChannel`. The value shall be a number in the range 0..39. Any bigger value will be coerced to 39.
- Configure the RF startup timings by writing the desired value as described in 4.9. This step is optional
- Define the own and peer address as described in 4.13 and 4.15.
- Clear all interrupts by writing 0xFF in register `Int1Sts` and `Int2Sts`
- Configure the interrupt mask to transfer interrupt RXDR to IRQ by writing in registers `Int1Msk` and `Int2Msk` the appropriate value defined in 4.3 and 4.4.
- Configure the acknowledgment system as described 4.12. This step is optional.
- Set the `Config.Start` and `Config.TxRxn` bits to 0.
- Wait for interrupt
- Read `RXPayloadLenght` Register to determine the length of the received packet
- Read up to `RXPayloadLenght` Data from RX FIFO as described in 4.24
- Increment RX FIFO pointer by writing 0x40 in Register `FIFOCtrl`.

```
void start_rx(void)
{
        //set RF Channel. Eg channel 19
        EM920xWrite (0x07, 19);

        //set RF startup time. Eg 150us
        EM920xWrite (0x08, 0xAD);

        //set device address /peer address. Eg 0x12345F
        EM920xWrite (0x0E, 5F);
        EM920xWrite (0x0F, 34);
        EM920xWrite (0x10, 12);
        //Set peer address. Eg 0x12005F
        EM920xWrite (0x11, 5F);
        EM920xWrite (0x12, 00);
        EM920xWrite (0x13, 12);

        //Clear interrupts
        EM920xWrite (0x00,0xFF);
        EM920xWrite (0x01,0xFF);

        // Configure IRQ on Data received
        EM920xWrite (0x02, 0x80);

        // Configure ACK. Eg Disable ACK
        EM920xWrite (0x0B, 0x1D);

        // Put the device in RX mode
        // data reception possible after RFStartupTime
        EM920xWrite (Config,0x02);

        If (IRQ())
        {
                //read the packet length and the RX FIFO
                U8 len, data[31];
                SPI_read(0x15, &len);
                for (int I = 0; I < len; I++)
                {
                        SPI_read(0x60 + I, data[I]
                }
                // increment FIFO pointer
                EM920xWrite (0x16, 0x20);
                //Clear interrupts
                EM920xWrite (0x00,0xFF);
                EM920xWrite (0x01,0xFF);
        }
}
```

The last procedure will:

- Power up the radio in RX on the given channel
- Wait for an incoming packet.

- If an incoming packet is detected, EM9201 checks the address and CRC. If both are valid EM9201 assert IRQ to indicate to the host that a valid packet has been received.
- If ack system is enabled, EM9201 automatically acknowledges the TX that the packet was correctly received.
- If a valid packet was received, EM9201 stores the payload received in the registers starting from registers RX FIFO (0x60 to 0x7F). The payload length is stored in Register RXPayloadLength (0x15). Host MCU shall read the latter register to know how many bytes shall be taken from the RX FIFO registers.
- Host MCU can stop the reception by setting Config.Start bit to 0.

3.4.4 Packet format

EM9201 air packet is depicted in Figure 3.3. Each packet contains the following information:

- Preamble: it is used to synchronize the received packet and extrapolate the symbol rate. The preamble is "01010101" if the address LSB is 0, 1 otherwise. The preamble is remove from the data stream.
- Address: it contains the address of the peer device. The receiving device compares its own address with the address found in the packet and only if both are the same, the packet is accepted. The address is 3 bytes long but it is mandatory to set the last the four least significant bits of the address to b1111. To improve the receiver performance it is advised to avoid long sequences of 0's and/or 1's. The address is removed from the data stream.
- Flags: it includes a 2 bit packet identifier (PID), 1 bit defining if the packet is a data packet or an ack packet and 5 bit which define the payload length.
- Payload: it is a 1 to 32 byte wide data stream
- CRC: it is used to verify the integrity of the received packet. The CRC polynomial is $x^{16} + x^{12}+x^5+1$

Multi byte data are always sent on-air LSByte first and each byte is sent the LSBit.

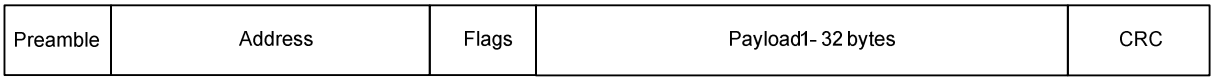


Figure 3.3: Typical EM9201 on air packet

The structure of the acknowledge packet is very close to the normal packet except that no data are present.

An acknowledgement packet may acts as an ACK or NACK. If the received CRC differs from the expected on, the received packet will be understood as a NACK otherwise it will be interpreted as an ACK packet.

3.4.5 Packet Identifier

Each packet contains a two bit wide PID field which is used, together with the CRC field, to detect if the received packet is new or resent. The PID will prevent that the RX device reports the same payload more than once to the host. The scheme of PID generation and detection is depicted in Figure 3.4

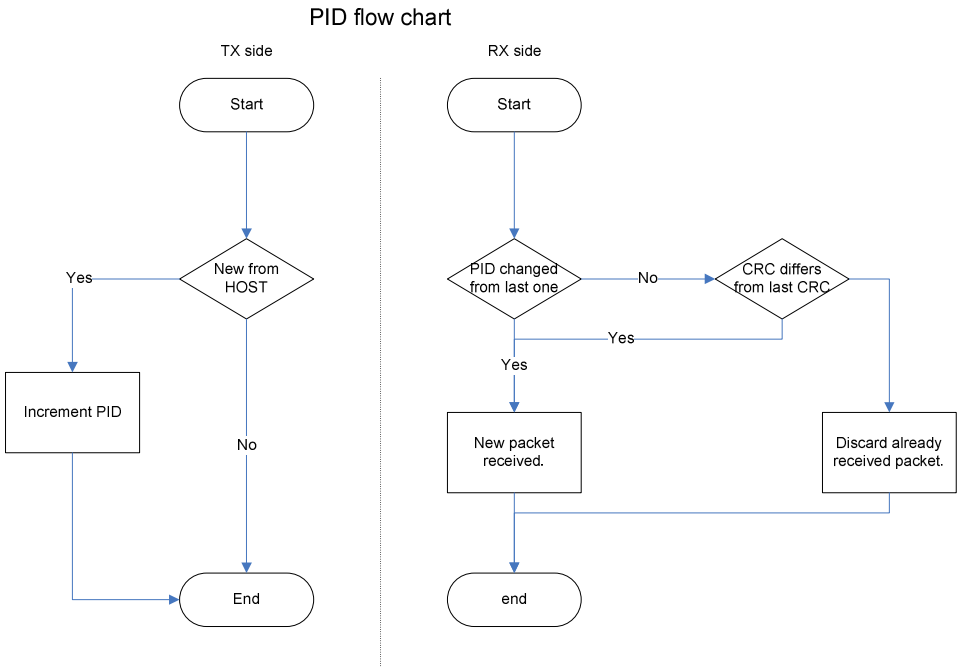


Figure 3.4: PID generation and detection

3.5 Power management

The power management system of the EM9201 provides the necessary supplies, voltage/current references and timing circuitry for reliable operation in all modes of operations. This includes all required low drop out voltage regulators (LDO) for the RF-core and the whole digital part, a low noise band-gap and a bias-generator. An external resistor is used to provide a reliable current reference in all operating conditions. All these circuits are powered through the VCC2 pin.

3.5.1 RF-core supplies

All analog parts in the RF-core are supplied using two fully integrated LDOs, one needed both for the RX and the TX chain and one used for the frequency synthesizer (PLL). An additional and dedicated regulator is implemented to provide a stable supply for the power amplifier. In order to ensure a good compromise between noise and stability, an external 4.7nF decoupling capacitor is required. The voltage reference for these three regulators is derived from a low noise band-gap circuit. In order to optimize the current consumption in any mode of operation, the regulators as well as the band-gap/bias are enabled individually when needed by an automatic flow chart both in TX and RX mode.

3.5.2 Digital supply

The supply for all digital parts (VDD) in the system is provided by a low power LDO and a second reference circuit. This assures that the logic is powered throughout the whole time of operation including the power-down modes described in §3.2.2. This regulator uses an external decoupling capacitor of 220nF.

3.5.3 Bias generator

In order to create a stable and temperature independent current reference for the RF-core, EM9201 features a bias generator based on an external 27 kΩ resistor and the on-chip band-gap reference. The spread of the current consumption in transmit/receive operation depends highly on the external resistor; therefore it is recommended that its tolerance is maximum +/- 2%.

3.6 Supply monitoring

EM9201 offers the possibility to monitor the supply voltage. The host-controller can launch a measurement by sending the appropriate SPI command. Once selected the desiderate comparison voltage level, EM9201 compares the supply node voltage with the selected level and returns 1 it the supply is above the reference level once the measurement is completed. The result (1 bit) can be read back from the SVLD register through SPI. It is recommended to repeat several times the measurements in order to reduce inaccuracies due to noise.

3.7 SPI interface

The EM9201 control interface is a 4-wire SPI bus with interrupt information. The four wires are described as below:

- CSN: Chip selected. This pin is active low
- SCK: Serial clock
- SDI: Serial data in (EM9201 view), also called MOSI.
- SDO: Serial data out (EM9201 view) also called MISO

EM9201 SPI interface is a byte based interface. This means that at least one byte of data shall be sent through the interface. Each byte shall be sent MSB first.

Table 3.2 specifies the general conditions for all SPI pins. All values specified in the following paragraphs are assuming a load capacitor of 15pF. Unless otherwise specified, the voltage VCC2 is set to 2.5V. Typical values are stated at room temperature (T=25 °C)

Parameter	Symbol	Min	Typ	Max	Unit
HIGH level input voltage	V_{IH}	0.7*Vcc2		Vcc2+0.2	V
LOW level input voltage	V_{IL}	-0.2		0.3*Vcc2	V
HIGH level output voltage	V_{OH}	Vcc2-0.3		Vcc2	V
LOW level output voltage	V_{OL}	0		0.3	V
Source current			2.5		mA
Sink current			2.5		mA

Table 3.2: Digital pin specifications

3.7.1 SPI transaction

A typical raw SPI transaction is depicted in Figure 3.5. Each change on SDI is latched on the rising edge of SCK, and each change on SDO is done on the falling edge of SCK. An SPI transaction is defined by all the changes of SCK, SDI and SDO in between a falling edge of CSN and its next rising edge.

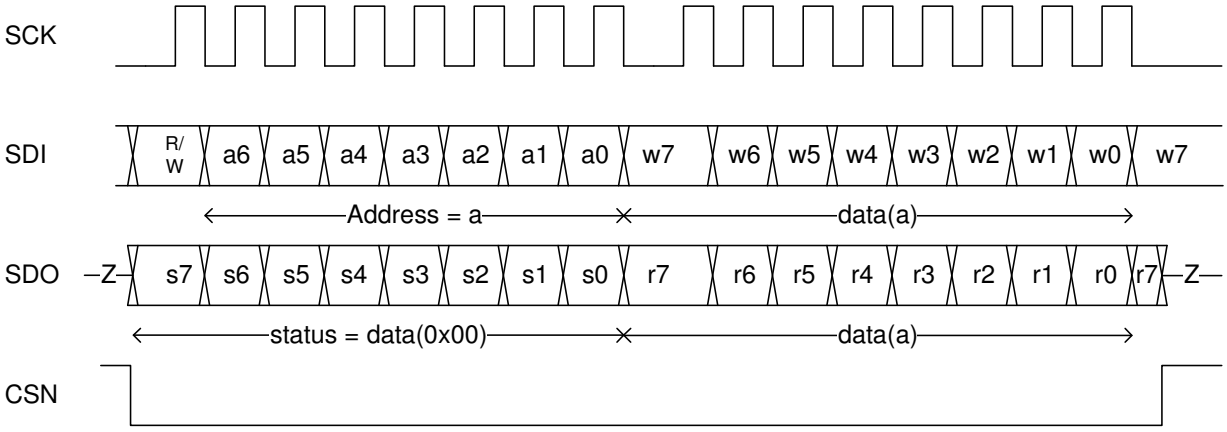


Figure 3.5 Raw SPI transaction

A transaction shall have a multiple of 8 SCK pulses to be complete. In case of incomplete transactions, only the complete bytes will be taken in account.

With SPI, it is possible to achieve the following actions:

- Read one or more consecutive register(s) and the status byte (register 0x00) (see Figure 3.6 below). This action needs at least 2 bytes (1 for address and read order, and 1 byte for reading the desired address.
- Write one or more consecutive register(s) and read the status byte (register 0x00) (see Figure 3.7 below). This action needs at least 2 bytes (1 for address and write order, and 1 byte for writing at the desired address.
- Read status byte. This action needs 1 byte.

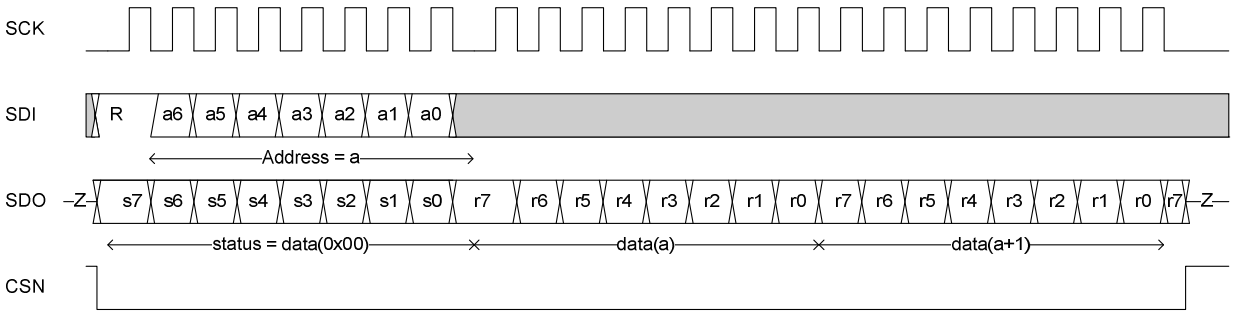


Figure 3.6 Multi-read SPI transaction

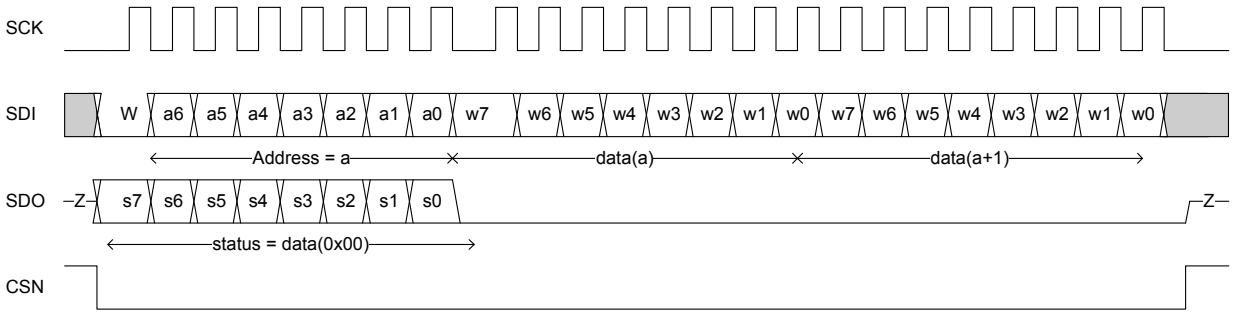


Figure 3.7 Multi-write SPI transaction

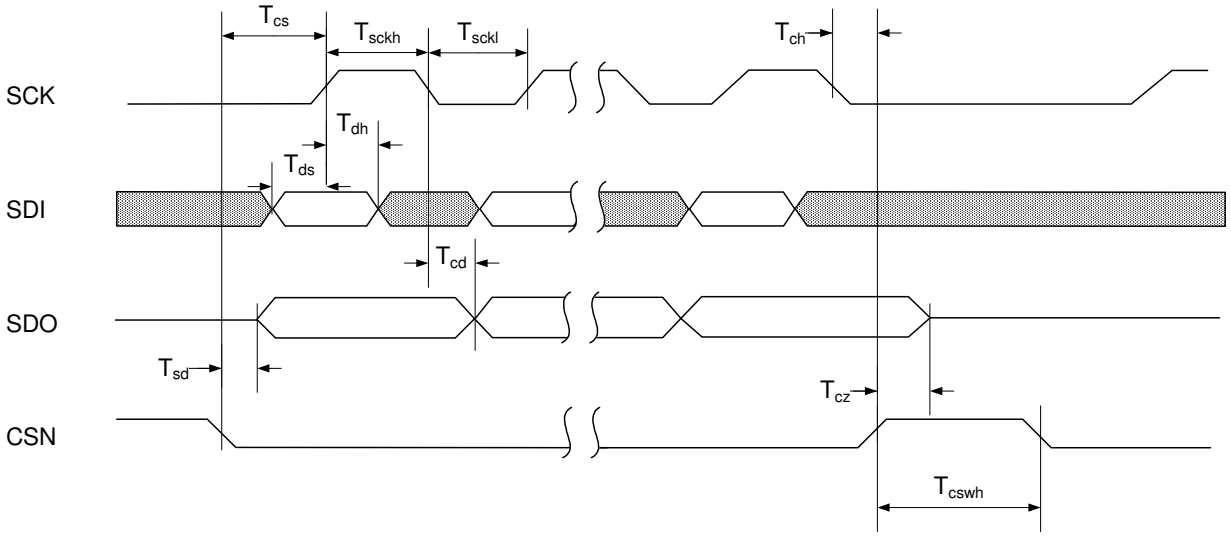


Figure 3.8 SPI timing diagram

Symbol	Parameters	Min	Max	Units
T_{ds}	Data to **SCK** Setup	5		ns
T_{dh}	**SCK** to Data Hold	5		ns
T_{sd}	**CSN** to Data Valid		30	ns
T_{cd}	**SCK** to Data Valid		30	ns
T_{sckl}	**SCK** Low Time	40		ns
T_{sckh}	**SCK** High Time	40		ns
F_{sck}	**SCK** Frequency	0	8	MHz
F_{sck_lp}	**SCK** Frequency in low power modes	0	1	MHz
T_{cs}	**CSN** to **SCK** Setup	125		ns
T_{ch}	**SCK** to **CSN** Hold	125		ns
T_{cswh}	**CSN** Inactive time	125		ns
T_{cz}	**CSN** to Output High Z		30	ns

Table 3.3: SPI timing values.

3.8 Interrupt flag

EM9201 has an active high interrupt pin (IRQ). This pin is activated when a bit of registers 0x00 or 0x01 goes high and the corresponding interrupts mask available in registers 0x02 and 0x03 are set to high. Note that the interrupt mask is only needed to transfer the values of registers 0x00 and 0x01 to the IRQ. The values the latter registers have is only dependent on the internal state of EM9201 and cannot be influenced by host. The value of register 0x00 is also directly visible as status information at each SPI transaction.
Each bit of any interrupt register can be cleared by writing 1 on it . If 0 is written the register value is kept

3.9 Bridge

The bridge mode provides a direct access to the physical part through the SPI interface and two dedicated pads. SPI is used to configure the physical layer whereas the two specific pads are dedicated to stream in/out a clock and data for a transmitted/received stream. The bridge mode can be used to emulate a proprietary link layer with the aid of an external component (MCU, FPGA, or ASIC) to use the GFSK modem and/or the power management features.

A more detailed description of the bridge mode features can be made available upon special request.

3.10 Software reset

The EM9201 can be reset using SPI. In reset condition, all registers take the default value indicated in the attached register map. After each reset, it is mandatory to run an auto calibration procedure.

To reset the EM9201 it is needed to write into the register `SwReset` two different values (0xB3 followed by 0x5E), in two consecutive SPI transactions. The EM9202 software reset procedure is as follow:

```
void EM920xSwReset() {
       EM920xWrite(SwReset,0xB3)
       EM920xWrite(SwReset,0x5E)
}
```

3.11 RSSI measurement

EM9201 includes a RSSI (receiver signal strength indicator) which may help to analyze how polluted is the receiving channel the EM9201 is set. By launching the RSSI measure, EM9201 measure the received power present on the selected channel. A user algorithm may use this information to choose a good channel for communication.
The following code can be used as example to launch the RSSI measurement.

```
U8 rssi_measure()
{
```

```
        U8 rssiVal;
        // enable RSSI function and trigger RSSI measurement
        EM920xWrite (0x09,0x10);
        // wait ~80 us for measurement to be performed
        // read RSSI value
        EM920xWrite (0x09, &rssiVal);
        // disable RSSI
        EM920xWrite (0x09,0x00);
        return (0x0F & rssiVal);
}
```

4. Registers

In this section all relevant registers of the EM9201 are described, i.e. their basic functionality and reset values. Any register not specifically mentioned here is a reserved one.

4.1 Register Int1Sts (0x00)

As described in 3.8, each of the interrupt can be cleared by writing 1 on the dedicated bit.

Mnemonic	Bit	type	Reset Value	Description
IntStsRxDr	7	R/W	0	When set means that a packet has been received
IntStsTxDS	6	R/W	0	When set means that a packet has been sent
IntStsMaxRT	5	R/W	0	When set, the maximum number of retransmission in TX mode has been exceeded
Reserved	4	R/W	0	Shall be always rewritten with a 1
Reserved	3	RO	0	Shall be always rewritten with a 1
IntStsPwrLow	2	R/W	0	SVLD Power check. Indicates that the SVLD measurement has finished if the value of bit SVLDIntOnFail in register SVLDCtrl is not set. In case the bit SVLDIntOnFail is set, this interrupt is set only if the measured voltage is below the chosen reference voltage.
IntStsXtalHiPwr	1	R/W	0	When set means that Low power stand-by was exited.
IntStsXmEnd	0	R/W	0	When set means that the power down mode was exited.

4.2 Register Int2Sts (0x01)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:2	-	b000000	Only b000000 allowed.
IntStsRstFlg	1	R/W	0	Reset flag. This interrupt cannot be deactivated
IntStsAutoCalEnd	0	R/W	0	RF Auto calibration procedure finished

4.3 Register Int1Msk (0x02)

By setting one of the following bits, the relative interrupt stored in register (0x00) will be transferred to the IRQ pin.

Mnemonic	Bit	type	Reset Value	Description
IntMskRxDR	7	R/W	0	Transfer interrupt RxDR to IRQ
IntMskTxDS	6	R/W	0	Transfer interrupt TxDS to IRQ
IntMskMaxRT	5	R/W	0	Transfer interrupt MaxRT to IRQ
Reserved	4	R/W	0	This bit shall be set to 0
Reserved	3	R/W	0	This bit shall be set to 0
IntMskPwrLow	2	R/W	0	Transfer interrupt PwrLow to IRQ
IntMskXtalHiPwr	1	R/W	0	Transfer interrupt XtalHiPwr to IRQ
IntMskXmEnd	0	R/W	0	Transfer interrupt XmEnd to IRQ

4.4 Register Int2Msk (0x03)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:1	-	b0000000	Only b0000000 allowed.
IntMskAutoCalEnd	0	R/W	0	Transfer interrupt Auto Calibration finished to IRQ

4.5 Register Config (0x04)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:6	-	b00	Only b00 is allowed.
WhitDis	5	R/W	0	Disable the whitener
Reserved	4	-	0	Only 0 is allowed.
RxRestart	3	R/W	0	Restart packet reception
TxCont	2	R/W	0	Enable continuous transmission in TX mode

Mnemonic	Bit	type	Reset Value	Description
Start	1	R/W	0	Starts RF operation set by TxRxn bit
TxRxn	0	R/W	0	Set the RF operational mode, 0 means RX, 1 means TX

4.6 Register PowerMgt (0x05)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:2	RO	b000000	Shall be always set to b000000
Xtreme	1	R/W	0	Switches the Power down mode on/off
LowPwrStdBy	0	R/W	0	Switches the Low power stand-by mode on/off

4.7 Register RFSetup (0x06)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:6	-	b00	Only b00 allowed.
RFAutoCal	5	R/W	0	Start PLL auto-calibration procedure
Reserved	4	R/W	1	Shall be always set to 1
Reserved	3	R/W	0	Shall be always set to 0
RFPwr	2:0	R/W	b110	Set RF output power in TX mode 000 – -20 dBm 001 – -16 dBm 010 – -12 dBm 011 – -9 dBm 100 – -6 dBm 101 – -3 dBm 110 – 0 dBm 111 – +2 dBm

4.8 Register RFChannel (0x07)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:6	-	b00	Only b00 allowed.
RFChannel	5:0	R/W	b00000	Channel number in which the device operates on (allowed values are in the range 0…39 in decimal format)

4.9 Register RFTiming (0x08)

All values not specified in this table are to be considered as no allowed

Mnemonic	Bit	type	Reset Value	Description
RFStUpTim	7:4	R/W	0xA	Defines the RF start-up time 0101 – 100 µs 0110 – 110 µs 0111 – 120 µs 1000 – 130 µs 1001 – 140 µs 1010 – 150 µs (default) 1011 – 160 µs 1100 – 170 µs 1101 – 180 µs 1110 – 200 µs 1111 – 250 µs
RFSwTim	3:0	R/W	0xD	Defines the RF RX/TX switching time 1000 – 100 µs 1001 – 110 µs 1010 – 120 µs 1011 – 130 µs 1100 – 140 µs 1101 – 150 µs(default) 1110 – 160 µs 1111 – 170 µs

4.10 Register RFRSSI (0x09)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:5	-	b000	Only value b000 is allowed.
RFRSSIEn	4	R/W	0	Start RSSI measure
RFRSSIOut	3:0	RO	0x0	Result of RSSI power measure

4.11 Register ACKSetup (0x0B)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:5	-	b000	Only b000 allowed.
ACKDis	4	R/W	0	Auto-acknowledge disable
ACKTimeout	3:0	R/W	0xD	Timeout for waiting for acknowledge 1000 – 110 µs 1001 – 120 µs 1010 – 130 µs 1011 – 140 µs 1100 – 150 µs 1101 – 160 µs(default) 1110 – 170 µs 1111 – 180 µs

4.12 Register RetrSetup (0x0C)

Mnemonic	Bit	type	Reset Value	Description
ARDly	7:4	R/W	0x7	Auto Re-transmit Delay. Sets up the timing between the end of actual transmission and the start of the next one. 0x0 – Wait for 250µs 0x1 – Wait for 500µs 0x2 – Wait for 750µs ..... 0x7 – Wait for 2000µs (default) ..... 0xF – Wait for 4000µs
ARCntMax	3:0	R/W	0x3	Auto Retransmit Count. Defines the maximum number of allowed retransmissions. 0x0 – Re-transmit disabled 0x1 – Up to 1 re-transmit ..... 0xF – Up to 15 re-transmit

4.13 Register RetrStatus (0x0D)

Mnemonic	Bit	type	Reset Value	Description
LstPckCnt	7:4	RO	0x0	Count the number of times different packets are lost. The counter is overflow protected to 15, and discontinue at max until reset. The counter is reset by writing in RFChannel
RsntPckCnt	3:0	RO	0x0	Count the number of times the packet has been retransmitted. The counter is reset each time a new packet transmission starts.

4.14 Registers OwnAddr (0x0E to 0x010)

The OwnAddr is splitted into 3 registers

Register	Mnemonic	Bit	type	Reset Value	Description
0x0E	DeviceAddrB0	7:0	R/W	0x0F	Address of this device (Byte 0). The 4 least significant bits of this resister shall be set to b1111 to achieve the best performances
0x0F	DeviceAddrB1	7:0	R/W	0x00	Address of this device (Byte 1)
0x10	DeviceAddrB2	7:0	R/W	0x00	Address of this device (Byte 2)

In order to achieve a communication between 2 devices the peer address of the receiving device shall be the same as the own address of the transmitting device.

4.15 Registers PeerAddr (0x11 to 0x13)

The PeerAddr is splitted into 3 registers

Register	Mnemonic	Bit	type	Reset Value	Description
0x11	PeerAddrB0	7:0	R/W	0x0F	Address of this device (Byte 0). The 4 least significant bits of this resister shall be set to b1111 to achieve the best performances
0x12	PeerAddrB1	7:0	R/W	0x00	Address of the peer device (Byte 1)
0x13	PeerAddrB2	7:0	R/W	0x00	Address of the peer device (Byte 2)

In order to achieve a communication between 2 devices the peer address of the receiving device shall be the same as the own address of the transmitting device.

4.16 Register TXPayloadLength (0x14)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:5	-	b000	Only b000 allowed.
TxPldLen	4:0	R/W	b00000	Number of bytes to be sent. Shall be between 0 and 31

4.17 Register RXPayloadLength (0x15)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:5	-	b000	Only b000 allowed.
RxPldLen	4:0	RO	b00000	Number of received bytes

4.18 Register FIFOCtrl (0x16)

The value of this register is automatically reset to 0x00, one shot (OS) register, once the desiderated operation is performed.

Mnemonic	Bit	type	Reset Value	Description
TxPtrInc	7	OS	0	Increment pointer in TX FIFO
TxFlush	6	OS	0	Flush TX FIFO
RxPtrInc	5	OS	0	Increment pointer in RX FIFO
RxFlush	4	OS	0	Flush RX FIFO
Reserved	3:0	-	0x0	Only 0x0 allowed.

4.19 Register FIFOStatus (0x17)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:4	-	0x0	Only 0x0 allowed.
RxFull	3	RO	0	Indicates that the RX FIFO is full
RxEmpty	2	RO	1	Indicates that the RX FIFO is empty
TxFull	1	RO	0	Indicates that the TX FIFO is full
TxEmpty	0	RO	1	Indicates that the TX FIFO is empty

4.20 Register SVLDCtrl (0x18)

Mnemonic	Bit	type	Reset Value	Description
SVLDResult	7	RO	0	SVLD results. This value is set when the measured voltage is below the selected reference
SVLDStart	6	R/W	0	Start SVLD measurement
SVLDIntOnFail	5	R/W	0	SVLD generates the interrupt Int1Sts.IntStsPwrLow when the measured voltage is below the selected reference
Reserved	4:1	R/W	b0000	Must be set by host to b0111 to obtain a correct measurement.
SVLDSelLvl	0	R/W	0	Select SVLD level: 0 2.23V 1 2.49V

4.21 Register 0x19

This register is reserved. The only allowed value is 0x01.

4.22 Register SwReset (0x1A)

Mnemonic	Bit	type	Reset Value	Description
SwReset	7:0	R/W	0	Write value 0xB3 and value 0x5E sequentially to generate a software reset of EM9201

4.23 TX FIFO (0x40 to 0x5F)

The address range 0x40 to 0x5F is dedicated to the TX FIFO. Each value can be read or write independently or in a sequence (multi-read or multi write transaction). Each register is 8-bit wide in read/write access. There is no reset value, thus their initial values are undetermined.

4.24 RX FIFO (0x60 to 0x7F)

The address range 0x60 to 0x7F is dedicated to the RX FIFO. Each value can be read independently or in a sequence (multi-read transaction). Each register is 8-bit wide in read-only access. There is no reset value, thus without any reception the value is undetermined.

4.25 Reserved registers

All the registers not listed above are reserved. It is not allowed to write onto those registers. In case of accidental write, a reset of the device is needed for further proper operations.

5. Peripheral information

In this chapter design constraints are given for peripheral circuitry around the RF-core, i.e. the antenna port and the XTAL oscillator. Furthermore, PCB guidelines are stated in order to achieve an optimum RF-performance.

5.1 Antenna port

The antenna port of the EM9201 is available at the ANTP and ANTN pins, where a balanced RF signal is either received or transmitted. The differential impedance is 200Ω+j0Ω, which enables the use of printed folded dipole antenna without external matching components. In case of other antenna impedances a simple matching network can be used.

5.1.1 Folded dipole antenna

A folded dipole antenna can directly be connected to the EM9201 antenna port. This structure has the advantage to offer the EM9201 a directly 200Ω matched and omni-directional antenna. With a proper design, no additional external components are required. In case this antenna is created using PCB layout techniques, careful consideration have to be taken on the PCB material and the antenna dimensions in order to ensure the best performances in terms of output power and spurious emission. Figure 5.1 shows a layout example.

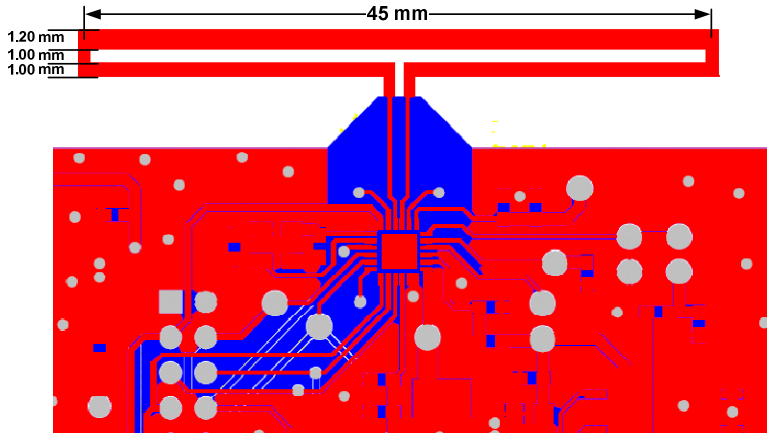


Figure 5.1: Layout example of a folded dipole antenna.

Designing PCB-antennas requires the use of dedicated CAD software which takes into account board materiel properties and antenna geometries. The layout proposal shown in Figure 5.1 is an example designed for a 2 layers FR4 PCB with 0.8 mm thickness. Placing ground close to the antenna structure (either top or bottom layer) will highly decrease the antenna performance (gain and directivity).

5.1.2 50 Ohm matching

The EM9201 can also be used with a 50Ω–termination to match a standard measurement system or a 50Ω–antenna structure. In that case, a matching circuit needs to be applied such that the required impedance conversion from the 50 Ω to the differential 200Ω antenna port impedance can be ensured. The matching network can as well be used to filter out the unwanted emission at frequency outside the ISM band. For this reason is highly advised to use components having high quality factor (QL > 50) to make the filtering characteristic as sharp as possible.

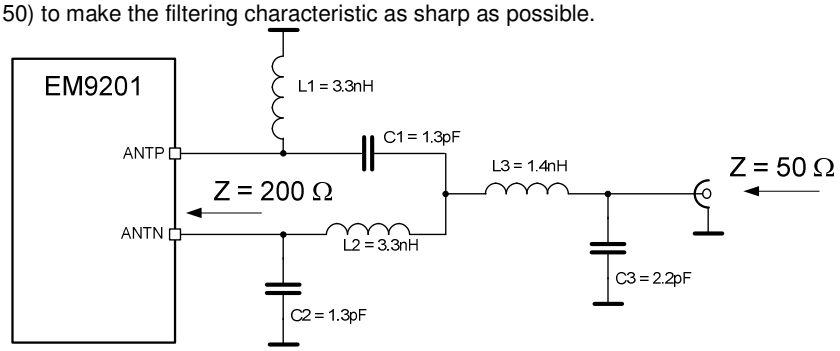


Figure 5.2: Matching circuit for 50 Ohm antenna.

Figure 5.2 shows a circuit example for such a matching network. Please note that also here the layout around the antenna port - both for the chip and attached antenna connector – needs to be done with having RF guidelines in mind.

5.2 XTAL Oscillator

In order to achieve low power operation and good frequency stability of the XTAL-oscillator, certain considerations with respect to the Quartz load capacitance C_0 need to be taken into account. Figure 5.3 shows a simplified block diagram of the amplitude regulated oscillator used in the EM9201.

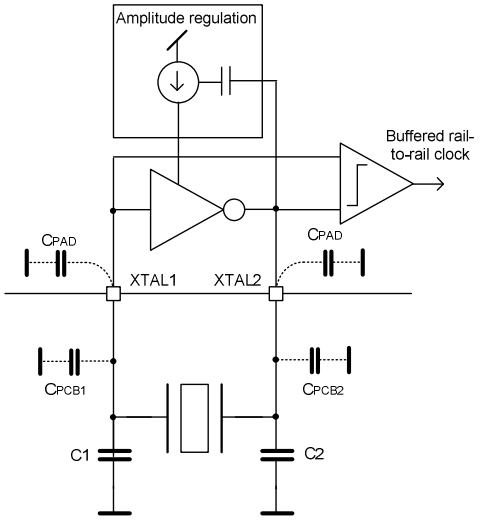


Figure 5.3: Amplitude regulated XTAL oscillator.

Low power consumption and fast start-up time is achieved by choosing a Quartz crystal with a low load capacitance C_0 – a reasonable choice is e.g. C_0=10pF as used in the typical application described in Section 2. To achieve good frequency stability the following equation then needs to be satisfied:

$$C_0 = \frac{C_1' \cdot C_2'}{C_1' + C_2'}$$, where $C_1' = C_1 + C_{PCB1} + C_{PAD}$, $C_2' = C_2 + C_{PCB2} + C_{PAD}$.

Capacitors C_1 and C_2 are external (SMD) components, C_{PCB1} and C_{PCB2} are PCB routing parasites and C_{PAD} is the equivalent small-signal pad-capacitance. The value of C_{PAD} is around 1pF for each pad.
The routing parasites should be minimized by placing Quartz and C_1 / C_2 close to the chip, not only for easier matching of the load capacitance C_0, but also to ensure robustness against noise injection.

To achieve good noise immunity against external interference, the XTAL oscillator is designed with low input impedance using a chip-internal 260kΩ resistor between XTAL1 and XTAL2. In case the noise robustness needs to be further increased, an external parallel resistor can be added at the cost of extra current consumption.

5.2.1 Frequency tolerance

In order to achieve the system target of +/-30ppm overall Xtal oscillator frequency stability, the external Quartz needs a total tolerance better than +/-30ppm. The specified frequency drift is meant to include initial frequency tolerance, temperature stability and aging effects.

5.3 PCB Guidelines

A number of PCB guidelines have to be respected in order to ensure proper RF operation of the EM9201. Generally, it is recommended to use at least a 2 layers PCB, dedicating one layer to one common ground plane covering all external components and the chip itself (the die pad should also be connected to this ground plane). Furthermore, prioritized layout focus should be kept for the following subjects:

- Antenna and antenna matching network.
- Power supplies.
- XTAL oscillator.

5.3.1 Antenna port and antenna matching network

Keep the EM9201 ANTN/ANTP symmetry both in component and in via placement, as well as line-routing. Place 100Ω transmission lines between the EM9201 RF output pins and the antenna output (or the matching network). In any case, try to minimize RF trace lengths.

Respect also a 3mm clearance to ground close to RF transmission lines and components (including matching network). In particular, respect clearance to ground for antenna structure (may varies with antenna topology). Do not put a ground plane below antenna structure to avoid gain loss and directivity modification.

5.3.2 Power supply

The power supplies have to be properly decoupled. In particular, the decoupling on AVDD_PA (Power supply for PA) and VDD (power supply for digital part) are critical and the decoupling capacitors have to be put as close as possible to the pin. In any case, the ground connections have to be as short as possible using vias directly to the ground plane. Avoid sharing vias between different signals and different grounds.

5.3.3 XTAL oscillator

Connect each capacitor of the XTAL oscillator to ground by a separate via, also separated from XTAL ground pads. Please also read the consideration regarding PCB routing parasites described in Section 5.2.

5.3.4 Layout example

Figure 5.4 shows an example of a well designed PCB the layout. It shows how the EM9201 is placed together with all external components and a 50 Ω RF-port (see also 5.1.2).

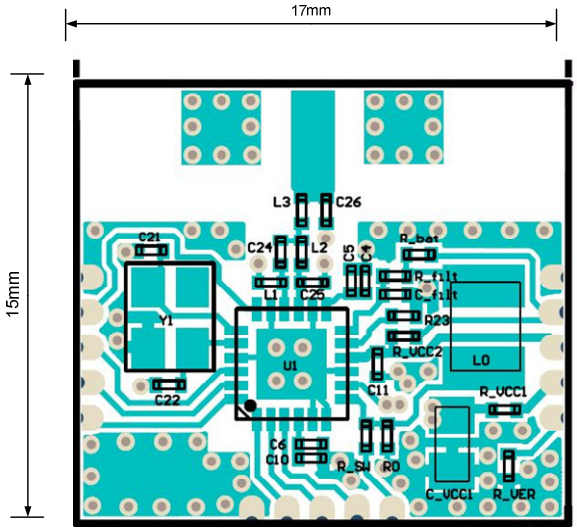


Figure 5.4: Layout example for good component placement.

On the left side of the IC the Quartz (Y1) together with load capacitors C21/C22 are placed. Both components are very close to the IC as routing parasites need to be minimized. To the North of the EM9201 one can find the 50Ω/200Ω - matching network (L1, L2, L3, C24, C25,C26). Decoupling caps for the supply (AVDD_PA: C4,C5 and VDD: C6, C10) are also in close vicinity of the chip, such that their effect on spike reduction is maximized.

5.3.5 Pad Location diagram

This chapter describes the location and the dimension of the EM9201 Pads in die form. Refer to Figure 5.5 for the detailed dimensions and pad positioning.

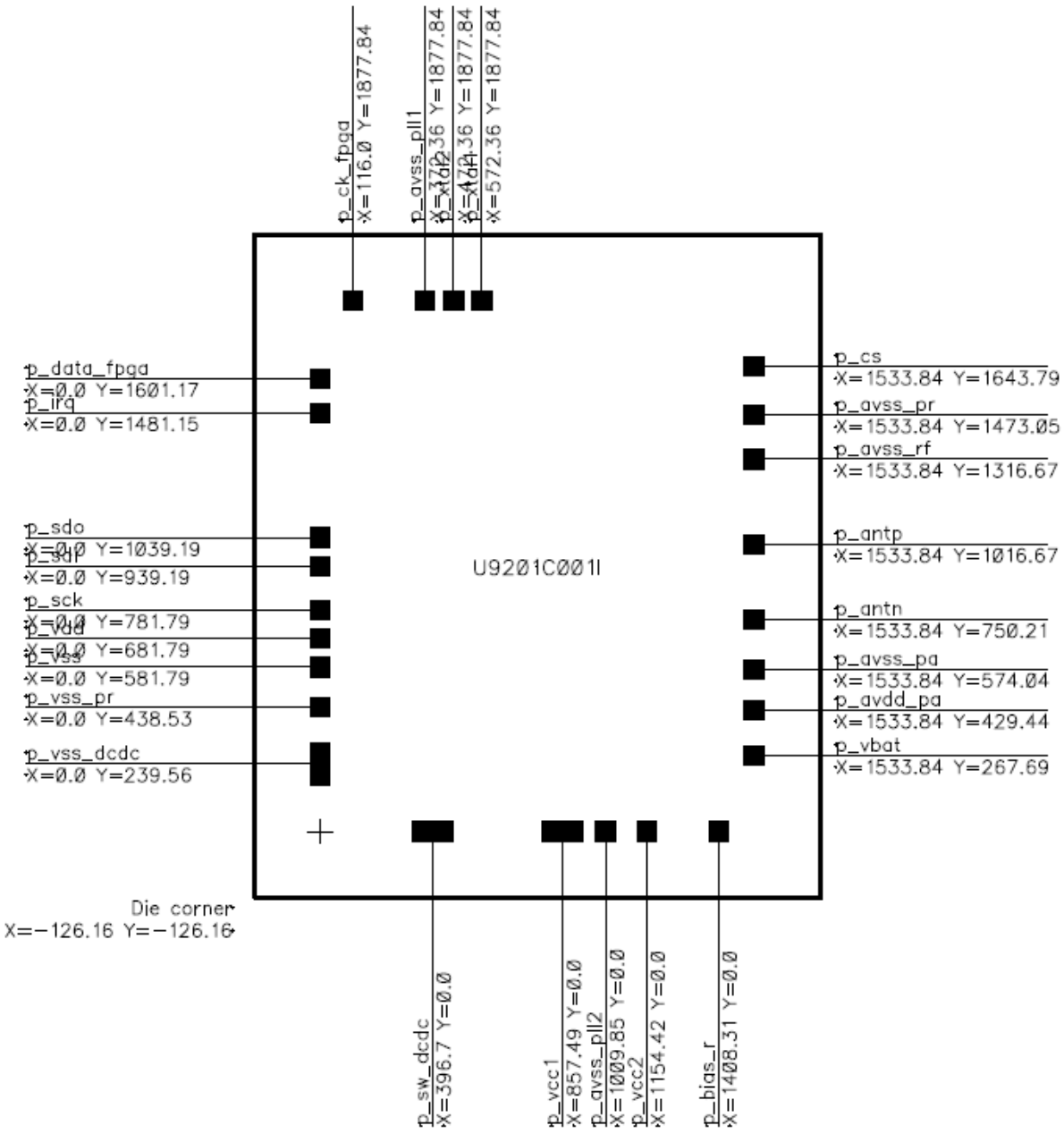


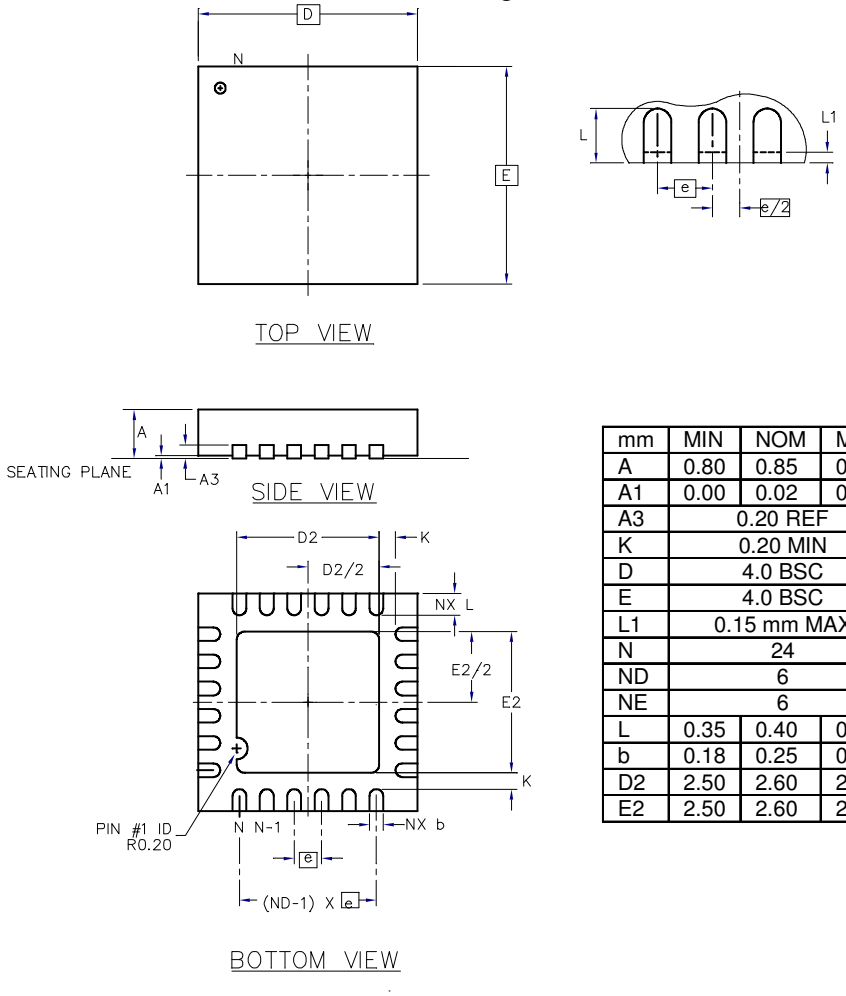
Figure 5.5: Pad location diagram

6. Ordering and Package Information

EM9201 is available in a MLF24 4 x 4 package. Table 6.1 and Figure 6.1 summarize the ordering and packaging information.

Ordering Code	Description	Packaging	Container
EM9201V12LF24D+	1 Mbps Transceiver	MLF24	TBD
EM9201V12WW7	1 Mbps Transceiver	Naked Die	TBD

Table 6.1: Ordering information



mm	MIN	NOM	MAX
A	0.80	0.85	0.95
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20 MIN	
D		4.0 BSC	
E		4.0 BSC	
L1		0.15 mm MAX	
N		24	
ND		6	
NE		6	
L	0.35	0.40	0.45
b	0.18	0.25	0.30
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70

Figure 6.1: Package information

1	2	3	4	5	6
A	9	2	0	1	0
B	0	2			
C					

Table 6.2: Package marking

products, expressly or by implications. EM's products are not authorized for use as components in life support devices or systems.