FCC ID: SQ9XKT1002
IC: 5768A-XKT1002

Technical Description:

The functions of main ICs are mentioned as below;

1) U2 acts as 2.4GHz RF Module (EM9201).
2) U1 acts as MCU (SNC82120).
3) U3 acts as Voltage Regulator (S-1112B33 MC-L6 STF G).
4) U4, L1 and associated circuit act as control the motion of Lucy.
5) S1 acts as Control button

Antenna Used:
Patch Antenna has been used.

World's First Fully Integrated Single-Cell Battery 2.4 GHz Transceiver

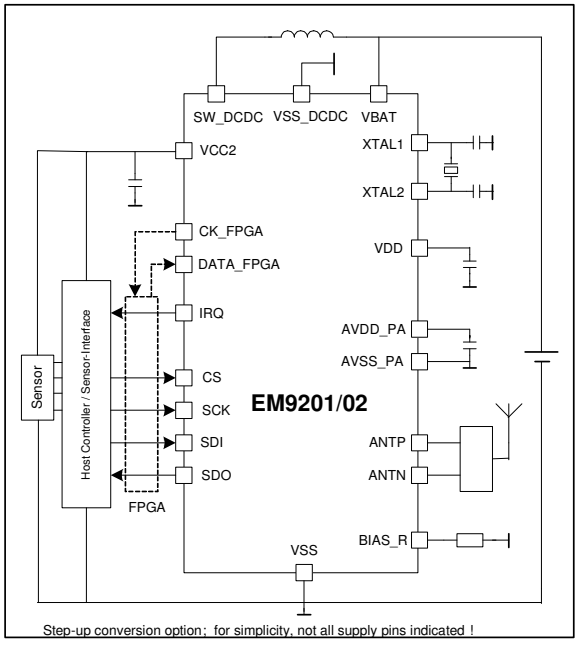
Description

The EM9201/02 is a low-voltage 2.4GHz transceiver IC with built-in link-layer logic permitting proprietary wireless links in the 2.400 … 2.4835 GHz ISM band. It has a radio core with a low-IF architecture and GFSK modulation scheme being compliant with the emerging Bluetooth low energy technology standard.
Control of the link-layer logic is possible though the SPI interface using an external host-controller. An FPGA bridge is included in the circuit such that with an external FPGA any protocol compatible with the RF characteristics can also be emulated through the SPI port of the EM9201/02.
The EM9201/02 can be operated from a single 1.5V battery by making use of the on-chip step-up (boost) DC/DC converter. This converter is designed to support an extra load such as a low-power microcontroller (host) or sensor interface circuit with a dedicated application profile.
The EM9201/02 can also operate without the DC/DC converter, when supplied from a 3 V battery or any other source such as an external LDO regulator. No external coil is needed then.

EM9201: up to 1 Mb/s on air data rate
EM9202: up to 2 Mb/s on air data rate

Chip versions, programmable by metal mask option
V1: with DC/DC converter for 1.5V battery
V2: w/o DC/DC converter for any voltages 1.9 – 3.6V

Typical Application Schematic



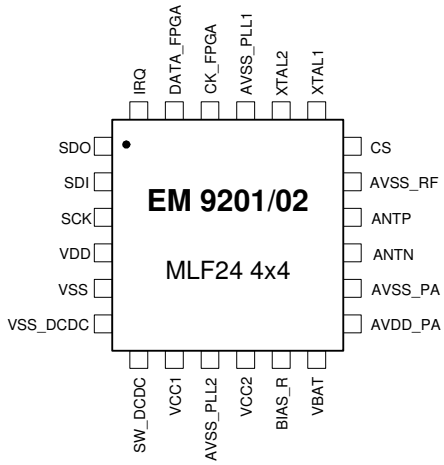
Features

- Single cell 1.5V battery operation (Alkaline AA, AAA)
- Operation down to V_{BAT} = 0.8 V (for start-up --> 1.0V)
- 3 V Lithium battery as alternative
- Bluetooth Low Energy-compliant GFSK modulation
- Low drift of PLL frequency by design
- On air data rate: 1Mb/s for EM9201, configurable 1Mb/s or 2Mb/s for EM9202
- Programmable RF output level:
  -20 dBm … + 4dBm in 8 steps
- No antenna matching elements needed through appropriate PCB antenna design :
- 200 Ω differential impedance of antenna port
- Low-cost 26MHz Xtal
- BLD function: battery level detection in accordance with selected battery
- Current consumption (on V_{CC}, V_{CC} =2.1V, 2Mb/s)
  12.5 mA in RX
  11.5 mA in TX (0dBm output power)
  3.0 µA in sleep-mode (DC/DC running on RCosc) [1)]
  0.8 µA in power-down mode (3V version, DC/DC off)
  [1)] External load reduced to < 500µA
- MLF24 4x4 package

Applications

- Remote sensing in general
- Wireless mouse,keyboard etc.
- Wireless sensors in watches
- Wireless sports equipment
- Alarm and security systems

Pin Assignment



Contents

1. Introduction

The EM9201/02 is a highly integrated multi-channel RF transceiver designed for low-power and low-voltage wireless applications in the world wide ISM frequency band at 2.400 - 2.4835GHz.

EM9201/02's TX-chain features a completely on-chip GFSK transmitter based on direct synthesis of the RF-signal directly applied to the 2.4GHz power amplifier. The output power can be digitally tuned in a wide range (-20 dBm …+4 dBm) in order to optimize the current consumption for a wide set of applications. For the EM9201 the on-air transmission rate is 1Mb/s, in the EM9202 it can be digitally set either to 1Mb/s (W-mode) or 2Mb/s (E-mode).

Thanks to the very robust low-IF architecture employed in the RX-chain, the EM9201/02 can operate without the need of expensive external filters for the blocking of undesired RF-signals. It features a fully on-chip low noise, high sensitivity 2.4 GHz front-end, which works reliably despite the presence of a power-full DC/DC converter. The fast configurability of the integrated frequency synthesizer makes the EM9201/02 also suitable for frequency hopping.

By employing an on-air interface with a differential real impedance of 200 Ohm, the EM9201/02 allows the usage of a properly designed loop antenna without the need of further external components. Adaptation to any other load impedance, can be however achieved using a simple matching network.

In addition to the RF transceiver the EM9201/02 has a power management system that is capable, on its DC/DC enabled version, to work on a single 1.5 V button battery cell. The DC/DC step-up converter not only feeds the whole RF-core, it is also powerful enough to supply some external components like a microcontroller at 2.1 V, and up to 100 mA load. Furthermore, the DC/DC converter can be re-configured into an extreme low-power mode, where it provides around 2 V with only very little intrinsic current consumption (3 uA) and therefore enables power-efficient 1.5V applications with low RF duty cycle.

These features make the EM9201/02 an attractive choice for a broad range of wireless applications, where power-efficient single battery operation is a needed. With the low bill-of-material thanks to minimized component count and cheap of-the-shelf components, this device on top of that will also make the difference in terms of system cost.

1.1 Block diagram

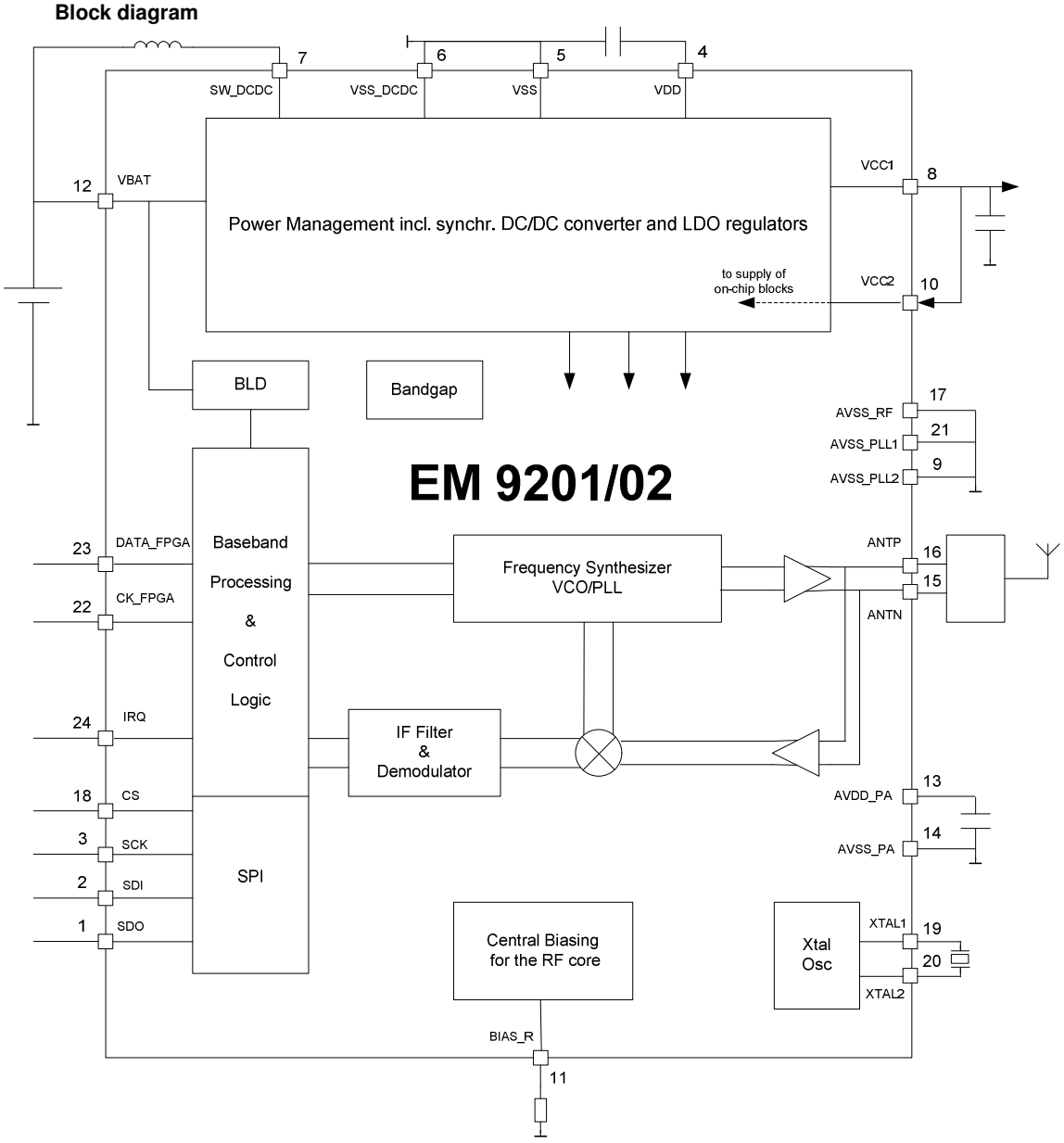


Figure 1 Simplified block diagram (DC/DC configuration).

1.2 Pin information (all versions)

Pin Nr	Name	I/O	Description
1	SDO	O	SPI data output
2	SDI	I	SPI data input
3	SCK	I	SPI clock input
4	VDD	O	Positive supply of digital part (baseband and frequency synthesizer)
5	VSS		Negative supply of digital part (plus ESD protection digital segment) [1)]
6	VSS_DCDC		Negative supply for DC/DC converter [1)]
7	SW_DCDC	I/O	Coil switch of DC/DC converter
8	VCC1	O	Output of DC/DC converter. On Version 2 (no DC/DC) connected to ground [2)]
9	AVSS_PLL2		Negative supply of PLL [1)]

Pin Nr	Name	I/O	Description
10	VCC2	I	Feedback / for chip supply, to be connected to VCC1 (plus ESD protection)
11	BIAS_R	I/O	Terminal for bias-setting resistor
12	VBAT		Positive battery supply (for DC/DC). On Version 2, connected to ground.
13	AVDD_PA	O	Regulated output voltage of PA supply; not to be loaded by any external circuitry
14	AVSS_PA		Negative supply of PA [1)]
15	ANTN	I/O	Negative antenna terminal
16	ANTP	I/O	Positive antenna terminal (input in RX-, output in TX mode)
17	AVSS_RF		Negative supply of RF part (plus ESD protection Analog/RF segment) [1)]
18	CSN	I	SPI Chip Select
19	XTAL1	I	Xtal oscillator input
20	XTAL2	O	Xtal oscillator output
21	AVSS_PLL1		Negative supply of PLL [1)]
22	CK_FPGA	O	Clock out for optional FPGA
23	DATA_FPGA	I/O	Data terminal for optional FPGA
24	IRQ	O	Interrupt output for external hostcontroller

Note 1: For a proper operation of the chip, this terminal shall be connected to a common ground plane

Note 2: Version 1 is the EM9201/02 with on-chip DCDC converter; Version 2 has no DC/DC.

2. Electrical specifications

2.1 Absolute maximum ratings

Parameter	Min.	Max.	Unit
Supply Voltage VSUP - VSS	-0.3	3.8	V
Input Voltage	VSS – 0.2	VSUP+0.2	V
Electrostatic discharge to Mil-Std-883C method 3015.7 with ref. to VSS	-2000	+2000	V
Maximum soldering conditions / Packages are Green-Mold and Leadfree	As per Jedec J-STD-020C		

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction

2.2 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

2.3 General Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply voltage Version 1 (applied on pin VBAT)	0.8	1.5	1.8	V
Supply voltage Version 2 (applied on pin VCC2)	1.9	3.0	3.6	V
Temperature range	-40		+85	°C

2.4 Electrical Characteristics

In this chapter, the electrical characteristics of the EM9201/02 are summarized for all its Versions. As the main difference in these Version is only how the general supply Vcc2 is used (i.e. with the DC/DC for Version 1 and w/o on Version 2), the electrical specs overlap greatly and therefore do not have to split-up. Please inspect the Version summary on in Chapter 6.

2.4.1 Supply Currents on Vcc2 (all Versions)

V_{CC2} = 2.1V (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power-Down	Icc_pd	Version 2 (no DC/DC), no oscillators running, register values maintained		0.8		µA
Xtreme Mode (DCDC sleep mode)	Icc_xtr	Version 1 (DC/DC), RC oscillator running, Xtal-oscillator off. DC/DC in Xtreme low-power mode I_{Lext} < 500µA		3		µA
Standby (26 MHz) [1)]	Icc_stdby_26	26MHz Xtal oscillator active		150		µA
Standby low power (26 MHz) [1)]		Xtal low power mode activated		90		uA
Transmit Mode Current	Icc_tx	Pout = 0 dBm		11.5		mA
Receive Mode Current	Icc_rx			12.5		mA

Note 1 Depends on exact type of crystal, typical values are for TSS-3225A with 15pF load capacitors.

2.4.2 Vbat Supply and DC/DC step-up converter (Version 1)

Vbat = 1.5V, ILext = 10mA (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Battery Voltage Range	Vbat_suc	I_{Lext} < 30mA	0.8	1.5	1.8	V
Minimum start-up voltage	Vbat_start	I_{Lext} < 20mA			1.0	V
Battery-Low Detection Threshold Levels [1)]	Vbatmin_suc Vbatminw_suc Vbatlo_suc Vbatlow_suc	Battery Protection Battery Prot. Early Warning Battery Low Indication Battery Low Early Warning	 1.02	0.82 0.92 1.12 1.25	 1.22	V
Programmable Output Voltages	Vcc_suc	Code = 00 Code = 01 Code = 10 Code = 11	1.9 2.0 2.2 2.4	2.1 2.2 2.4 2.6	2.3 2.4 2.6 2.8	V
Xtreme mode output voltage	Vcc_xtr	I_{Lext} < 1uA		2.0		V
Output Voltage Ripple [2)]	Vcc_ripple	active (RF mode),I_{Lext} < 30mA Xtreme LP mode, I_{Lext} < 0.8mA			50 100	mVpp
Converter Efficiency [3)]	Eff_DC-DC	active (RF mode), I_{Lext} = 30mA, Vbat =1.2V Xtreme LP Mode, I_{Lext} = 30uA, Vbat = 1.2V		88 55		%
External load on Vcc2	Ivcc2_ext				100	mA
Current drawn from battery in battery protection mode	Ibat_bpm				75	µA

Note 1 default values, some fine adjustments with metal mask option is foreseen
Note 2 for C = 22uF, ESR_C = 100mΩ and L=10uH, ESR_L=120mΩ.
Note 3 Depends on external components (ESR_C, ESR_L, Ri_bat) ! Typical values are for C, L and ESR like in Note 2)

2.4.3 Vcc2 Supply for disabled DC/DC converter version (Version 2)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Battery Voltage Range	Vbat_nodc		1.9	3.0	3.6	V
Battery-Low Detection Threshold levels	Vbatlow_nodc	Battery Protection Battery Low Early warning	2.1	2.27 2.49	2.45	V

2.5 RF Characteristics

Vcc = 2.1V, (unless otherwise specified)

Parameter		Symbol	Notes	Min	Typ	Max	Unit
General RF conditions							
Operating frequency		f_{OP}		2400		2484	MHz
Differential antenna impedance					200		Ω
Data Rate	in W mode	DR_W			1000		kbps
	in E mode	DR_E	1		2000		kbps
Channel spacing	in W mode	F_{CHW}			2		MHz
	in E mode	F_{CHE}	1		2		MHz
Frequency deviation	in W mode	Δf_{MW}		±225	±250	±275	kHz
	in E mode	Δf_{ME}	1		±320		kHz
Crystal frequency		f_{XTAL}			26		MHz

Parameter		Symbol	Notes	Min	Typ	Max	Unit
Crystal frequency accuracy		Tol_{XTAL}	2			±50	ppm
Bit-Bandwidth product		BT			0.5		
Deviation from the channel centre frequency	in W mode					±150	kHz
	in E mode		1			±125	kHz
Maximum drift rate in W mode						200	Hz/µs
Frequency drift for any packet length in W mode						50	kHz
Transmitter Operation							
Output Power		P_{RF}		-20	0	+4	dBm
RF Output power dynamic range		P_{RFC}			24		dB
Number of output power steps		P_{STP}			8		
RF power accuracy		P_{RFAC}			±3		dB
Transmit power @ 2 MHz offset		P_{RF2}				-20	dBm
Transmit power @ 3 MHz offset		P_{RF3}				-30	dBm
Spurious emission in operating mode for *f* in the ranges 47MHz – 74MHz 87.5MHz – 118 MHz 174MHz – 230MHz 470MHz – 862MHz			3		-54		dBm
Spurious emission in operating mode for other *f* ≤ 1GHz			5		-36		dBm
Spurious emission in operating mode for *f* in the ranges 1.8 GHz – 1.9 GHz 5.15 GHz – 5.3 GHz			4		-47		dBm
Spurious emission in operating mode for other *f* > 1GHz			5		-30		dBm
Spurious emission in stand-by mode for *f* ≤ 1GHz			5		-57		dBm
Spurious emission in stand-by mode for *f* > 1GHz			5		-47		dBm
Receiver Operation							
Sensitivity for 0.1% BER	in W mode	RX_{SEW}			-83		dBm
	in E mode	RX_{SEE}	1		-82		dBm
Maximum input power for 0.1% BER		RX_{MAX}		-10			dBm
Spurious emission for 25MHz < *f* < 1GHz			5		-57		dBm
Spurious emission *f* > 1GHz			5		-47		dBm
Out-of band blocking for an input signal level -67 dBm specified in W & E mode							
Frequency range 30-1999 MHz					-30		dBm
Frequency range 2000-2399 MHz					-35		dBm
Frequency range 2484-2999 MHz					-35		dBm
Frequency range 3000-12750 MHz					-30		dBm
In band blocking for an input signal level -67 dBm specified in W mode							
Co-channel interference C/I					15		dB
1 MHz offset interference					15		dB

Parameter	Symbol	Notes	Min	Typ	Max	Unit
2 MHz offset interference				-17		dB
≥ 3 MHz offset interference				-27		dB
Image frequency interference				-9		dB
Adjacent interference to in-band image				-15		dB
In band blocking specified in E mode (see Note 1)						
Co-channel interference		1		11		dB
2 MHz offset interference		1		4		dB
4 MHz offset interference		1		-20		dB
6 MHz offset interference		1		-27		dB

Note 1 The E-mode (2Mb/s on-air data rate) is only available for EM9202

Note 2 Frequency accuracy includes initial tolerance and stability over temperature range and aging

Note 3 Measuring conditions and signals specifications are described on ETSI EN 300 440-1 V1.3.1 (2001-09) TX §7.3

Note 4 Measuring conditions and signals specifications are described on ETSI EN 300 328 V1.7.1 (2006-05) TX §4.3RX §8.4

Note 5 Measuring conditions TBD

2.6 Timing Characteristics

Vbat = 1.5V, Vcc = 2.1V, I_{Lext} = 10mA (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RX↔TX in same channel	Trx_tx				128	µs
RX↔TX with channel change	Trx_tx_ch				128	µs
Stand-by Mode → TX/RX Mode (transmission)	Tstd_rf				128	µs
Power-down → Stand-by Mode 1)	Tpd_std			0.8	1.5	ms
DC/DC converter start-up 2)	Tst_dcdc	Output settled to within ripple spec			100	ms
Xtreme LP mode to normal DC/DC mode transition time 1)	Txt_std	Output settled to within ripple spec			4.5	ms
Stdby mode to active (RF) mode transition time	Tstdb_rf	VCO/PLL settled EM9201/02 ready to receive/transmit			150	µs

Note 1: This time is dominated by the Xtal oscillator start-up. Typical values are for TSS-3225A with 15pF load caps.

Note 2: First start-up upon insertion of battery includes Xtal oscillator start-up and RC cold-start delay.

3. Functional description

3.1 EM9201/02 Start-up

From the power management point of view the EM9201/02 comes along in two different versions. In Version 1 the EM9201/02 can take advantage of an integrated DC-DC up-converter for applications that operate with a battery ≤ 1.8V, while Version 2 (without DC/DC converter) lives from batteries delivering a supply ≥ 1.9V. A detailed description of the different EM9201/02 versions is given on §6 on page 29.
The start-up procedure of those two versions is only slightly different and described below. This description is intended to be informational only as it is independent of any external actions.

3.1.1 Start-up with DC-DC up converter (Version 1)

When a battery is inserted, an RC oscillator starts up and provides a clock with fixed duty-cycle to the DC/DC converter. This one then ramps-up the VCC1 voltage with its soft-start circuitry, including coil current limitation and a voltage limiter to avoid excessive current in the coil, and on-chip switches, as well as a too big output voltage which could lead to a destruction of the chip. Any excessive on-chip load is avoided in that phase, i.e. the RF-core circuitry stays disabled, only the power management control part and most important bias circuitry is enabled.

The output of the voltage regulator for the digital part, supplied by VCC2, is monitored by a power-check detector circuit. As soon as this detector signals 'sufficient voltage', the Xtal oscillator is powered-up as the main timing-reference for the DC/DC and RF-core circuitry. After this amplitude regulated Xtal-oscillator indicates enough amplitude, the full regulation circuitry of the DC/DC converter is switched on, and the converter starts to work either in CCM (continuous current mode) or burst mode, according to the load which is present on its output.

At the same time, the IRQ pin is set to logic 1 such that the application (normally an attached host-controller) can have an indication when the start-up sequence is finished, the DC/DC converter can be loaded as well as the chip is ready to communicate through SPI. The DC/DC is designed to support loads up to 100mA and more, however its efficiency is optimized to a lower load current. Please notice, that the external load should be minimized when the EM9201/02 is in an on-air mode.

3.1.2 Start-up without DC-DC (Version 2)

In case an EM9201/02 Version 2 is used for applications without DC/DC converter, the start-up sequence is only slightly different than described above. Upon connecting a battery to the VCC2-pin, the regulated digital supply ramps up quickly and the RC oscillator is turned-on, providing a clock to the power-check circuit. After this one indicates enough supply, the Xtal oscillator is enabled which in turn releases the IRQ after a certain crystal dependent start-up time. The RC oscillator, used to allow a reliable Xtal start-up, is then stopped.

3.2 Functional Modes

This part describes in which modes the EM9201/02 can operate in and the way to control the changes in between them - Figure 2 shows a corresponding state diagram. As described in §3.1 on page 11 the EM9201/02 becomes functional at the end of the start-up procedure. At this point the change in between the states is mainly due to external commands (through the SPI interface). Some of the transitions are also automatic, e.g. for a one-shot transmission.

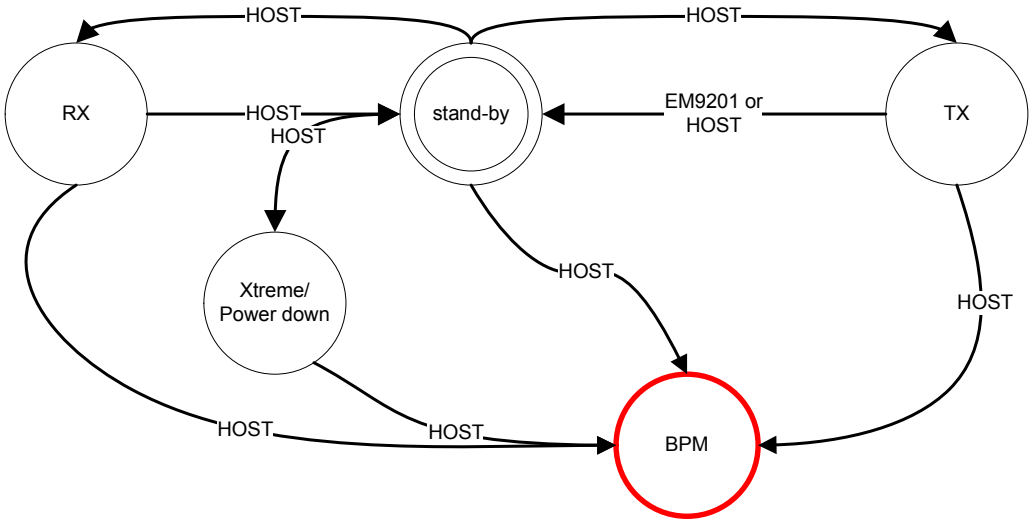


Figure 2 Simplified system state diagram.

3.2.1 Standby mode

This is the default mode into which the EM9201/02 goes after the reset, and the starting point for any RF operation (transmission / reception) or activation of special power-management modes (power-down / Xtreme-mode – see below). Here, only the Xtal oscillator is running and of course the DC/DC converter in case a Version 1 chip is used.

3.2.2 Battery Protection Mode (BPM)

For single battery cell applications using the DC/DC step-up converter the EM9201/02 features a so-called battery protection mode. It protects weak batteries from leaking their chemistry by limiting the amount of long-term constant current in case the device is not used. The BPM-mode is activated by an SPI command and sends the chip into a state where all electronics, except a resistive load, is switched off. It is important to know, that the BPM mode can only be left by inserting a fresh battery.
The BPM feature is of particular significance at the start-up of the system, since it can prevent excessive steady-state current due to an improperly started DC/DC converter in case a weak battery is applied.
It is recommended that after the start-up sequence is finished (IRQ goes high, see §3.1.1), a supply-check function is executed and in case this reveals insufficient battery voltage, the chip is sent into BPM.

3.2.3 Xtreme/ Power down mode

In order to minimize the power in idle case, the EM9201/02 can be set into a very low consumption mode. This mode is enabled by an SPI command. (`PowerMgt.Xtreme` = 1) and has different effects for the two chip-versions – in Version 1 it is called 'Xtreme mode', in Version 2 it is the 'Power down mode'.

3.2.3.1 Xtreme low-power mode (Version 1)

When entering the Xtreme-mode, the Xtal oscillator is turned off, and the DC/DC converter continues to operate from a low-frequency RC oscillator. As well, the major part of the converter's regulation circuitry is disabled and replaced by a simple regulation loop working acc. to a bang-bang principle. The VCC1 voltage swings then about linearly up and down, with a period depending on the actual circuit and external load. An increased ripple of 100mVpp will have to be tolerated on VCC1 then. The circuit is designed such that a certain external load is still supported. However, in order to fully profit from the very low current consumption of the EM9201/02 in that mode, it is strongly recommended to put also the external host controller into its mode of lowest consumption.

3.2.3.2 Power down mode (Version 2)

In this mode - only applicable for Version 2 chips without DC/DC converter - all on-chip clocks are disabled and the power consumption of the regulated digital supply is minimized. While in normal operation the voltage level seen on the VDD-pin is around 1.8V, it's now reduced to around 1.2V such that off-state leakage is reduced. All register values in the SPI interface are kept.

3.2.4 TX Mode

The TX-mode is defined as the mode in which the EM9201/02 will first set the radio core in TX state, and after a complete packet transmission, it will switch the radio core in RX state in order to receive the acknowledge (if the auto-acknowledge is selected). For a better description of the radio core states, refer to § 3.3.
The TX-mode can be only accessed from the 'Standby (see below) and provides correct RF-operation at the antenna port no later than the time specified in `RFTiming. RFStUpTim` – mainly determined by the settling time of the PLL in the frequency synthesizer.

3.2.5 RX Mode

In RX-mode, the EM9201/02 is ready to receive a GFSK-modulated RF-signals at 2.45GHz. In this mode the radio core is set in RX state, and upon reception of a packet set the radio on TX state for sending the acknowledge (if the auto-acknowledge is selected).
This mode can only be activated from the 'Standby' mode,.
After setting the RX mode a reliable RF-reception is possible after a time defined in `RFTiming. RFStUpTim`.

3.2.6 DC/DC Converter modes (not shown in Figure 2)

Apart from the already described Xtreme low power mode, the DC/DC converter operates in a set of different modes, some of which are activated automatically. The DC/DC reacts to the largely varying load present at its output VCC1 by automatically selecting the most effective operation – for small loads it's the so-called 'Burst mode', for high loads it the continuous current mode (CCM).

As it may be expected that the external host controller + sensor/interface need more voltage for some measurement and signal processing prior to sending data to the EM9201/02 for the on-air link to be established, the DC/DC output voltage can be set by the host temporarily to a higher value. It is recommended, however, to run the host-controller not in a high-speed mode with big consumption in the same time when the on-air link is running.

3.2.7 Standby low power (not shown in Figure 2)

The EM9201/02 also provides a second standby mode, where the current consumption of the only active Xtal-oscillator is reduced and the main system clock is set to around 400 kHz. This mode is complementary to the above mentioned Xtreme- / Power down mode since here the accurate time-base due to the Xtal oscillator is kept. However, the Standby low power mode is much less effective in terms of current savings.

3.3 Radio core

The radio (RF-core) of the EM9201/02 features a highly integrated multi-channel RF transceiver for wireless applications in the world-wide ISM frequency band at 2.4000 – 2.4835 GHz. Its robust low-IF architecture and the direct GFSK modulation scheme are not only designed for proprietary communication protocols, but also to be compatible with the emerging Bluetooth Low Energy Wireless standard. On air date-rates of 1Mb/s or 2Mb/s (only EM9202) are supported for up to 40 channels. The digital GFSK-modulation and -demodulation is performed using a bit-bandwidth product (BT) of 0.5 and a data-rate dependent modulation index of 0.5 for 1Mbit/s and 0.32 for 2Mbit/s (only EM9202).
The radio core can be programmed to be in two main states:

- TX state: the whole transmit-chain is active and the digital baseband data can be up-converted to a 2.4GHz GFSK modulated signal
- RX state: the frequency synthesizer and the whole RX-chain are active and ready to receive a packet.

The RF-core is built-up of three major sub-systems:

3.3.1 Frequency synthesizer (PLL)

The frequency synthesizer provides accurate and low jitter 2.45 GHz RF signal used both for the up-conversion process in TX state and for the down-conversion of an on-air RF signal in RX state. Up to 40 different frequencies can be synthesized. In order to support direct GFSK- modulation in transmit-operation with low frequency drift, its architecture is based on a closed loop modulation approach. For proper centring of the VCO control voltage an auto-calibration mechanism is included in the PLL. Furthermore, the PLL lock-status can be read from outside the chip using a corresponding SPI read command (see §4.1)

3.3.2 RX-chain

High sensitivity (-83dBm for 1Mb/s) RF-reception at 2.45 GHz is achieved by using a low noise resonant RF-amplifier (LNA), followed by a down-conversion mixer and an IF-filter. The output of the IF-filter is fed to a limit-amplifier, whose digital I/Q signals stimulate the subsequent digital GFSK-demodulator. At the demodulator output, received packet data and status information is available, which finally is fed to the digital baseband (see Chapter §3.4).
The RX-chain also features a receive-signal-strength indicator (RSSI), which can measure the down-converted RF-power after the IF-filter. Its averaged value can be read through the SPI after the single-shot RSSI measurement has been completed (see §0).

3.3.3 TX-chain

The TX chain consists on a GFSK modulator which is included in the frequency synthesizer (see §3.3.1) and a Power Amplifier (PA) output stage.
The PA output power can be adjusted to one of its 8 levels like shown in Table 1 – these levels can be set by the `RFPwr[2:0]` bits of the `RFSetup` register.

RF Power (RFPwr[2:0])	Output power	DC Current consumption
111	+4 dBm	15.6 mA
110	0dBm	11.8 mA
101	-3 dBm	10.2 mA
100	-6 dBm	8.9 mA
011	-9 dBm	7.9 mA
010	-12 dBm	7.3 mA
001	-16 dBm	6.9 mA
000	-20 dBm	6.7 mA

Measuring conditions: VCC2 = 3.3V, VSS=0V, T=27°, load impedance = 200 Ohm.
Table 1 RF power setting of the EM9201/02 (at 2Mb/s).

3.3.4 Air data rate

The EM9201/02 can be set to have 1Mb/s (W-mode) or 2Mb/s (E-mode, only EM9202) on-air data rate transmission/reception. A higher data rate allows having less probability of on-air collision due to the minimisation of the transmission time. It also lowers the average power consumption beside higher peak consumption.

The air data rate is set by `RFSetup.RFDR` bit.

To be able to establish a communication both devices of a link shall be set on the same data rate.

3.3.5 Channel frequency

The channel frequency determines the centre frequency of transmission channel used by the EM9201/02. The width of the channel is depending on the data rate. With a data rate of 1Mb/s the channel width is 1 MHz. The width increases to 2MHz for 2Mb/s (only EM9202).

The channel is set on `RFChannel` register. `RFChannel` shall be a value in between 0 and 39. If a value greater than 39 is set the channel will be considered to be 39.

The center frequency is defined as below:

F_c = 2402 + `RFChannel*2`

To be able to establish a communication both devices of a link shall be set on the same channel.

3.4 Baseband

The 'Baseband' -processor is the central digital control system of the EM9201/02. It handles all states of the chip including power-management, SPI transactions and of course the whole RF radio-control. Furthermore, it configures digital data for transmission as well as it processes packets received from the demodulator – generally all what is referred to 'Linklayer'. In the following, these link layer operations are described, i.e. the detailed function of the baseband for transmission and reception, packet format /identifier, etc.

The EM9201/02 is able to send and receive each packet in an independent way. An EM9201/02 configure in TX will send a packet in a burst, wait for the acknowledge packet from the other side, and go on stand-by mode (on stand-by mode, the host controller will be able to set the EM9201/02 in a different power mode). The EM9201/02 will also deal automatically with any re-transmission in case of bad acknowledge or absence of acknowledge.

The EM9201/02 can also send continuously, to transmit the complete FIFO.

In RX mode the EM9201/02 will wait for any packet on the given frequency, and verify the address, flag and CRC, then send a acknowledgement (ACK or NACK), and go back in reception until the host controller change the EM9201/02 mode to stand-by.

3.4.1 Autocalibration flow

For a correct transmission and reception, the PLL shall be calibrated before any data transmission attempt.
The calibration is done automatically by the PLL when requested.

To request the auto-calibration the `RFSetup.AutoCalib` bit shall be set to 1

This bit goes back to 0 at the end of the autocalibration, furthermore if requested an IRQ can be generated. The autocalibration end information is on `Int2Sts.IntStsAutoCalEnd` bit and can be masled by `Int2Msk.IntMskAutoCalEnd` bit.

The calibration of the PLL can differs slightly from one channel to another channel, and can vary if the external conditions change (e.g. temperature), thus this calibration request shall be re-done from time to time.

Note: The interrupt for the end of auto-calibration also appears during a normal transmit or receive operation, as it indicates that the PLL has completed its set-up procedure.

3.4.2 Transmission flow

1. Set PeerAddr[2:0] to the targeted address, and DeviceAddr[2:0] to the device address
2. Configure the data rate (only EM9202) and output power (RFSetup register)
3. Configure the channel used (0..39) (on RFChannel register. All values over 39 sets the channel to 39)
4. Set the mask for interrupts (on Int1Msk and Int2Msk).
5. Set packet length (TxPayloadLength) and data (TxFifo[0..length-1])
6. If the EM9201/02 is on Sleep/Xtreme mode the host shall go out of the Sleep/Xtreme mode by writing PowerMgt.Xtreme to 0, and wait for an acknowledge from the EM9201/02, by IRQ or polling (Int1Sts.StsXm_End).
7. Set the Config.Start and Config.TxRxn bits to 1.
8. The EM9201/02 will
   - Power up the radio system in transmitter state on the given frequency
   - Send the packet in one burst at the given data rate

- Go on receiver state and wait for the acknowledge packet

9. After having started the communication the host is allowed to send other data.
10. If the EM9201/02 will receive the acknowledge packet, it will go on stand-by mode, and sets the Config.Start to 0, with an Int1Sts.StsTxDs irq.
11. If the EM9201/02 doesn't receive any acknowledgement or receive a NACK packet, it increments the auto retransmission counter and if lesser than the maximum allowed goes back in transmission state (see 8), otherwise it goes on stand-by with a MAX_RT irq

3.4.3 Reception flow

1. Set PeerAddr[2:0] to the targeted address, and DeviceAddr[2:0] to the device address
2. Configure the data rate (only EM9202).
3. Configure the channel used (0..39) (on RFChannel register. All values over 39 sets the channel to 39)
4. Set the mask for interrupts (on Int1Msk and Int2Msk).
5. If the EM9201/02 is on Sleep/Xtreme mode the host shall go out of the Sleep/Xtreme mode by writing PowerMgt.Xtreme to 0, and wait for an acknowledge from the EM9201/02, by IRQ or polling (Int1Sts.StsXm_End).
6. Set the Config.Start bit to 1 and Config.TxRxn bit to 0.
7. The EM9201/02 will
   - Power up the radio system in receiver state on the given frequency
   - Listen for incoming communication
8. When a packet with matching address has been received, the EM9201/02 will go on transmitter state to send an ACK or NACK according to the correctness of the CRC, and come back on the receiver state.
9. If the packet was valid (correct CRC) the payload and length is stored on the data storage area, the Int1Sts.StsRxDr is set to 1, and the IRQ pin is set (if the corresponding mask is active).
10. The host micro-controller can stop the reception by setting Config.Start bit to 0.
11. It can then read the payload at its own data rate.

N.B. The EM9201/02 is able to receive one other packet during the time the host is reading the payload data.

12. The EM9201/02 is now ready for any other transmission.

3.4.4 Packet format

The packet has to contain the following information

Multi-byte data are always sent on-air with LSByte first. For each byte the LSBit is sent first on air.

Preamble	Address	Flags	Payload 1-32 bytes	CRC

Preamble	Preamble to detect 0 and 1 levels. The preamble is “01010101” if the address LSB is 0 The preamble is “10101010” if the address LSB is 1 The preamble is removed from the data stream
Address	The address field contains the address of the receiver. The address is 3 bytes long No more than 6 consecutive 0 are allowed The address is removed from the data stream
Flags	The flag is 1 byte long. 2 bits for packet identification 1 bit for packet type 5 bits for packet length

Payload	1-32 bytes wide
CRC	2 bytes The polynomial check is $x^{16} + x^{12}+x^5+1$

The structure of the acknowledge packet is very close to the normal packet except that no data are present.

Preamble	Address	Flags	CRC

This packet act as an ACK or NACK according to the CRC. If the CRC received is different of the one sent, this packet become a NACK otherwise it is an ACK packet.

3.4.5 Packet Identifier

Each packet contains a two bit wide PID field to detect if the received packet is new or resent. The PID will prevent that the RX device presents the same payload more than once to the HOST. The PID and CRC field is used by the RX device to determine whether a packet is resent or new.

The scheme of PID generation and detection is depicted in Figure 3

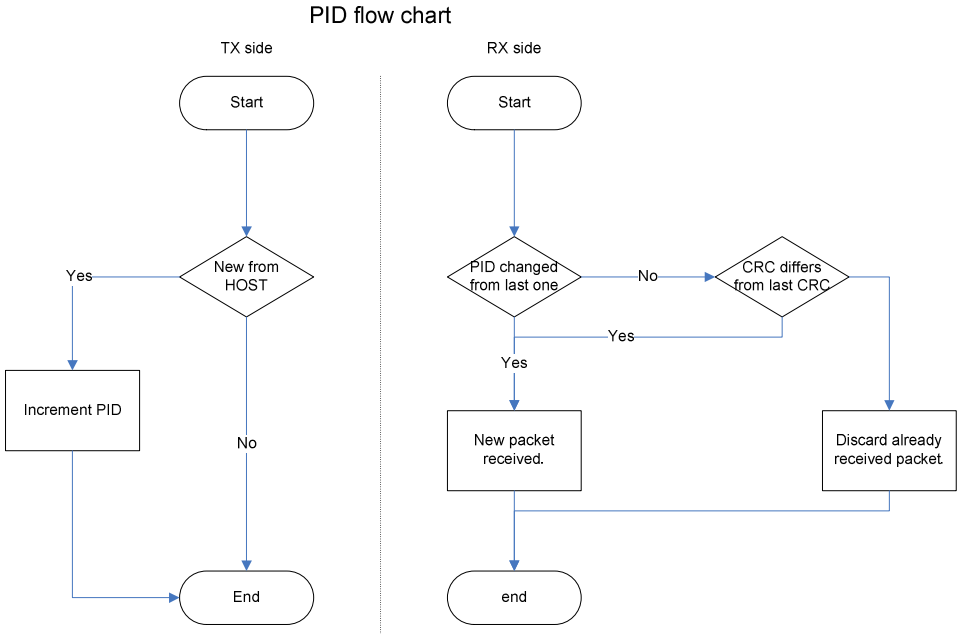


Figure 3 PID generation and detection

3.5 Power management

The power management system of the EM9201/02 provides the necessary supplies, voltage- / current references and timing circuitry for reliable operation in all modes of operations. Apart from the DC/DC converter, this includes low drop-out voltage regulators (LDO) for the RF-core and the whole digital part, a low noise band-gap and a bias-generator using an external resistor. All these circuits are powered through the VCC2 pin – either using the DCDC or by direct supply connections.

3.5.1 RF-core supply

All analog parts in the RF-core are supplied by two fully on-chip LDOs for the RX-chain (LNA, mixer, IF-filter) and the frequency synthesizer (PLL), plus a dedicated regulator for the power amplifier relying on an external 4.7nF decoupling capacitor. The voltage reference for these three regulators is derived from a low noise band-gap circuit. In order to optimize the current consumption in any mode of operation, the regulators as well as the band-gap/bias are enabled individually when needed – either automatically with respect to reception or transmission flow or by using the 'Bridge mode' (see §3.8).

3.5.2 Digital supply

The supply for all digital parts (VDD) in the system (base-band, frequency synthesizer and demodulator) is provided by a low power LDO and a second reference circuit. It assures that the logic is powered throughout the whole time of operation - not only in RF- but also in the power-down modes described in §3.2.3. This regulator uses an external decoupling capacitor of 220nF.

3.5.3 Bias generator

In order to create a stable and temperature independent current reference for the RF-core, the EM9201/02 features a bias generator based on an external 27 kΩ resistor and the on-chip band-gap reference. The spread of the current consumption in transmit / receive operation depends on this, therefore it is recommended that its tolerance is maximum +/- 2%.

3.6 Supply monitoring

The EM9201/02 offers the possibility for supply monitoring on several nodes in the system (VBAT, VCC2, VDD). The host-controller can launch a measurement by sending an SPI command, which compares the actual node voltage with a predefined level (see §4.20). After the measurement is completed the result (1 bit) can be read back from the corresponding SPI register. The following table shows how the supply monitoring is used for the different Versions:

EM9201/02 Version	Supply	Level [V]	Function
(1) DC/DC	VBAT	0.82	BPM mode, battery monitoring (see §3.2.2)
	VBAT	0.92	BPM early warning
	VBAT	1.12	Battery low detection (1.5V batteries)
	VBAT	1.25	Battery low detection, early warning (1.5V batteries)
(1) and (2)	VDD	1.43	n.a. (used for power-check at start-up)
(2) no DC/DC	VCC2	2.00	n.a. (used for chip internal monitoring)
	VCC2	2.27	Battery low detection (3V batteries)
	VCC2	2.49	Battery low early warning (3V batteries)

It is recommended that measurements are repeated several time in order to reduce inaccuracies due to noise.

3.7 SPI interface

The EM9201/02 can be controlled thanks to a 4-wire SPI interface and interrupt information (IRQ). The four wires are described as below:

- CSN: Chip selected (negated)
- SCK: Serial clock
- SDI: Serial data In (EM9201/02 view), also called MOSI.
- SDO: Serial data out (EM9201/02 view) also called MISO

3.7.1 SPI transaction

Each change on SDI is latched on the rising edge of SCK, and each change on SDO is done on the falling edge of SCK (see Figure 7 and Table 2)
Over this physical interface the protocol is byte-based. Each byte shall be sent MSBit first
An SPI transaction is defined by all the changes on SCK, SDI and SDO in between a falling edge of CSN and its next rising edge (see Figure 4 below).

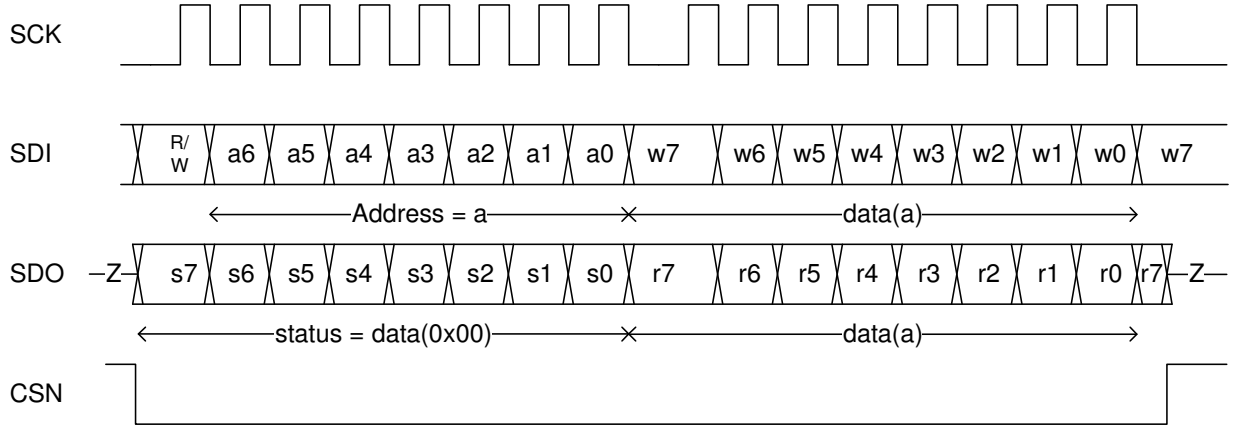


Figure 4 Raw SPI transaction

A transaction shall have a multiple of 8 SCK pulses to be complete. In case of incomplete transactions, only the complete bytes will perform the desired action.

The possible actions are:

- Read one or more consecutive register(s) and the status byte (register 0x00) (see Figure 5 below).
  This action needs at least 2 bytes (1 for address and read order, and 1 byte for reading the desired address.
- Write one or more consecutive register(s) and read the status byte (register 0x00) (see Figure 6 below).
  This action needs at least 2 bytes (1 for address and write order, and 1 byte for writing at the desired address.
- Read status byte.
  This action needs 1 byte.

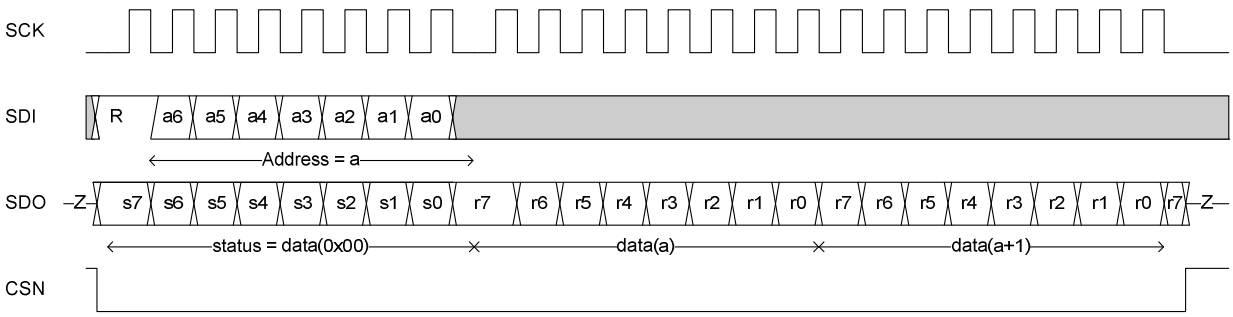


Figure 5 Multi-read SPI transaction

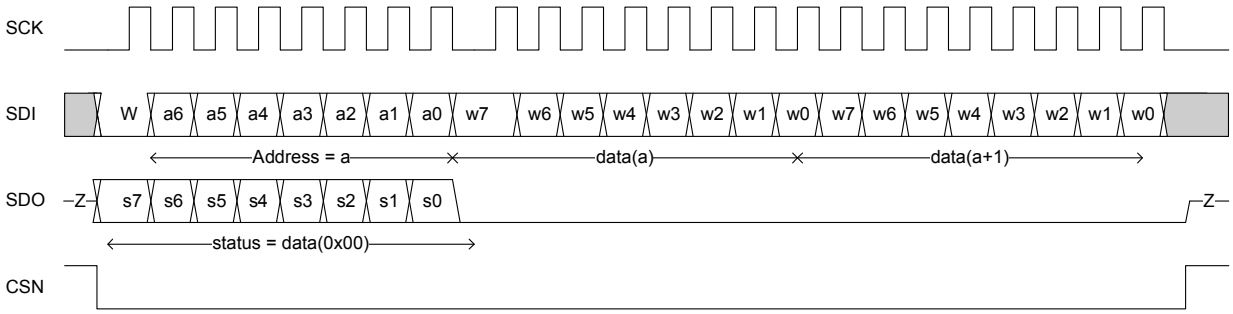


Figure 6 Multi-write SPI transaction

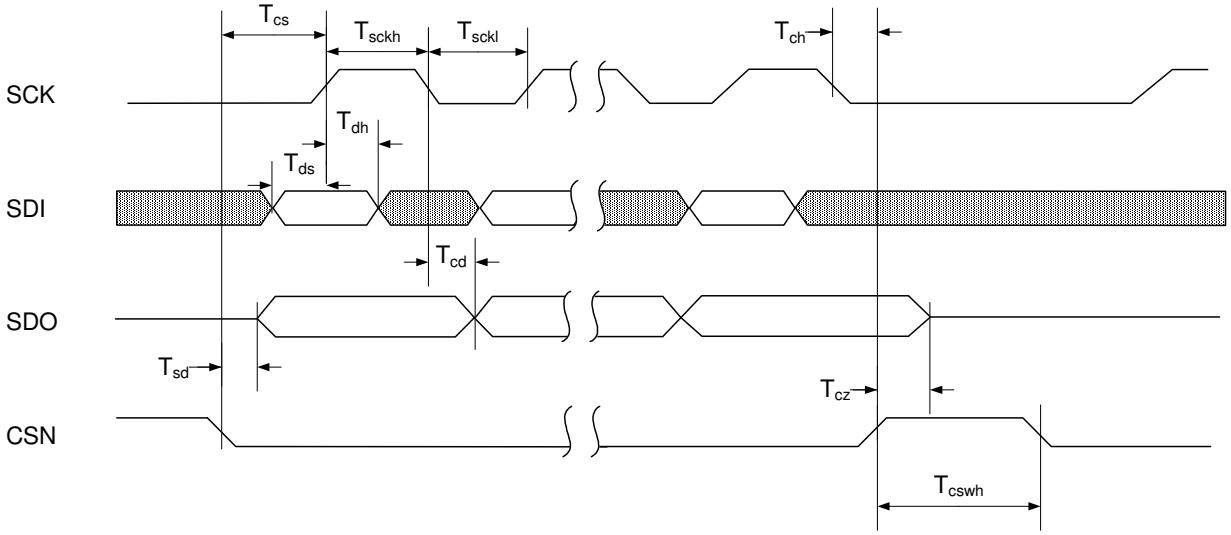


Figure 7 SPI timing diagram

Symbol	Parameters	Min	Max	Units
Tds	Data to SCK Setup	5		ns
Tdh	SCK to Data Hold	5		ns
Tsd	CSN to Data Valid		30	ns
Tcd	SCK to Data Valid		30	ns
Tsckl	SCK Low Time	40		ns
Tsckh	SCK High Time	40		ns
Fsck	SCK Frequency	0	10	MHz
Fsck_lp	SCK Frequency on low power/Xtreme mode	0	5	MHz
Tcs	CSN to SCK Setup	20		ns
Tch	SCK to CSN Hold	20		ns
Tcswh	CSN Inactive time	20		ns
Tcz	CSN to Output High Z		30	ns

Table 2 SPI timing values.

3.7.2 Interrupt flag

The EM9201/02 has an active high interrupt pin (IRQ).
The pin IRQ is activated when the selected interrupts (according to the mask information of the register 0x02 and 0x03) are activated on register 0x00 and 0x01.

Whatever is the value of the corresponding mask, the interrupt is stored on the register 0x00 and 0x01. The mask is used only to select which interrupt will activate the IRQ pin.

Note: the register 0x00 is also directly visible as the status information at each SPI transaction.

The interrupt register can be cleared by writing 1 to the bit to be cleared, and writing 0 on the one to keep.

3.8 Bridge

The bridge mode is used for allowing a direct access to the physical part thanks to the SPI for all configurations of the physical layer and two specific pads dedicated to the clock and stream needed to fed and receive correct data from the physical layer.

The bridge mode is useful when a link layer is done on an external component (MCU, FPGA, or ASIC) to use the GFSK modem and/or the power management features.

A more detailed description of the bridge mode features can be made available upon special request.

3.9 Software reset

The EM9201/02 can be soft reset by SPI.

To reset the EM9201/02 it is needed to write into the register SwReset two different values (0xB3 followed by 0x5E), in two consecutive SPI transactions.

The EM9201/02 software reset procedure is as follow:

```
Procedure EM920xSwReset() {
        EM920xWrite(SwReset,0xB3)
        EM920xWrite(SwReset,0x5E)
}
```

4. Registers

In this section all relevant registers of the EM9201/02 are described, i.e. their basic functionality and reset values. Any register not specifically mentioned here is a reserved one, and its content shall be set to 0x00.

4.1 Register Int1Sts (0x00)

As described As described on §3.7.2 on page 19, each of the interrupt can be clear by writing 1 on the bit to clear.

Mnemonic	Bit	type	Reset Value	Description
IntStsRxDr	7	R/W	0	Rx data ready. 1 means that a packet has been received
IntStsTxDS	6	R/W	0	TX data send. 1 means that a packet has been sent
IntStsMaxRT	5	R/W	0	Maximum number of TX retransmission exceeded
IntStsPLLNoLock	4	R/W	0	PLL not in Lock. 1 means that the PLL was not locked after the RF start-up-time or RX2TX switch time.
IntStsPckError	3	R/W	0	Packet error, phase variance to high during packet reception. Demodulator desynchronizes itself.
IntStsPwrLow	2	R/W	0	Power check measurement end. According to the value of SVLDCtrl. SVLDIntOnFail this bit indicates the end of each measurement or only the one that failed.
IntStsXtalHiPwr	1	R/W	0	Low power stand-by mode end
IntStsXmEnd	0	R/W	0	Sleep/Xtreme mode end

4.2 Register Int2Sts (0x01)

This register has the same behaviour as the Int1Sts. IntStsRstFlg is not maskable, and indicates the that the chip had a reset event.

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:2	-	0x00	Only 0x00 allowed.
IntStsRstFlg	1	R/W	0	Reset flag for power-up
IntStsAutoCalEnd	0	R/W	0	Auto calibration procedure end

4.3 Register Int1Msk (0x02)

Mnemonic	Bit	type	Reset Value	Description
IntMskRxDR	7	R/W	0	Interrupt mask - RxDR
IntMskTxDS	6	R/W	0	Interrupt mask - TxDS
IntMskMaxRT	5	R/W	0	Interrupt mask - MaxRT
IntMskPLLNoLock	4	R/W	0	Interrupt mask - PLLNoLock
IntMskPckError	3	R/W	0	Interrupt mask - PckError
IntMskPwrLow	2	R/W	0	Interrupt mask - PwrLow
IntMskXtalHiPwr	1	R/W	0	Interrupt mask - XtalHiPwr
IntMskXmEnd	0	R/W	0	Interrupt mask - XmEnd

4.4 Register Int2Msk (0x03)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:1	-	0x00	Only 0x00 allowed.
IntMskAutoCalEnd	0	R/W	0	Interrupt mask - AutoCalEnd

4.5 Register Config (0x04)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:6	-	0x00	Only 0x00 allowed.
WhitDis	5	R/W	0	Disable the RX-Whitener

Mnemonic	Bit	type	Reset Value	Description
Reserved	4	-	0	Only 0x00 allowed.
RxRestart	3	R/W	0	Restart packet reception
TxCont	2	R/W	0	Enable continuous transmission in TX mode
Start	1	R/W	0	Transmission start
TxRxn	0	R/W	0	Transmission mode, 0 - RX, 1 - TX

4.6 Register PowerMgt (0x05)

Mnemonic	Bit	type	Reset Value	Description
BPM	7:2	R/W	0	Battery protection mode. Write "0x3F" to go on BPM. Read returns always "0x00"
Xtreme	1	R/W	0	Xtreme mode on/off
LowPwrStdBy	0	R/W	0	Low power stand-by mode on/off

4.7 Register RFSetup (0x06)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:6	-	0x00	Only 0x00 allowed.
RFAutoCalib	5	R/W	0	Start PLL auto-calibration procedure
RFAFCDis	4	R/W	0	Disable AFC in RF core
RFDR	3	R/W	0	Data rate, can only be configured in EM9202 0 : 1 Mb/s 1 : 2 Mb/s
RFPwr	2:0	R/W	0	Set RF output power in TX mode 000 – -20 dBm 001 – -16 dBm 010 – -12 dBm 011 – -9 dBm 100 – -6 dBm 101 – -3 dBm 110 – 0 dBm 111 – +4 dBm

4.8 Register RFChannel (0x07)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:6	-	0x00	Only 0x00 allowed.
RFChannel	5:0	R/W	0x00	Channel number device operates on (maximum 39 channels)

4.9 Register RFTiming (0x08)

Mnemonic	Bit	type	Reset Value	Description
RFStUpTim	7:4	R/W	0xA	RF start-up time 0000 – 50 µs 0001 – 60 µs 0010 – 70 µs 0011 – 80 µs 0100 – 90 µs 0101 – 100 µs 0110 – 110 µs 0111 – 120 µs 1000 – 130 µs 1001 – 140 µs 1010 – 150 µs (default) 1011 – 160 µs 1100 – 170 µs

Mnemonic	Bit	type	Reset Value	Description
				1101 – 180 µs 1110 – 200 µs 1111 – 250 µs
RFSwTim	3:0	R/W	0xD	RF RX <-> TX switching time 0000 – 25 µs 0001 – 30 µs 0010 – 40 µs 0011 – 50 µs 0100 – 60 µs 0101 – 70 µs 0110 – 80 µs 0111 – 90 µs 1000 – 100 µs 1001 – 110 µs 1010 – 120 µs 1011 – 130 µs 1100 – 140 µs 1101 – 150 µs(default) 1110 – 160 µs 1111 – 170 µs

4.10 Register RFRSSI (0x09)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:5	-	0x00	Only 0x00 allowed.
RFRSSIEn	4	R/W	0	Enable of RSSI
RFRSSIOut	3:0	RO	0x0	Result of RSSI power measure

4.11 Register ACKSetup (0x0B)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:5	-	0x00	Only 0x00 allowed.
ACKDis	4	R/W	0	Auto-acknowledge disable
ACKTimeout	3:0	R/W	0xD	Timeout for waiting for acknowledge 0000 – 30 µs 0001 – 40 µs 0010 – 50 µs 0011 – 60 µs 0100 – 70 µs 0101 – 80 µs 0110 – 90 µs 0111 – 100 µs 1000 – 110 µs 1001 – 120 µs 1010 – 130 µs 1011 – 140 µs 1100 – 150 µs 1101 – 160 µs(default) 1110 – 170 µs 1111 – 180 µs

4.12 Register RetrSetup (0x0C)

Mnemonic	Bit	type	Reset Value	Description
ARDly	7:4	R/W	0x7	Auto Re-transmit Delay 0x0 – Wait for 250µs 0x1 – Wait for 500µs 0x2 – Wait for 750µs ..... 0x7 – Wait for 2000µs (default)

Mnemonic	Bit	type	Reset Value	Description
				…….. 0xF – Wait for 4000µs (Delay from end of transmission to start of the next transmission)
ARCntMax	3:0	R/W	0x3	Auto Retransmit Count 0x0 – Re-transmit disabled 0x1 – Up to 1 re-transmit ……. 0xF – Up to 15 re-transmit

4.13 Register RetrStatus (0x0D)

Mnemonic	Bit	type	Reset Value	Description
LstPckCnt	7:4	RO	0x7	Count lost packets. The counter is overflow protected to 15, and discontinue at max until reset. The counter is reset by writing in RFChannel
RsntPckCnt	3:0	RO	0x3	Count resent packets. The counter is reset when transmission of a new packet starts.

4.14 Registers DeviceAddr (0x0E to 0x010)

The DeviceAddr is splitted into 3 registers

Register	Mnemonic	Bit	type	Reset Value	Description
0x0E	DeviceAddrB0	7:0	R/W	0x00	Address of this device (Byte 0)
0x0F	DeviceAddrB1	7:0	R/W	0x00	Address of this device (Byte 1)
0x10	DeviceAddrB2	7:0	R/W	0x00	Address of this device (Byte 2)

4.15 Registers PeerAddr (0x11 to 0x13)

The PeerAddr is splitted into 3 registers

Register	Mnemonic	Bit	type	Reset Value	Description
0x11	PeerAddrB0	7:0	R/W	0x00	Address of the peer device (Byte 0)
0x12	PeerAddrB1	7:0	R/W	0x00	Address of the peer device (Byte 1)
0x13	PeerAddrB2	7:0	R/W	0x00	Address of the peer device (Byte 2)

4.16 Register TXPayloadLength (0x14)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:5	-	0x0	Only 0x00 allowed.
RxPldLen	4:0	R/W	0x00	Number of bytes to be sent

4.17 Register RXPayloadLength (0x15)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:5	-	0x0	Only 0x00 allowed.
TxPldLen	4:0	R/W	0x00	Number of received bytes

4.18 Register FIFOCtrl (0x16)

Mnemonic	Bit	type	Reset Value	Description
TxPtrInc	7	R/W	0	Increment pointer in TX FIFO
TxFlush	6	R/W	0	Flush TX FIFO
RxPtrInc	5	R/W	0	Increment pointer in RX FIFO
RxFlush	4	R/W	0	Flush RX FIFO
Reserved	3:0	-	0x0	Only 0x00 allowed.

4.19 Register FIFOStatus (0x17)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:4	-	0x0	Only 0x00 allowed.
RxFull	3	RO	0	RX FIFO full
RxEmpty	2	RO	1	RX FIFO empty
TxFull	1	RO	0	TX FIFO full
TxEmpty	0	RO	1	TX FIFO empty

4.20 Register SVLDCtrl (0x18)

Mnemonic	**Bit**	**type**	**Reset Value**	**Description**
SVLDResult	7	RO	0	SVLD result/output
SVLDStart	6	R/W	0	Start SVLD measurement
SVLDIntOnFail	5	R/W	0	SVLD generates interrupt on failed measurement 0 Int1Sts. IntStsPwrLow: the end of measurement 1 Int1Sts. IntStsPwrLow: failed measurement.
SVLDSelSrc	4:3	R/W	00	Select the source measured 00 Digital Regulated Voltage 01 VCC2 Voltage 10 VBAT Voltage 11 Digital Regulated Voltage
SVLDSelLvl	2:0	R/W	000	Select SVLD level 000 0.82V 001 0.92V 010 1.12V 011 1.25V 100 1.43V 101 2.00V 110 2.27V 111 2.49V

4.21 Register DCDCCtrl (0x19)

Mnemonic	**Bit**	**type**	**Reset Value**	**Description**
Reserved	7:2	-	0x0	Only 0x00 allowed.
DCDCLvl	1:0	R/W	01	DCDCLvl 00 2.1V 01 2.2V (default) 10 2.4V 11 2.6V

4.22 Register SwReset (0x1A)

Mnemonic	**Bit**	**type**	**Reset Value**	**Description**
SwReset	7:0	R/W	0	Write value 0xB3 and value 0x5E to generate a reset

4.23 TX FIFO (0x40 to 0x5F)

The address range 0x40 to 0x5F is dedicated to the TX FIFO. Each value can be read or write independently or in a sequence (multi-read or multi write transaction). Each register is 8-bit wide in read/write access. There is no reset value, thus their initial values are undetermined.

4.24 RX FIFO (0x60 to 0x7F)

The address range 0x60 to 0x7F is dedicated to the RX FIFO. . Each value can be read independently or in a sequence (multi-read transaction). Each register is 8-bit wide in read-only access. There is no reset value, thus without any reception the value is undetermined.

4.25 Reserved registers

All the registers not listed above are reserved. It is not advised to write onto those registers. In case of writing it is mandatory to write 0x00.

5. Peripheral information

In this chapter design constraints are given for peripheral circuitry around the RF-core, i.e. the antenna port and the XTAL oscillator. Furthermore, PCB guidelines are stated in order to achieve an optimum RF-performance.

5.1 Antenna port

The antenna port of the EM9201/02 is provided by the ANTP and ANTN pins, where a balanced RF signal is either received or emitted. Its differential impedance is 200Ω+j0Ω , which enables the use of printed folded dipole antenna without external matching components. In case of other antenna impedances a simple matching network can be used.

5.1.1 Folded dipole antenna

A folded dipole antenna can directly be applied to the antenna port. This structure has the advantage to offer the EM9201/02 a directly 200Ω matched and omni-directional antenna (no additional component required). In case this antenna is created using PCB layout techniques, careful consideration have to be taken on the PCB material and the antenna dimensions. Figure 8 shows a layout example.

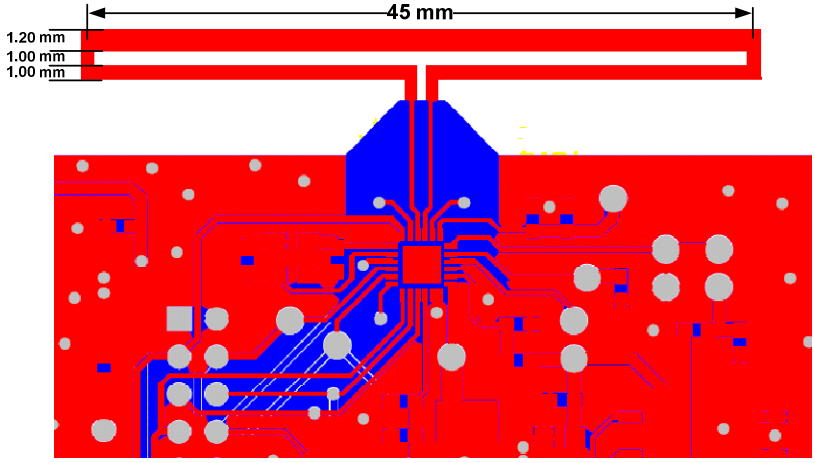


Figure 8: Layout example of a folded dipole antenna.

Designing PCB-antennas requires the use of dedicated CAD software which take into account board materiel properties and antenna geometries. The layout proposal shown in Figure 8 is an example designed for a 2 layers FR4 PCB with 0.8 mm thickness. Placing ground close to the antenna structure (either top or bottom layer) will highly decrease the antenna performance (gain and directivity).

5.1.2 50 Ohm matching

The EM9201/02 can also be used with a 50Ω–termination to match a standard measurement system or a 50Ω–antenna structure. In that case, a matching circuit needs to be applied such that the required impedance conversion from the 50 Ω to the differential 200Ω antenna port impedance can be ensured.

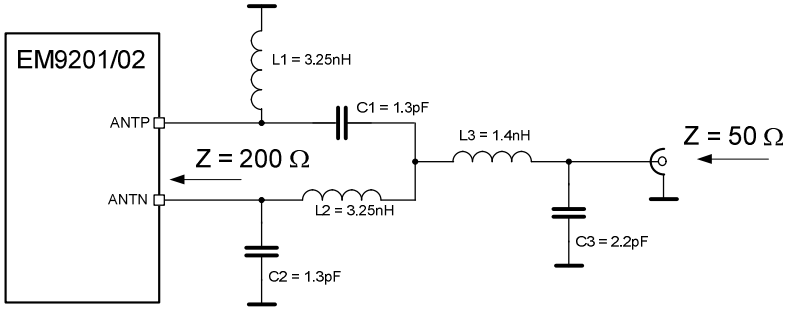


Figure 9: Matching circuit for 50 Ohm antenna.

Figure 9 shows a circuit example for such a matching network. Please note that also here the layout around the antenna port - both for the chip and attached antenna connector – needs to be done with having RF guidelines in mind.

5.2 XTAL Oscillator

In order to achieve low power operation and good frequency stability of the XTAL-oscillator, certain considerations with respect to the Quartz load capacitance C_0 need to be taken into account. Figure 10 shows a simplified block diagram of the amplitude regulated oscillator used in the EM9201/02.

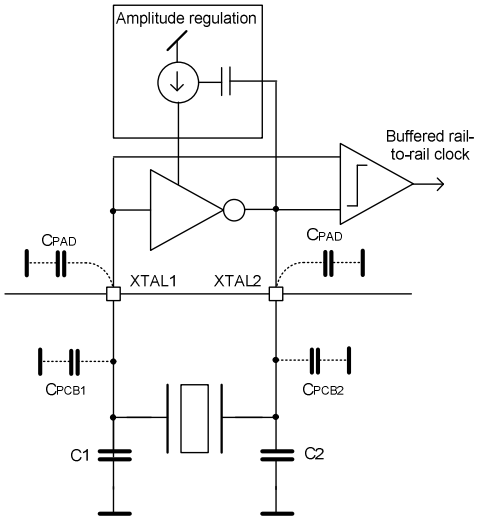


Figure 10: Amplitude regulated XTAL oscillator.

Low power consumption and fast start-up time is achieved by choosing a Quartz crystal with a low load capacitance C_0 – a reasonable choice is e.g. C_0=10pF as used in the typical application described in Section 9. To achieve good frequency stability the following equation then needs to be satisfied:

$$C_0 = \frac{C_1' \cdot C_2'}{C_1' + C_2'}$$, where $C_1' = C_1 + C_{PCB1} + C_{PAD}$, $C_2' = C_2 + C_{PCB2} + C_{PAD}$.

Capacitors C_1 and C_2 are external (SMD) components, C_{PCB1} and C_{PCB2} are PCB routing parasites and C_{PAD} is the equivalent small-signal pad-capacitance. The value of C_{PAD} is around 1pF for each pad.
The routing parasites should be minimized by placing Quartz and C_1 / C_2 close to the chip, not only for easier matching of the load capacitance C_0 , but also to ensure robustness against noise injection.

To achieve good noise immunity against external interference, the XTAL oscillator is designed with low input impedance using a chip-internal 260kΩ resistor between XTAL1 and XTAL2. In case the noise robustness needs to be further increased, an external parallel resistor can be added at the cost of extra current consumption.

5.3 PCB Guidelines

A number of PCB guidelines have to be respected in order to ensure proper RF operation of the EM9201/02, also due to the presence of a powerful DCDC converter. Generally, it is recommended to use at least a 2 layers PCB, dedicating one layer to one common ground plane covering all external components and the chip itself (the die pad should also be connected to this ground plane). Furthermore, prioritized layout focus should be kept for the following subjects:

1. Antenna port (and matching network).
2. Power supplies.
3. XTAL oscillator.
4. DCDC converter

5.3.1 Antenna port (and matching network)

Keep the EM9201/02 ANTN/ANTP symmetry in component- and via-placement, as well as line-routing. Place 100Ω transmission lines between the EM9201/02 RF output pins and the antenna output (or the matching network). In any case, try to minimize RF trace lengths:
Respect also a 3mm clearance to ground close to RF transmission lines and components (matching network). In particular, respect clearance to ground for antenna structure (varies with antenna topology).
Do not put a ground plane below antenna structure to avoid gain loss and directivity modification.

5.3.2 Power supply

The power supplies have to be properly decoupled. In particular, the decoupling on AVDD_PA (Power supply for PA) and VDD (power supply for digital part) is critical: the decoupling capacitors have to be put as close as possible to the pin.
In any case, the ground connections have to be as short as possible using vias directly to the ground plane.
Avoid sharing vias between different signals.

5.3.3 XTAL oscillator

Connect each capacitor of the XTAL oscillator to ground by a separate via, also separated from XTAL ground pads. Please also read the consideration regarding PCB routing parasites described in Section 5.2 above.

5.3.4 DCDC converter

The series routing resistance of the two DCDC-pins SW_DCDC and VSS_DCDC can have a strong impact on the EM9201/02 DCDC converter efficiency. Therefore, the trace-length between the coil and the EM9201/02 pins should be minimized.

5.3.5 Layout example

As an example of a well designed PCB the layout shown in Figure 11 can be inspected. It shows how the EM9201/02-Version 1 (with DCDC-converter) is placed together with all external components and a 50 Ω RF-port (see also 5.1.2).

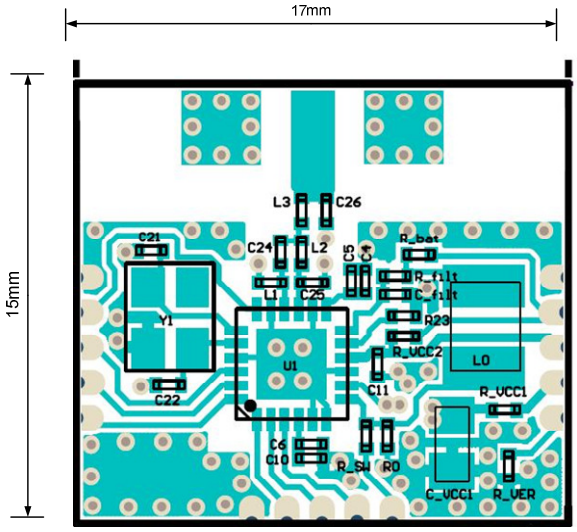


Figure 11: Layout example for good component placement.

On the left side of the IC the Quartz (Y1) together with load capacitors C21/C22 are placed, while on the right side the DCDC-coil (L0) can be found. Both components are very close to the IC as routing parasites need to be minimized. To the North of the EM9201/02 one can find the 50Ω/200Ω -matching network (L1, L2, L3, C24, C25,C26). Decoupling caps for the supply (AVDD_PA: C4,C5 and VDD: C6, C10) are also in close vicinity of the chip, such that their effect on spike reduction is maximized.

6. Versions and ordering information

The EM9201/02 is available in two different Versions as summarized in the table below. The two versions differ only in one metal layer and therefore have the same pin-out.

	Version	Description /Features	Applications / Comments
1	DC/DC step-up	2.4 GHz transceiver with on-chip DC/DC step-up converter for 1.5V single batteries. - 26 MHz crystal required. - 1 or 2 Mb/s (only EM9202)on air data-rate. - Xtreme low-power mode for DC/DC. - BPM mode available.	RF application where only one 1.5V battery is available, like e.g. wireless mouse.
2	no DC/DC – direct battery supply	2.4 GHz transceiver for direct 3V battery supply (or external LDO). - 26 MHz crystal required. - 1 or 2 Mb/s (only EM9202) on air data rate. - Power-down mode.	Wireless applications relying on 3V button cells (e.g. in watches) or where an external LDO is available (USB dongle)

6.1 Ordering information

Ordering Code	Description	Packaging	Container
EM9201-V1	1 Mb/s Transceiver with DCDC	MLF24	TBD
EM9201-V2	1 Mb/s Transceiver without DCDC	MLF24	TBD
EM9202-V1	1 / 2 Mb/s Transceiver with DCDC	MLF24	TBD
EM9202-V2	1 /2 Mb/s Transceiver without DCDC	MLF24	TBD
EMEVK9201/02	Evaluation Kit		

6.2 Package marking

EM9201 Version 1 (with DCDC)

1	2	3	4	5	6
A	9	2	0	1	0
B	0	1			
C					

EM9201 Version 2 (without DCDC)

1	2	3	4	5	6
A	9	2	0	1	0
B	0	2			
C					

EM9202 Version 1 (with DCDC)

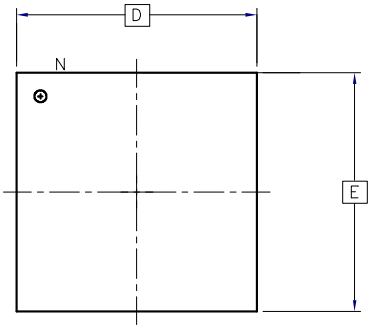
1	2	3	4	5	6
A	9	2	0	2	0
B	0	1			
C					

EM9202 Version 2 (without DCDC)

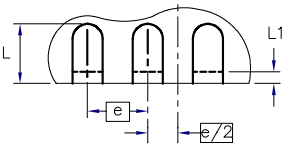
1	2	3	4	5	6
A	9	2	0	2	0
B	0	2			
C					

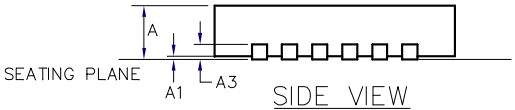
7. Package Information

MLF24 4mm x 4mm

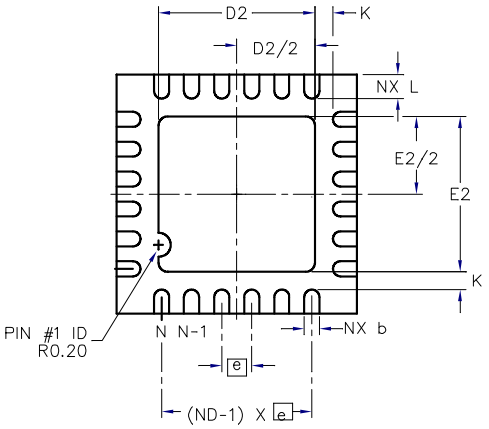


TOP VIEW





SIDE VIEW



BOTTOM VIEW

mm	MIN	NOM	MAX
A	0.80	0.85	0.95
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20 MIN	
D		4.0 BSC	
E		4.0 BSC	
L1		0.15 mm MAX	
N		24	
ND		6	
NE		6	
L	0.35	0.40	0.45
b	0.18	0.25	0.30
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70

8. Typical Operating Characteristics

In this chapter, typical operation characteristics of the EM9201/02 are described. The measurements should help to understand better the main functions of chip and can be seen as a complement to the tabular specifications stated in the beginning. The following is shown:

1. Version 1 and Version 2 start-up scenarios.
2. DCDC Efficiency versus load.
3. RX-Sensitivity (BER / PER).

8.1 DCDC Converter Efficiency

The DCDC converter efficiency is evaluated by loading its output VCC1 (=VCC2) with an external current ILext for a fixed input (battery) voltage applied to VBAT. The efficiency η := Pout/Pin = V(VCC1)* ILext / (V(VBAT)*Ibat) is then plotted against the load-current for the three main DCDC-operation modes: CCM- / burst- and Xtreme-mode – see also Section 3.2.6. Please note that in these measurements the chip-internal current consumption (from VCC2) is included!

Setup: EM9201/02-Version 1 configured like described in Section 9.1, with L1 = 10uH / ESR=110mΩ, C3=22uF (Ceramic X5R). The measured DCDC output voltage in CCM / burst-mode is 2.13V and 2.0V in Xtreme-mode – this has to be taken into account when looking at the figures below.

8.1.1 CCM / Burst-mode efficiency

Figure 12 shows the measured DCDC converter efficiency versus the fully available external load current 0…100mA, when the EM9201/02 is Standby-mode (i.e. chip-internal current cons. is approx 150uA). Three different input supply voltages (applied on VBAT) at 0.85 / 1.2 / 1.4V are taken as parameter.

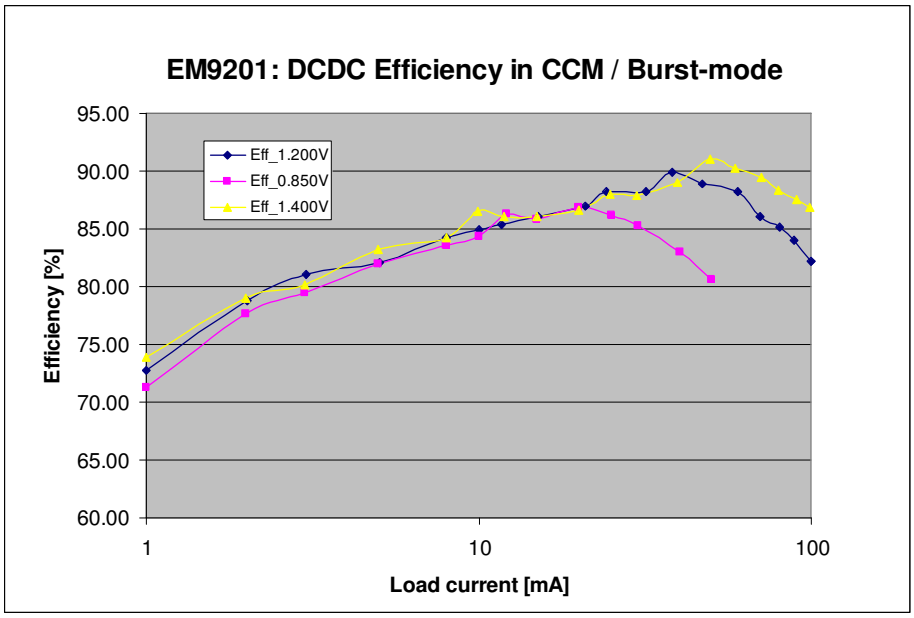


Figure 12: Typical measured DCDC-efficiency in CCM / burst-mode.

In this measurement, an efficiency η >85% is achieved for load currents 10 … 30mA and battery supplies greater than VBAT = 0.85V. At battery supplies around 1.2V and load currents of 50mA close to 90% efficiency can be observed.

8.1.2 Xtreme-mode efficiency

Figure 13 shows the efficiency-performance versus load current for the ultra low-power DCDC mode called “Xtreme-mode”, where the on-chip VCC2 consumption is only approx. 3uA. Again, three measurement traces are plotted for 0.85 / 1.2 /1.4V input voltage, covering a load range 0… 500uA.

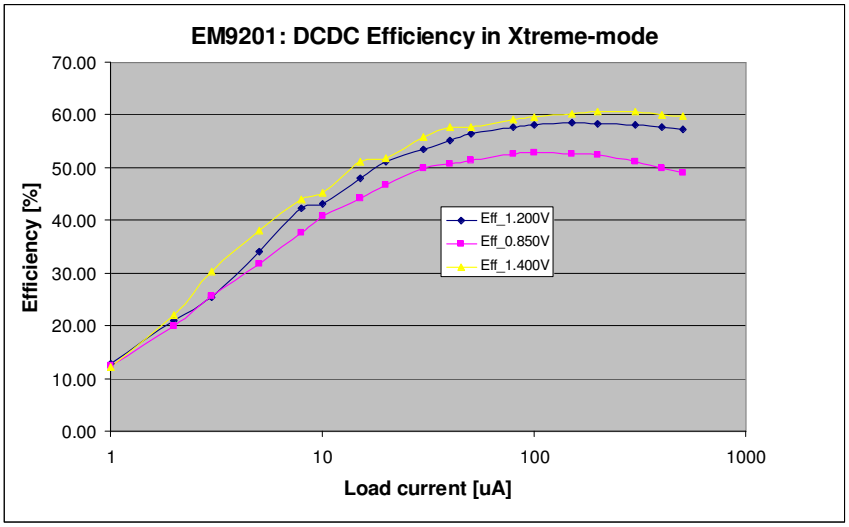


Figure 13: DCDC converter efficiency in Xtreme-mode.

The efficiency in this mode achieves a typical value of η = 55% at a load-current of 30uA.

8.1.3 Xtreme-mode battery versus load-current

For most battery powered applications, the equivalent battery current is of interest – especially when EM9201/02's low power Xtreme-mode is used. Figure 14 shows the battery current versus the load current for 0.85 / 1.2 / 1.4V supply (battery) – it is actually the same data as used to derive the efficiency plots shown in Figure 13.

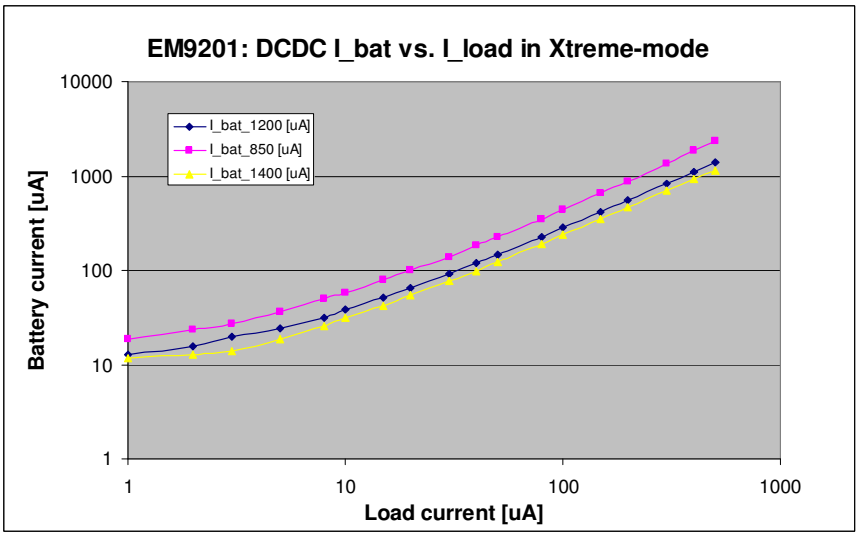


Figure 14: Xtreme-mode - battery current vs. load-current.

For typical supply voltages at 1.2V, the measured battery current is around 10uA when there is no external load, and rises to around 40uA when an external application would draw 10uA.

9. Typical Applications

In this chapter, typical application scenarios for the EM9201/02 are described – both for the DC/DC step-up configuration (Version 1) and for system using a direct battery (or LDO) supply.

9.1 Application schematic (Versions 1 and 2)

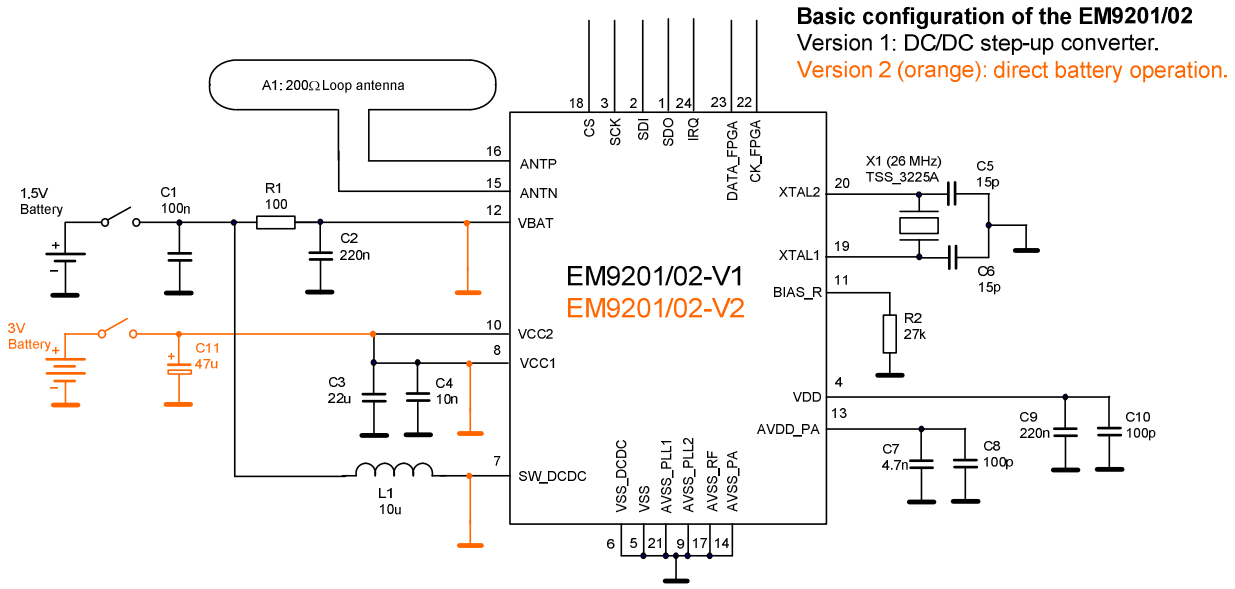


Figure 15: Application schematic for Version 1 (DC/DC) and Version 2 (no DC/DC). For Version 2 (orange), the pins VBAT, VCC1 and SW_DCDC are connected to system ground as well as components L1, R1, C2 and C3 need to be removed.

Component	Value	Footprint	Description
A1	200Ω	-	Printed loop antenna
C1	100n	0402	VBAT decoupling capacitor, +/- 10%
C2	220n	0805	VBAT filter capacitor, +/- 10%
C3	22uF	0805	DC/DC storage capacitor, X5R +/- 10%
C4	10nF	0402	VCC2 decoupling, +/- 10%
C5	15pF 1)	0402	XTAL load capacitor , +/- 5%
C6	15pF 1)	0402	XTAL load capacitor, +/- 5%
C7	4.7nF	0402	LDO-PA decoupling capacitor, +/- 10%
C8	100pF	0402	LDO-PA decoupling capacitor, +/- 10%
C9	220nF	0805	LDO-Digital decoupling capacitor, +/- 10%
C10	100pF	0402	LDO-Digital decoupling capacitor, +/- 10%
C11	47uF	1206	Version 2: VCC2 decoupling capacitor
L1	10uH	-	DC/DC coil: recommended ESR < 120mΩ, +/- 20%
R1	100 Ω	0402	VBAT filter resistor, +/- 10%
R2	27k Ω	0402	RF-biasing resistor, +/- 2%
X1	26 MHz	-	Crystal, +/- 50ppm, C0 = 10pF. Example: TSS_3225A

Note 1: C5 and C6 must have values that match the crystal load capacitance.

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