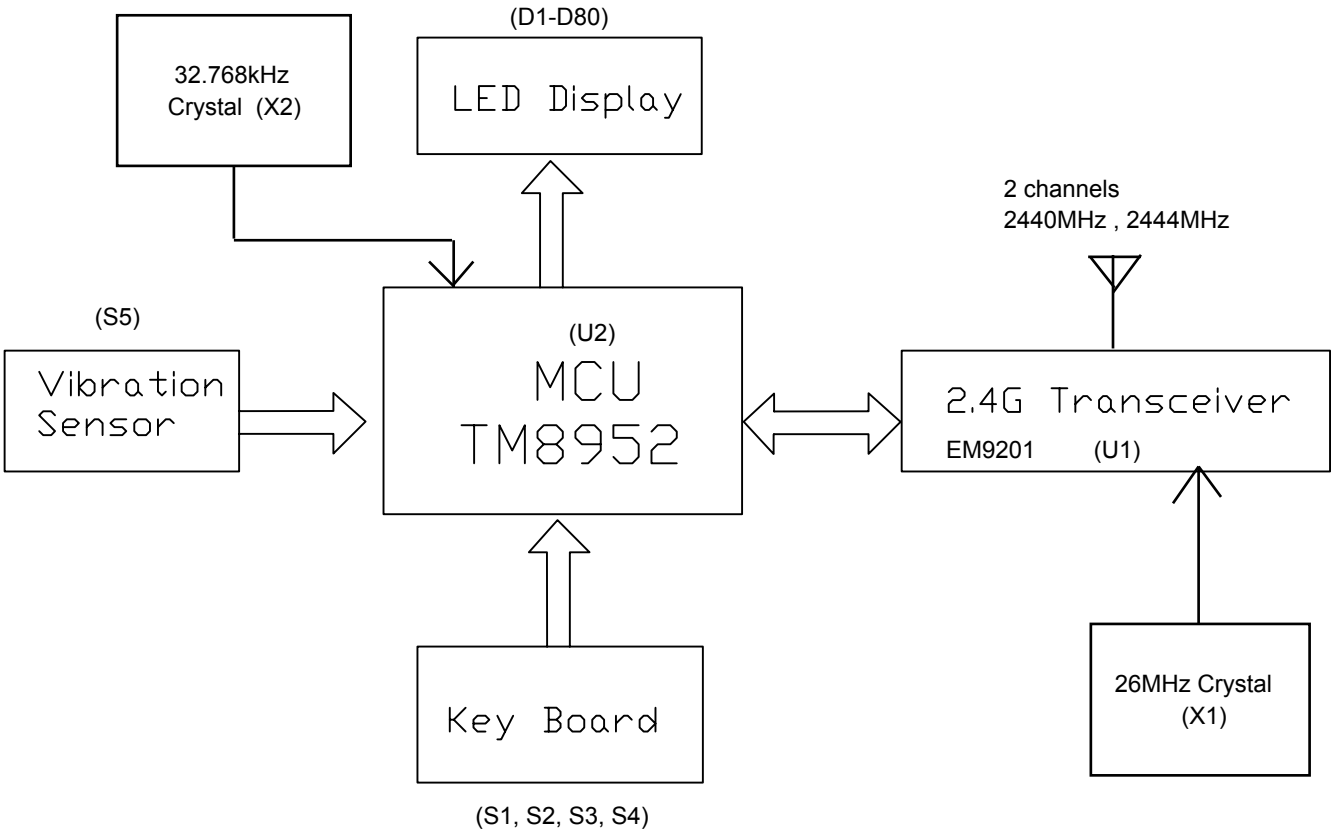

TextBand BLOCK DIAGRAM

Model: SWP1001

1.1 Block diagram

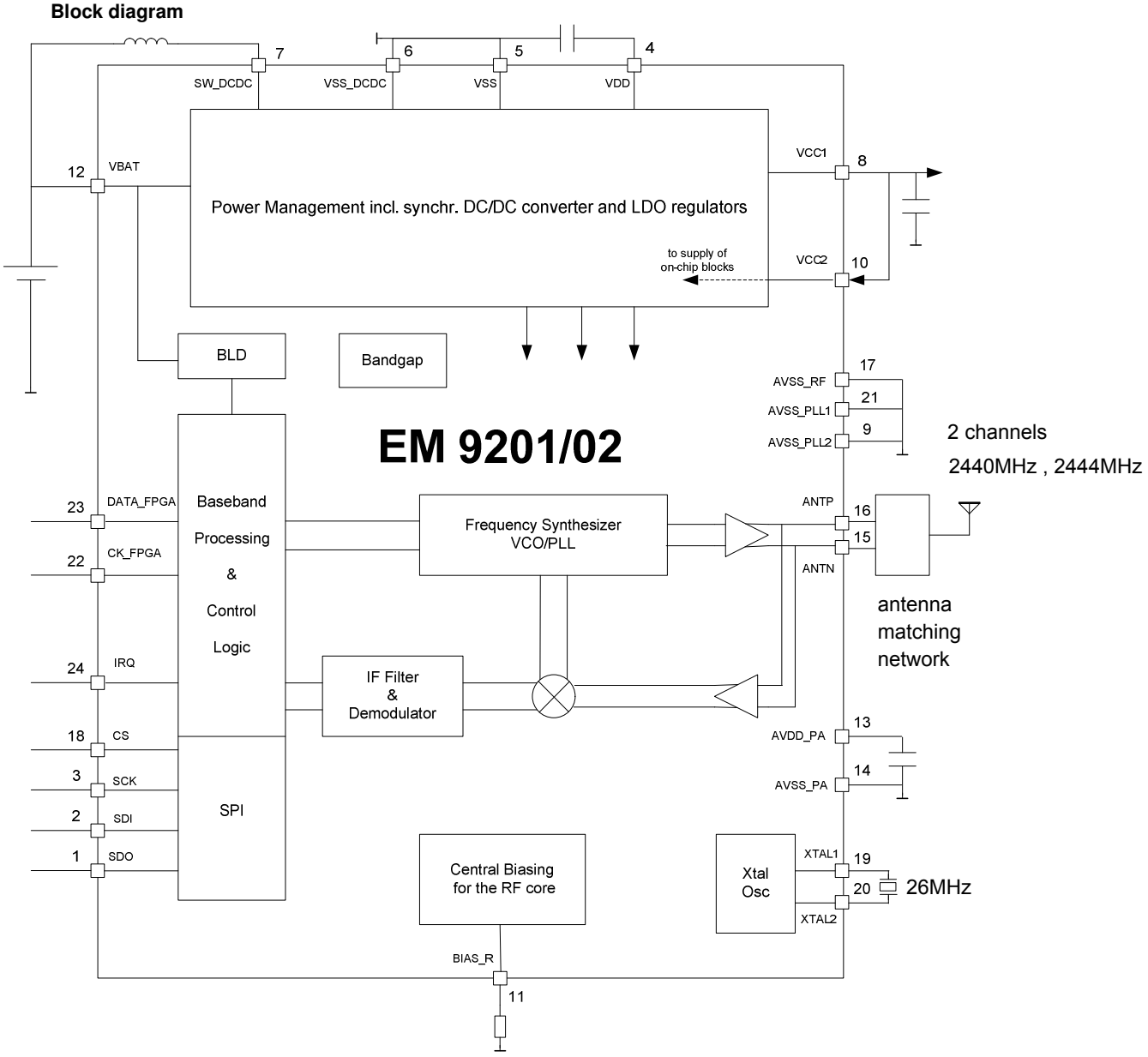

Figure 1 Simplified block diagram (DC/DC configuration).

1.2 Pin information (all versions)

Pin Nr	Name	I/O	Description
1	SDO	O	SPI data output
2	SDI	I	SPI data input
3	SCK	I	SPI clock input
4	VDD	O	Positive supply of digital part (baseband and frequency synthesizer)
5	VSS		Negative supply of digital part (plus ESD protection digital segment) [1)]
6	VSS_DCDC		Negative supply for DC/DC converter [1)]
7	SW_DCDC	I/O	Coil switch of DC/DC converter
8	VCC1	O	Output of DC/DC converter. On Version 2 (no DC/DC) connected to ground [2)]
9	AVSS_PLL2		Negative supply of PLL [1)]

Pin Nr	Name	I/O	Description
10	VCC2	I	Feedback / for chip supply, to be connected to VCC1 (plus ESD protection)
11	BIAS_R	I/O	Terminal for bias-setting resistor
12	VBAT		Positive battery supply (for DC/DC). On Version 2, connected to ground.
13	AVDD_PA	O	Regulated output voltage of PA supply; not to be loaded by any external circuitry
14	AVSS_PA		Negative supply of PA [1)]
15	ANTN	I/O	Negative antenna terminal
16	ANTP	I/O	Positive antenna terminal (input in RX-, output in TX mode)
17	AVSS_RF		Negative supply of RF part (plus ESD protection Analog/RF segment) [1)]
18	CSN	I	SPI Chip Select
19	XTAL1	I	Xtal oscillator input
20	XTAL2	O	Xtal oscillator output
21	AVSS_PLL1		Negative supply of PLL [1)]
22	CK_FPGA	O	Clock out for optional FPGA
23	DATA_FPGA	I/O	Data terminal for optional FPGA
24	IRQ	O	Interrupt output for external hostcontroller

Note 1: For a proper operation of the chip, this terminal shall be connected to a common ground plane

Note 2: Version 1 is the EM9201/02 with on-chip DCDC converter; Version 2 has no DC/DC.